Am8150

Display Refresh Controller

DISTINCTIVE CHARACTERISTICS

- Address controller in bit-mapped graphics systems
- Performs video refresh, memory arbitration, dynamic RAM control, and dynamic RAM refresh functions
- 18-bit address supports 16K x 1, 16K x 4, 64K x 1, and 64K x 4 RAMs
- Supports pan and scroll
- Programmable priority of Graphics Processor (GP) access to display memory

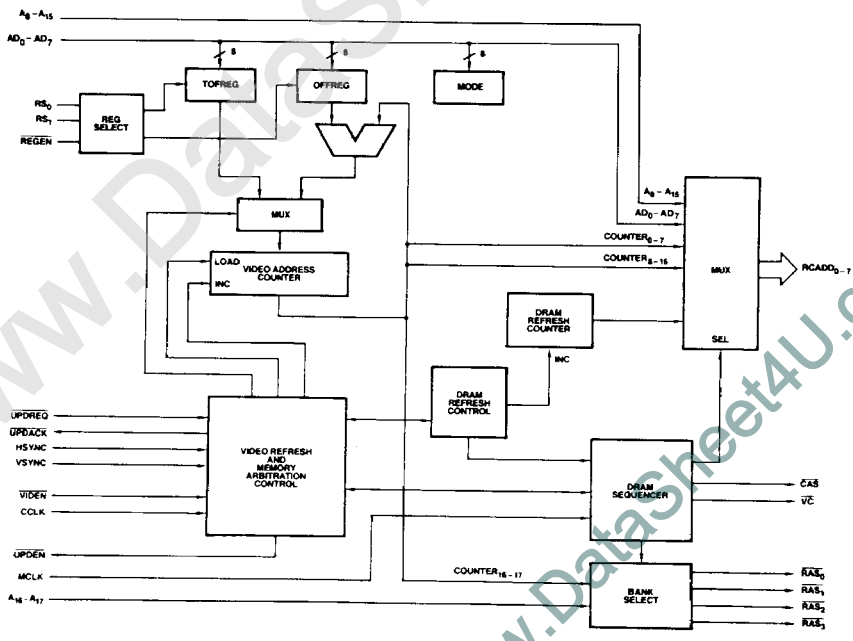
GENERAL DESCRIPTION

The Am8150 Display Refresh Controller (DRC) generates the addresses into the display RAM necessary to provide the video refresh function. It also provides the address interface between a bit-mapped display buffer and the Graphics Processor (GP) which updates the buffer. It acts as a memory access arbiter (permitting CPU access to the display memory at user-defined times), a video refresh controller, and a dynamic RAM refresh controller. It provides the signals ($\overline{RAS}$, $\overline{CAS}$, and video latch enable) and the timing necessary to cycle the dynamic RAMs and latch the video word in either random access or page mode.

The DRC provides the GP with an 18-bit address path to the bit map. Referring to the block diagram, the 8-bit multiplexer chooses the row or column address bits for the dynamic RAM. The inputs to this multiplexer are the address supplied by the GP, the Video Address Counter (VAC), and the dynamic RAM refresh counter. The two high-order bits of the address (from the GP or the video refresh counter) control a bank select decoder which activates one of four $\overline{RAS}$ lines. Each $\overline{RAS}$ line drives a separate bank of dynamic RAMs.

The DRC contains four write-only 8-bit registers which are programmed by the host. These contain the Top of Frame Address, the Offset, and the operating modes.

BLOCK DIAGRAM



BD003111

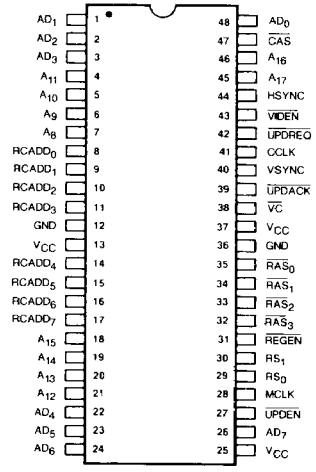
December 1985

Order # 04478C

RELATED PRODUCTS

Part No.	Description
Am8151	Graphics Color Palette
Am8157	Video Shift Register
Am8158	Video Timing Controller
Am8177	Video Data Serializer

CONNECTION DIAGRAM



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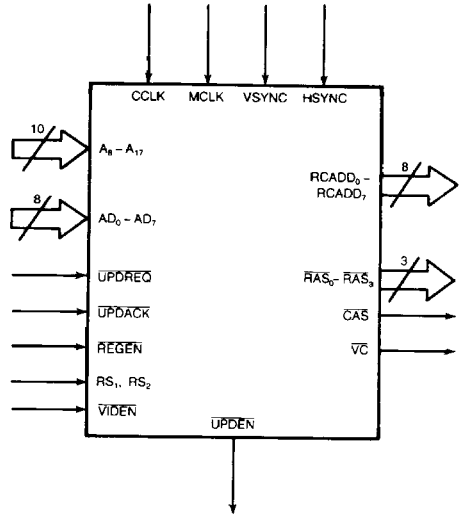
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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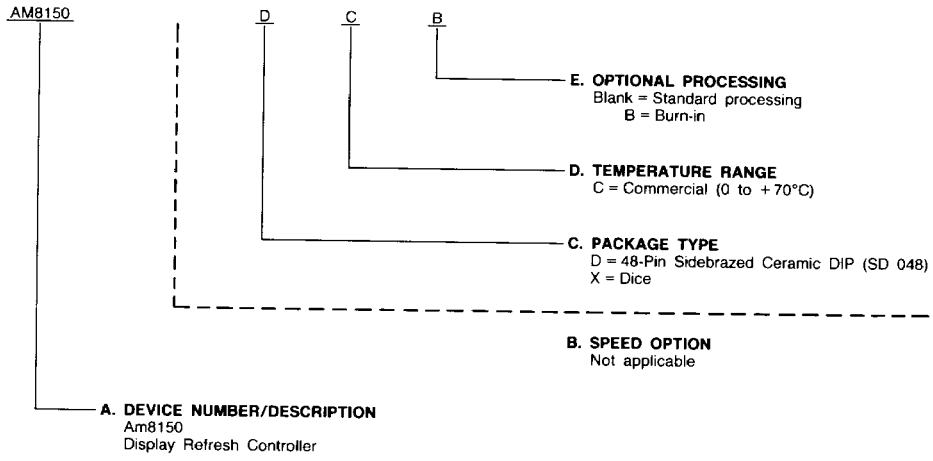
V_{CC} = Positive Power Supply
GND = Ground

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM8150	DC, DCB, XC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$AD_0 - AD_7$ Address/Data (Inputs (8))
When loading the 8-bit registers, data is taken from $AD_0 - AD_7$. These eight lines are also the low order bits of the address bus (see description of $A_8 - A_{17}$ below).

$A_8 - A_{17}$ Address (Inputs (10))
These ten inputs are concatenated with $AD_0 - AD_7$ to make up the 18 address lines used by the graphics processor to access the display RAM. A_{17} is the most significant bit (MSB) and AD_0 is the least significant bit (LSB).

A_{16} and A_{17} are decoded to drive one of the four $\overline{RAS}$ signals. A_8 through A_{15} provide the row address. AD_0 through AD_7 provide the column address. When using 16K x 4 RAMs, AD_1 through AD_6 provide column address (AD_0 and AD_7 are "Don't Cares" in this case).

RS_0, RS_1 Register Select (Inputs (2))
These two inputs are decoded to select one of the four 8-bit registers to be loaded with the data on $AD_0 - AD_7$. The register is latched on the LOW-to-HIGH transition of $\overline{REGEN}$. See Am8150 Register Set.

$\overline{REGEN}$ Register Enable (Input)
The input data on $AD_0 - AD_7$ is latched into one of the four internal registers on the LOW-to-HIGH transition of $\overline{REGEN}$. The register to be loaded is selected with RS_0, RS_1.

$\overline{UPDREQ}$ Update Request (Input)
This input signals a request from the GP to access the display RAM (either for a read or write). The DRC recognizes $\overline{UPDREQ}$ on the next positive transition of MCLK provided the set-up time (AC Parameter 1) is met.

$\overline{UPDACK}$ Update Acknowledge (Output, Open Collector)
This output signal is the handshaking signal which indicates that the current display RAM access has NOT been completed and that the GP must wait. This signal goes active (LOW) following $\overline{UPDREQ}$ and stays active until the cycle has gone to completion. In the case of a write, the address and data should remain valid until $\overline{UPDACK}$ goes inactive.

$\overline{UPDEN}$ Update Enable (Output)
$\overline{UPDEN}$ is active except during video and dynamic RAM refresh cycles. It identifies when a cycle can be granted to the GP. $\overline{UPDEN}$ should be used to gate the write enable signal(s) to the display memory so that writes occur only when the GP is actually given access. In the case where the data-in and data-out pins on the RAMs are connected together, this signal should also be used to gate the data into the array for a write.

MCLK Master Clock (Input)
This clock is used to generate the timing relationships among $\overline{RAS}$, $\overline{CAS}$, and the Row/Column multiplexer selects. The frequency is dependent upon the time specifications for the dynamic RAM being used. See the section on CCLK and MCLK Considerations.

CCLK Character Clock (Input)
CCLK determines the rate at which RAM cycles for video refresh are executed. CCLK may be taken directly from the CCLK output of the Am8158 Video Timing Controller. The CCLK period will be the pixel period times the width (in pixels) of the display RAM word.

$RCADD_0 - RCADD_7$ Row/Column Address (Outputs (8))
These outputs are the multiplexed row and column addresses which are sent to the dynamic RAMs. These are standard TTL outputs and will have to be buffered to drive a display memory of more than about sixteen dynamic RAMs.

$\overline{RAS_0} - \overline{RAS_3}$ Row Address Strobe (Outputs (4))
$\overline{RAS}$ strobes the row address into one of up to four banks of RAM in the display memory. It is also used to strobe the refresh address during a dynamic RAM refresh cycle. Depending on the array size, these signals may need to be buffered.

$\overline{CAS}$ Column Address Strobe (Output)
$\overline{CAS}$ strobes the column address into all of the dynamic RAMs in the display memory. All of the banks of memory receive the same $\overline{CAS}$ signal. This signal may need to be buffered.

$\overline{VC}$ Video Cycle (Output)
This is used externally to latch the parallel video output from the display RAMs. It may be used directly to drive the $\overline{VLE}$ input on the Am8157 Video Shift Register(s).

HSYNC Horizontal Synchronization (Input)
This input causes the DRC to add the contents of the Offset Register to the Video Address Counter, thereby advancing to the first word of the next scan line. It also causes the DRC to execute the dynamic RAM refresh cycles as programmed in the Mode Register. HSYNC may be taken directly from the HSYNC output of the Am8158 VTC.

VSYNC Vertical Synchronization (Input)
This input causes the Video Address Counter to be loaded with the contents of the Top of Frame (TOF) Register. During vertical blank, HSYNC pulses are prevented from causing the offset to be added to the Video Address Counter.

$\overline{VIDEN}$ Video Enable (Input)
$\overline{VIDEN}$ is active (LOW) during the active video time (that is, whenever horizontal blank and vertical blank are both inactive). $\overline{VIDEN}$ is used in the arbitration logic.

V_{CC} TTL Positive Power Supply

GND Ground

FUNCTIONAL DESCRIPTION

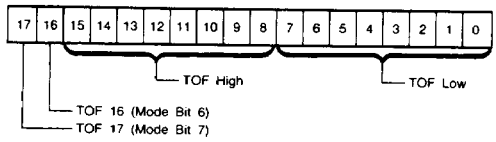
Register Set

The DRC has four 8-bit registers which must be loaded by the host. The registers are loaded by placing the desired data on $AD_0 - AD_7$, placing the register address on RS_1, RS_0 and strobing the data into the register using $\overline{REGEN}$. The data is loaded into the register on the LOW-to-HIGH transition of $\overline{REGEN}$ (see timing diagram "Loading Registers"). The Offset Register must be loaded first, then the Mode Register. The Top of Frame Registers may be loaded at any time but are normally changed only during vertical blank.

RS_1	RS_0	Register Name
		Top of Frame (TOF)
0	0	Low
		Top of Frame (TOF)
0	1	High
1	0	Offset
1	1	Mode

The Top of Frame Registers are concatenated to specify the address of the first word in the video buffer to be displayed on the screen (that is, the word which is to appear at the upper

left corner of the screen). The 18-bit address is made up as indicated below:



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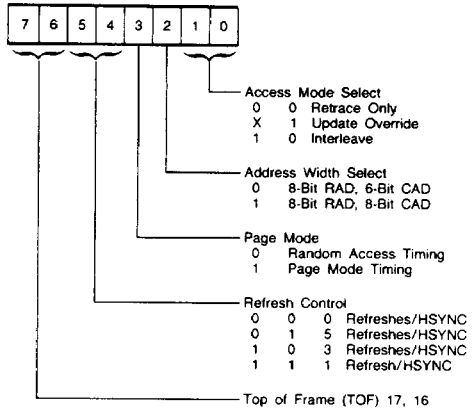
See the sections on Display Refresh and Scrolling and Panning for further information on the programming of the Top Of Frame Registers, but remember that this is a word address, not a pixel address.

The Offset Register is used to treat the case where the width of the display memory is not the same as the width of the screen (the display memory is wider to allow panning). At each HSYNC time, the contents of the Offset Register are added to the contents of the Video Address Counter which forces the display from the last word of the current line to the first word of the next line. See the section on Display Refresh for further information on the use of the Offset Register. Loading the Offset Register forces a hardware reset in the DRC and will abort any memory cycle in progress. For this reason, the Offset Register must be loaded first.

The Mode Register specifies the operating modes. The eight bits in this register are defined as follows:



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Display Refresh

A primary function of the DRC is to generate the addresses into the display RAM necessary to refresh the display. It does so with an 18-bit counter whose contents can be modified in three ways. The counter is called the Video Address Counter (VAC).

It is important to keep in mind that the addresses generated in the DRC are word and not pixel addresses. The word width is the number of pixels which are loaded into the shift register for each CCLK cycle.

When the DRC sees VSYNC , the VAC is loaded from the Top of Frame Registers. When the accesses begin for the first scan line, they will begin with the address contained in the Top of Frame Registers. Thus, the word whose address is contained in the Top of Frame Registers will appear at the upper left of the screen. If the screen size is the same as the display size, the Top of Frame Registers should be programmed to zero.

Once $\overline{\text{VIDEN}}$ has gone active (indicating active video), the DRC will access one word during each CCLK cycle (or every other CCLK cycle in the case of interleaved operation). It will also increment the VAC once for each video word it has accessed. Thus, video words are fetched in order and presented to the Am8157 VSR(s) for serialization. This procedure continues until $\overline{\text{VIDEN}}$ becomes inactive, indicating a horizontal or vertical blank period.

When the DRC receives HSYNC , the contents of the Offset Register are added to the VAC. If the screen width is the same as the display width, the Offset Register will have been programmed to zero and this is an effective NOP. In this case, the first word of the nth scan line is contiguous with the last word of the n -1th scan line. In the case where the display RAM is wider than the screen, the Offset Register will have been programmed with the difference (in words, not pixels). Thus the DRC will skip over the "unused" words to get to the words for the next scan line.

This addition is inhibited for HSYNC pulses which occur between the rising edge of VSYNC and the falling edge of $\overline{\text{VIDEN}}$. This insures that the value loaded from the Top of Frame Registers does not get altered by HSYNCs which occur during vertical blank.

The offset must be equal to or less than 126, and must be even.

Scrolling and Panning

It is possible to effect scrolling on a scan line basis, and if the display memory is wider than the physical screen, panning on a video word basis is possible. This is done as follows:

To scroll the contents of the display up (that is, to cause scan lines to disappear off the top of the screen and previously invisible scan lines to appear from the bottom of the screen), point the Top of Frame Registers to the left-most word of the "next" scan line. To scroll down, point the Top of Frame Registers to the left-most word of the "previous" scan line.

Soft scrolling can be effected by loading the Top of Frame Registers with a series of pointers between the beginning point and the ending point. Obviously, the scroll rate will be determined by the rate at which the pointers are changed.

The display will "wrap" if there are scan lines remaining at the bottom of the screen when the VAC gets to the bottom of the display.

Panning can be effected by loading the Top of Frame Registers with values which do not point to the left-most word of a scan line.

Since there are multiple segments of the Top of Frame Registers, it is important to insure that the VAC never gets loaded with a partially updated Top of Frame value. This can be done by always modifying the registers right after the leading edge of VSYNC.

Graphics Processor (GP) Access to the Display RAM

The DRC provides the address pathway to allow the GP access to the display RAM. The address is presented on $A_8 - A_{17}$ and $AD_0 - AD_7$. The GP signals a request by driving $\overline{\text{UPDREQ}}$ active which makes $\overline{\text{UPDACK}}$ active asynchronously. When the cycle actually begins, $\overline{\text{UPDEN}}$ will go active. When the cycle is complete $\overline{\text{UPDACK}}$ goes inactive and the GP may continue.

Since the display RAM (and the address pathway) may be busy taking care of display refresh, it is necessary to provide a

means to arbitrate the access requests. Three modes are available. The user programs bits 1 and 0 of the Mode Register to select the desired mode.

Retrace Only: This mode allows the GP access to the display RAM only when $\overline{\text{VIDEN}}$ is not active (and when no dynamic RAM refresh cycles are pending). This will be the case during vertical blank and horizontal blank. Depending on the relationships of blank and active video times (both horizontal and vertical), this may provide the GP access to the RAM about 10-30% of the time. Observe that this time occurs in bursts during horizontal and vertical blanking time. Retrace Only is selected by programming bits 1 and 0 of the Mode Register to 0,0.

Update Override: If a 1 is programmed in bit zero of the Mode Register, Update Override is selected (regardless of bit 1). In this mode, screen refresh is suspended and the VAC is not incremented. This mode will cause incorrect information to appear on the screen until the next VSYNC after Update Override is turned off, but allows the GP nearly 100% access to the display RAM. Dynamic RAM refresh cycles will still take priority over the GP accesses.

Interleaved Update: This mode allows the GP access to the display RAM on alternate CCLK cycles during video refresh. This permits update access at something greater than 50%. Since this allows display refresh cycles only on alternate cycles, the video RAM bandwidth must be doubled (with respect to what it otherwise would have had to have been). Interleaved access may not be combined with Page Mode operation.

The DRC provides three control pins for the GP interface: $\overline{\text{UPDREQ}}$ is an input which is asserted when the GP needs access to the display RAM. When the DRC sees $\overline{\text{UPDREQ}}$, it will drive $\overline{\text{UPDACK}}$ active (LOW) until the cycle has been completed. The system designer must insure that $\overline{\text{UPDACK}}$ is recognized by the processor.

When the DRC actually begins the display RAM cycle for the GP, it will make $\overline{\text{UPDEN}}$ active (LOW). The system designer should use $\overline{\text{UPDEN}}$ to gate write enable to the display RAM. This assures that writes occur only during the correct cycles. In addition, if the data-in and data-out pins on the RAMs are tied together, $\overline{\text{UPDEN}}$ should be used to gate the write data into the array.

The trailing edge of $\overline{\text{CAS}}$ may be used to latch the data during a read cycle. During a write cycle, the address and data must remain valid until the trailing edge of $\overline{\text{UPDACK}}$.

Dynamic RAM Refresh

The DRC is also used to perform the dynamic RAM refresh function. Refresh is accomplished beginning at HSYNC and is asynchronous to CCLK. Bits 5 and 4 of the Mode Register are used to control the number of refresh cycles executed at each HSYNC. An 8-bit counter is used to keep track of the refresh address. It is incremented once for every refresh cycle.

Each refresh cycle consists of a $\overline{\text{RAS}}$-only memory cycle; all four $\overline{\text{RAS}}$ lines are made active. The duration of $\overline{\text{RAS}}$ is six MCLK cycles, followed by four MCLK cycles for $\overline{\text{RAS}}$ precharge.

Some devices require 128 refresh cycles every 2 ms while others require 256 refresh cycles every 4 ms. In either case, one refresh cycle is required (on the average) every 15.625 microseconds.

The number of refresh cycles per HSYNC is:
HSYNC PERIOD/15.625 microseconds

For a 64 kHz horizontal frequency system, this works out to exactly 1.

The refresh cycles take place in the period between the beginning of HSYNC and the beginning of active video. The system designer must insure that this period is long enough to perform the required number of cycles. Each refresh cycle requires ten MCLK cycles.

Page Mode Operation

Page Mode operation of the display RAMs may be selected by programming bit three of the Mode Register to a one. This can be used to increase the video bandwidth or allow the use of slower RAM chips or both. The DRC uses ten MCLK periods to execute a non-page mode cycle and seven MCLK periods to execute a Page Mode cycle.

In Page Mode operation, the DRC performs video refresh cycles in page mode and performs CPU accesses with random cycle timing. For this reason, Page Mode operation cannot be combined with interleaved operation.

The system designer should be careful that Page Mode operations do not result in timing which violates the $\overline{\text{RAS}}$ pulse width specification for the RAM chips which are to be used.

CCLK and MCLK Considerations

In most systems, CCLK period will be equal to the pixel period times the number of bits accessed and loaded into the shift registers. When interleaved operation is used, CCLK period will be equal to $1/2$ the pixel period times the number of bits accessed (alternate CCLKs are used to access video data). CCLK will always be derived from the Dot Clock.

MCLK is used to clock a state machine which controls the RAM timing (in particular the relationship between $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, the address bits, and $\overline{\text{VC}}$). This timing is shown in detail in the timing diagrams. These diagrams can also be used to explain the lower bound on MCLK period.

The MCLK period will determine the time between the leading edge of $\overline{\text{RAS}}$ and the address bits changing. This is an AC parameter at the RAM chip and is called Row Address Hold Time (t_{RAH}). A "typical" DRAM requires 20 ns.

An additional restriction on the lower bound on MCLK period is set by the Column Access Time (t_{CAC}) of the devices in the array. There will be four MCLK HIGH times and three MCLK LOW times between the falling edge of $\overline{\text{CAS}}$ and the rising edge of $\overline{\text{VC}}$ (which should be used to latch the data in the serializer). Delays in the drivers should be taken into account.

A third restriction on the lower bound of the MCLK period is that CCLK must be low at the end of a RAM cycle. This means that MCLK $> 1/20$ CCLK for Random Mode, and MCLK $> 1/14$ CCLK for Page Mode.

The upper bound on MCLK period is:

In Random-Access Video Mode, MCLK period must be $< 1/10$ CCLK period.

In Page Mode, MCLK must be $< 1/7$ CCLK period.

In Interleaved Access Mode, MCLK period must be $\leq 1/10$ CCLK period.

In any case, MCLK period must be such that the programmed dynamic RAM refresh cycles can occur between HSYNC and active video. Each refresh cycle takes ten MCLK periods.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous (TTL) ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs for
High Output State (TTL) ..... −0.5 to +V_{CC} Max.
DC Input Voltage (TTL) ..... −0.5 to +7.0 V
DC Input Current (TTL) ..... −30 to +5.0 mA
DC Output Current (TTL) ..... 30 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

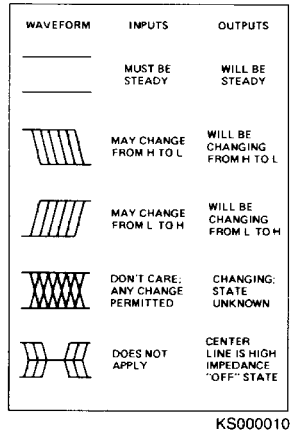
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbols	Parameter Descriptions	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.0 mA	2.4	3.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., All I_{OL} = 16 mA			0.5	V
V_{IH}	Input HIGH Level Voltage	V_{CC} = Max. Guaranteed Input HIGH Voltage for All Inputs (Note 4)	2.0			V
V_{IL}	Input LOW Level Voltage	V_{CC} = Min. Guaranteed Input LOW Voltage for All Inputs (Note 4)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_I = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IL} = 0.4 V			−550	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IH} = 2.4 V			100	μA
I_{SC}	Output Short-Circuit Current (Note 3)	V_{CC} = Max.	−10		−55	mA
I_{CC}	Supply Current	V_{CC} = Max., Outputs Open	360	450	650	mA
I_{VL}	Input Current at Max. Input Voltage	V_{CC} = Max., V_I = 5.5 V			1.0	mA

Notes: See notes following Switching Characteristics table.

KEY TO SWITCHING WAVEFORMS



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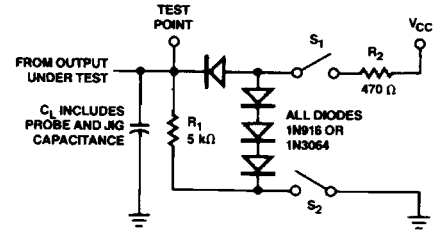
SWITCHING TEST CIRCUIT



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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

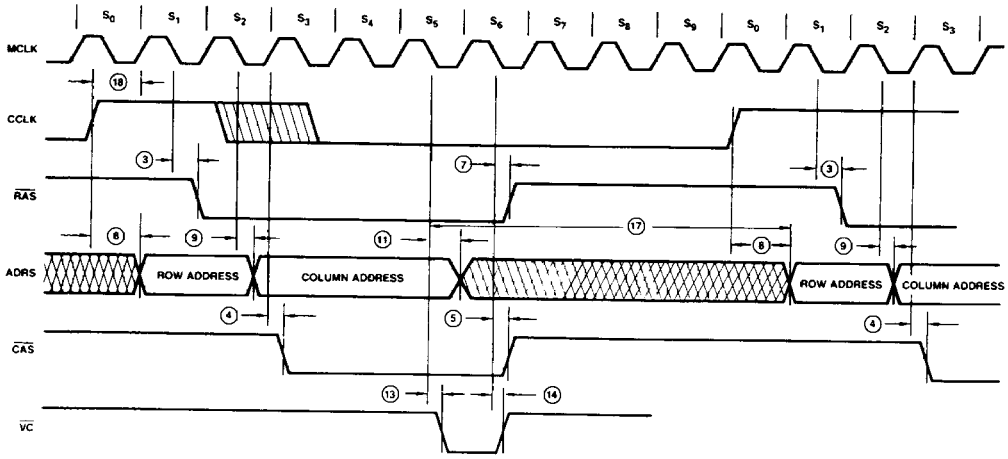
No.	Parameter Symbols	Parameter Descriptions	Min.	Max.	Units
1	t_S	$\overline{UPDREQ}\downarrow$ to MCLK↑ (Notes 6, 15)	12		ns
2	t_{PHL}	$\overline{UPDREQ}\downarrow$ to $\overline{UPDACK}\downarrow$		20	ns
3	t_{PHL}	MCLK↓ to $\overline{RAS}\downarrow$ (Notes 10, 13)	5	25	ns
4	t_{PHL}	MCLK↑ to $\overline{CAS}\downarrow$ (Note 11)	8	25	ns
5	t_{PLH}	MCLK↓ to $\overline{CAS}\uparrow$ (Note 14)	5	40	ns
6	t_{PLH}	MCLK↓ to $\overline{UPDACK}\uparrow$		30	ns
7	t_{PD}	MCLK↓ to $\overline{RAS}\uparrow$		40	ns
8	t_{PD}	CCLK↓ to RCADD = VIDEO RAD		40	ns
9	t_{PD}	MCLK↑ to RCADD = VIDEO CAD (Notes 10, 11)		30	ns
10	t_{PD}	MCLK↓ to RCADD = UPDATE CAD (Notes 10, 11)		40	ns
11	t_{PD}	MCLK↓ to RCADD = VIDEO INVALID		30	ns
12	t_{PD}	MCLK↓ to RCADD = VIDEO VALID (PM)		30	ns
13	t_{PHL}	MCKL↓ to $\overline{VC}\downarrow$		25	ns
14	t_{PLH}	MCLK↓ to $\overline{VC}\uparrow$ (Note 14)		25	ns
15	t_{PD}	CCLK↑ to RCADD = UPDATE RAD (Note 7)		40	ns
16	t_{PD}	MCLK↓ to RCADD = UPDATE RAD		30	ns
17	t_{PD}	MCLK↓ to RCADD = VIDEO VALID (RANDOM)		140	ns
18	t_S	CCLK↑ to MCLK↑ (Notes 8, 15)	15		ns
19	t_S	MCLK↑ to HSYNC↑ (Notes 12, 15)	2		ns
20	t_{PD}	MCLK↓ to RCADD = DRAM REFRESH ADDRESS (Note 13)		50	ns
21	t_{PD}	MCLK↓ to RCADD = DRAM REFRESH ADDRESS INVALID		30	ns
22	t_{PD}	CCLK↑ to $\overline{UPDEN}$ (BLANK)		30	ns
23	t_{PD}	CCLK↑ to $\overline{UPDEN}$ (INTERLEAVED)		30	ns
24	t_S	$\overline{UPDREQ}\downarrow$ to CCLK↑ (INTERLEAVED) (Note 15)	1		ns
25	t_{PD}	$AD_0 - AD_7$ to RCADD		30	ns
26	t_{PD}	$A_8 - A_{15}$ to RCADD		30	ns
27	t_S	RS to $\overline{REGEN}\downarrow$ (Note 15)	5		ns
28	t_S	AD to $\overline{REGEN}\uparrow$ (Note 15)	5		ns
29	t_H	$\overline{REGEN}\uparrow$ to RS (Note 15)	0		ns
30	t_H	$\overline{REGEN}\uparrow$ to AD (Note 15)	5		ns
31	t_W	$\overline{REGEN}$ Pulse Width	20		ns
32	t_W	MCLK HIGH (Note 9)	12.5		ns
33	t_W	MCLK LOW (Note 9)	12.5		ns
34	t_H	HSYNC↑ to MCLK↓ (Notes 12, 15)	15		ns

Notes*:

1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating ranges.
2. All typical values are $V_{CC} = 5.0$ V, $T_A = 25°C$.
3. The duration of the short-circuit should not exceed one second.
4. V_{IH}, V_{IL} are tested for each input at least once. Thereafter, hard HIGH and LOW levels are used for all other tests.
5. A combination of skewing the limits and adjusting the pulse test ambient temperature is used to ensure that the data sheet steady state limits are met at the ambient temperature specified.
6. Parameter 1 is the setup time required to ensure recognition of an Update Request in the next MCLK cycle. It is not an operating requirement.
7. Applies only in interleaved operation.
8. Parameter 18 is the setup time required to ensure recognition of CCLK in the next MCLK cycle. It is not an operating parameter.
9. See CCLK and MCLK Considerations in Functional Description section.
10. $\overline{RAS}$ falling edge to RCADD changing equal or greater than (MCLK minus 5 ns) (Note 15).
11. RCADD is valid (MCLK/2 minus 11.5 ns) prior to $\overline{CAS}$ falling edge (Note 15).
12. Not an operating requirement. Guarantees parameter 20.
13. RCADD is valid one MCLK low time prior to falling edge of $\overline{RAS}$.
14. $\overline{VC}$ rising edge to occur no later than 3 ns after $\overline{CAS}$ rising edge (Note 15).
15. Guaranteed by characterization/correlation to other AC parameters that are tested.
16. During this time, the last video character of the line is being shifted out.
17. Refresh and update cycles during blank are not synchronized to CCLK.
18, 19. The 2 CCLK periods following $\overline{VIDEN}\downarrow$ are allocated to completion of update cycles in progress, if any.
20. The third CCLK period following $\overline{VIDEN}\downarrow$ is allocated to $\overline{RAS}$ precharge in page mode, or idle otherwise.

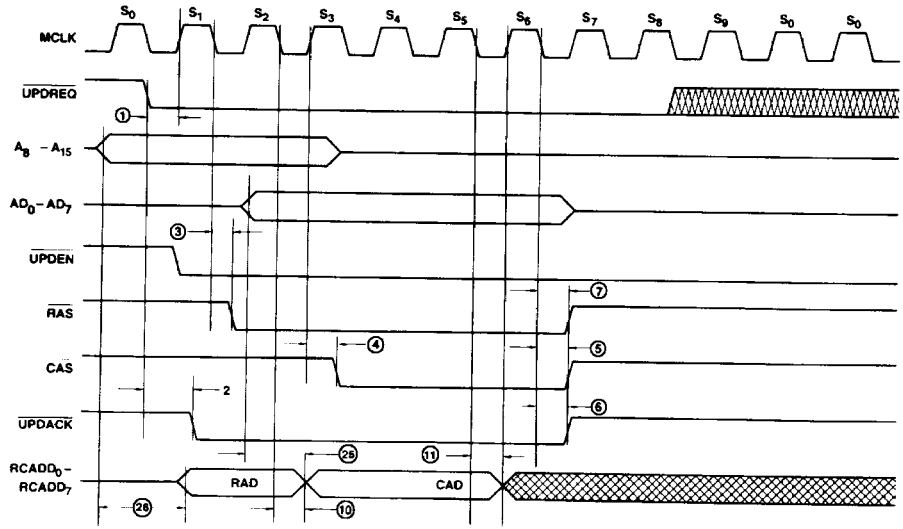
* Notes listed correspond to respective references made in DC Characteristics and Switching Characteristics tables, and Switching Waveforms section.

SWITCHING WAVEFORMS



WF020500

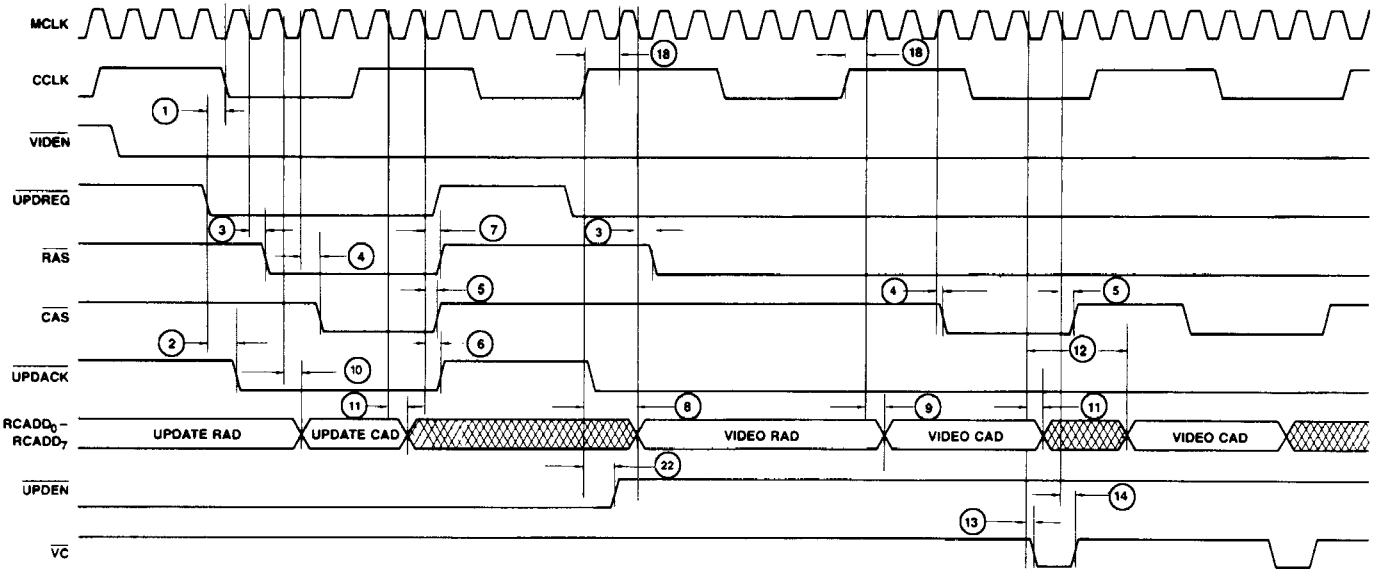
Random-Access Video Mode



WF020510

Update Cycle

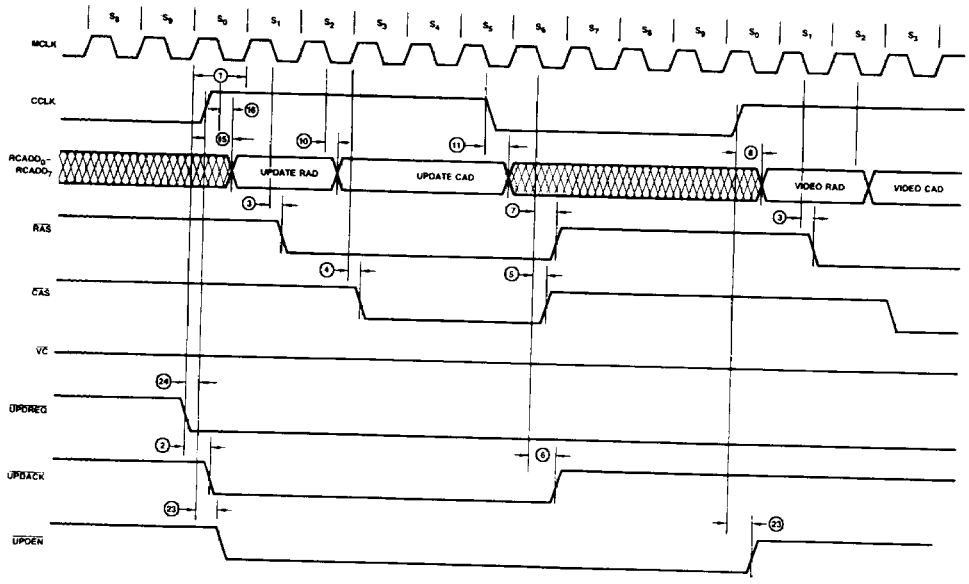
SWITCHING WAVEFORMS (Cont.)



WF020520

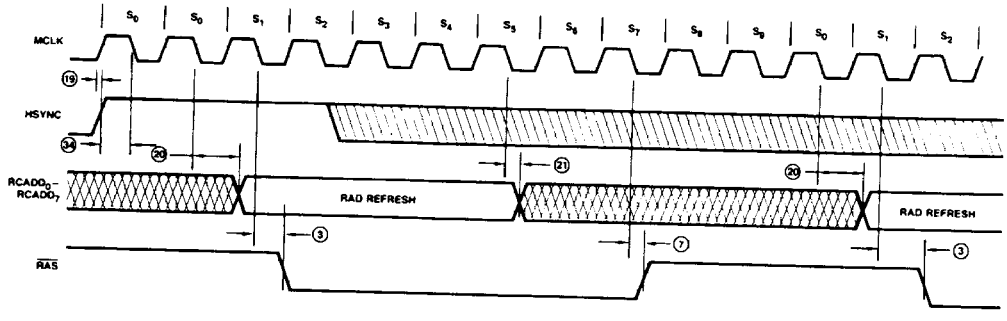
Page Mode Video

SWITCHING WAVEFORMS (Cont.)



WF020530

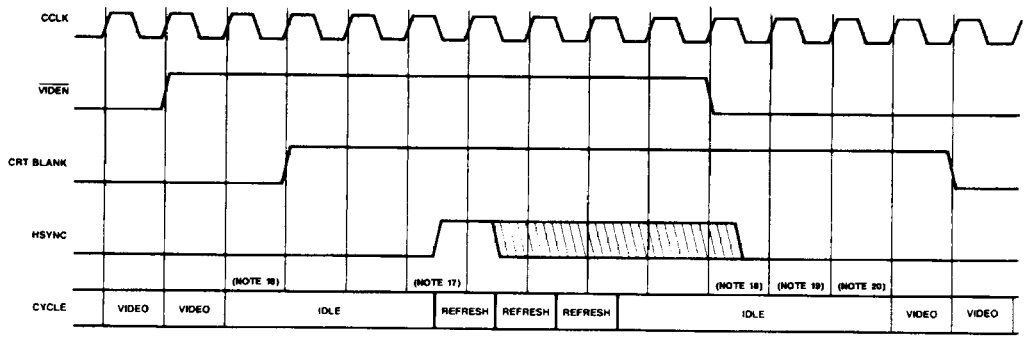
Interleaved Update/Video



WF020540

Refresh Cycles

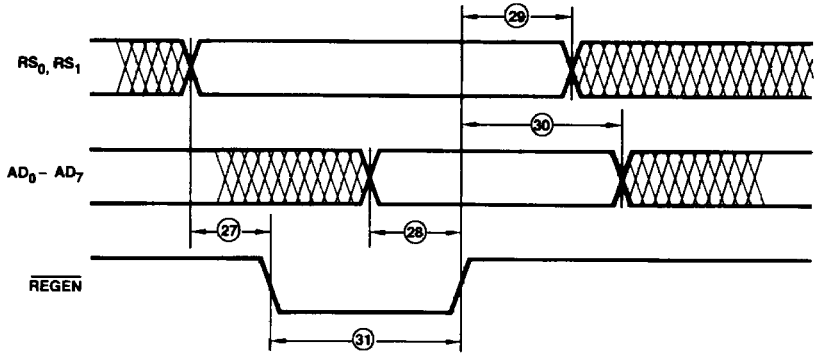
SWITCHING WAVEFORMS (Cont.)



WF020550

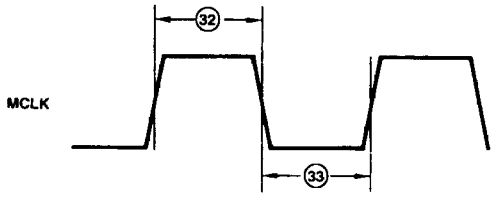
Notes: See notes following Switching Characteristics table.

Operating Sequence During Blank
(Random Cycle, Non-Interleaved, 3 Refresh Cycles, Cycle Programmed)



WF020560

Loading Registers

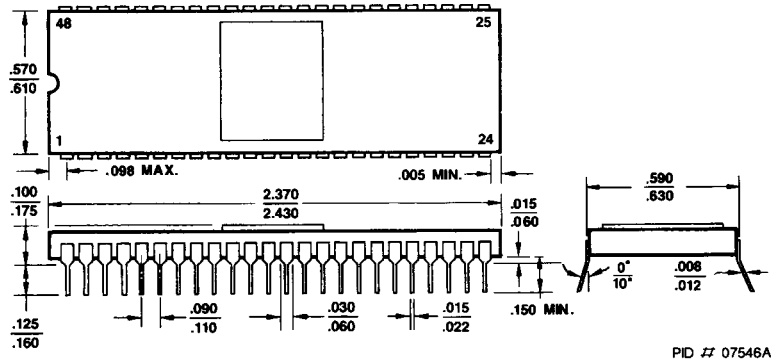


WF020570

MCLK Waveform

PHYSICAL DIMENSIONS

SD 048



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