Am8158

Video Timing Controller (with PLL)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Provides Dot Clock, Character Clock, HSYNC, VSYNC, and BLANK for bit-mapped graphics systems
- Fully programmable for all display sizes and resolutions
- On-chip crystal oscillator with times 5 Phase Locked LOOP (PLL) with a Dot Clock Out frequency range of 25 – 125 MHz. An external clock source can also be used.
- Fully compatible with Am815X Bit-mapped Graphics Family
- Operates with Dot Clock up to 125 MHz

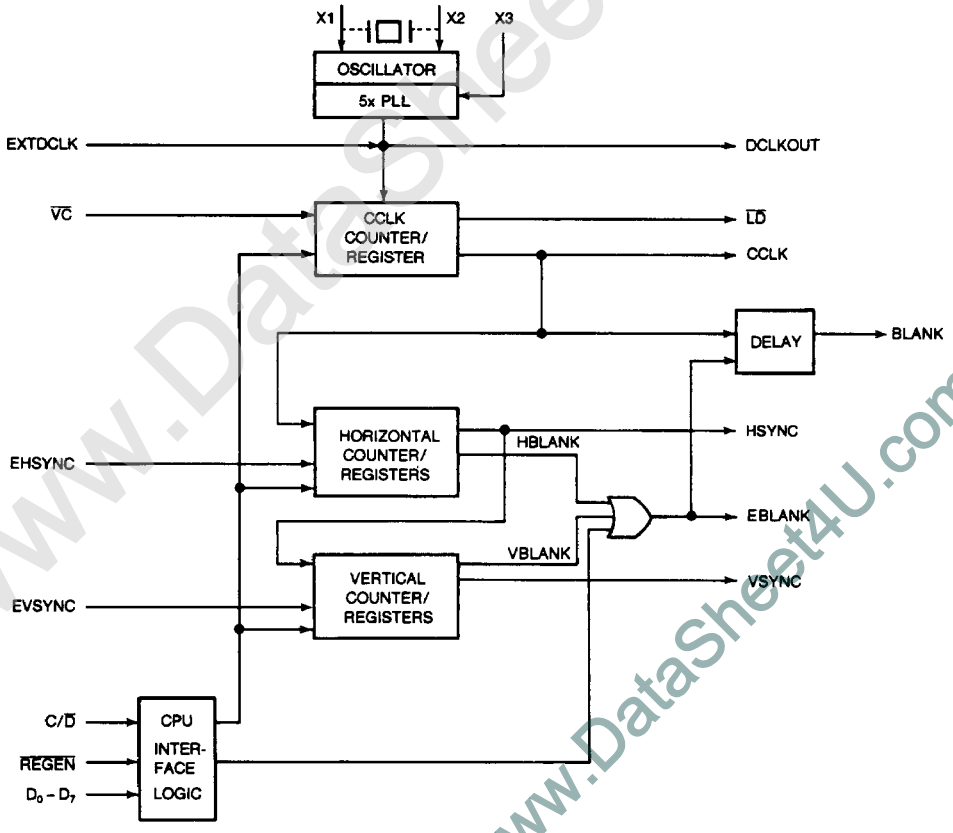
GENERAL DESCRIPTION

The Am8158 Video Timing Controller (VTC) is a fully programmable timing generator for bit-mapped graphics display systems. It generates the necessary timing signals for the remainder of the system and for the CRT monitor.

The Am8158 VTC is able to handle a Dot Clock rate of up to 125 MHz, allowing support of very high resolution displays such as 1K by 1K or more. The VTC can be synchronized to an external raster generator by using the external SYNC inputs.

The Am8158 VTC contains nine programmable registers which contain all the parameters necessary to define the raster.

BLOCK DIAGRAM



BD005054

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Issue Date: July 1987

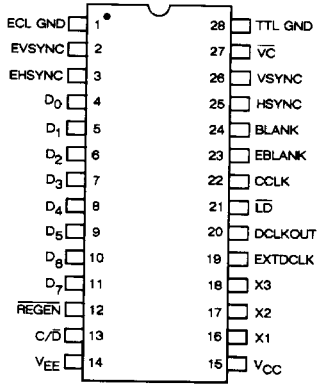
RELATED AMD PRODUCTS

Part No.	Description
Am8150	Display Refresh Controller
Am8151	Graphics Color Palette
Am8157	Video Shift Register
Am8177	Video Data Serializer

CONNECTION DIAGRAMS

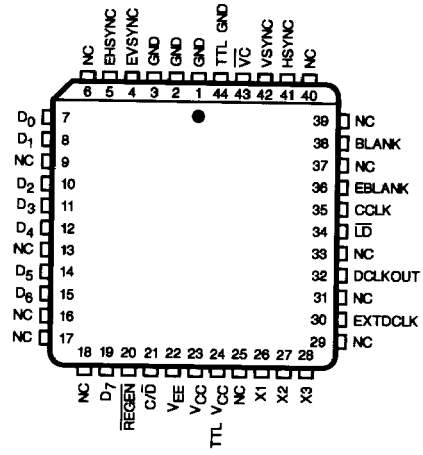
Top View

DIP



CD005741

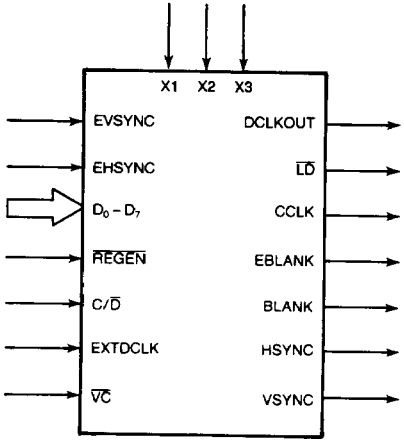
PLCC



CD009914

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



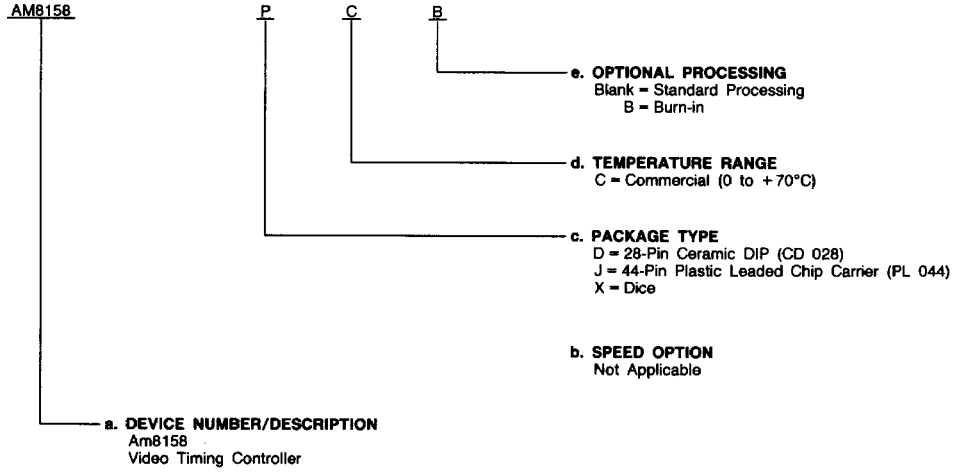
LS002150

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM8158	DC, DCB, JC, JCB, XC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

EXTDCLK External Dot Clock (Input, ECL)
If external times-1 clock mode is chosen, the externally generated ECL Dot Clock is applied to this pin. See the section on Dot Clock Generation. This input bypasses the crystal oscillator and the times-5 PLL multiplier.

X1, X2 Crystal Connects (X1 = Input, TTL)
X1 and X2 are used to connect a crystal for use with the on-chip oscillator. Alternatively, a TTL level clock can be applied to X1. See the section on Dot Clock Generation. The clock at X1 (or the crystal at X2/X1) is multiplied by 5 by an on-chip Phase Locked Loop (PLL) and is used as the Dot Clock. If a crystal is not used, X2 should remain open.

X3 Control Pin (Input, Non-TTL)
X3 is the control pin for the Voltage Controlled Oscillator (VCO). See the section on Dot Clock Generation.

DCLKOUT Dot Clock Out (Output, ECL)
This is the system Dot Clock. It is generated from the inputs at EXTDCLK or X1, X2, X3. See the section on Dot Clock Generation. All the timing in the chip is generated from this signal.

CCLK Character Clock (Output, TTL)
This is used to indicate when the next word must be read from the bit map. The dot clock is divided according to the contents of the CCKR register to generate this signal.

HSYNC Horizontal SYNC (Output, TTL)
This is the signal to the CRT monitor's horizontal electronics to begin horizontal retrace. The Am8158 initiates retrace on the LOW-to-HIGH transition of this signal.

VSYNC Vertical SYNC (Output, TTL)
This is the signal to the CRT monitor's vertical electronics to begin vertical retrace. The Am8158 initiates retrace on the LOW-to-HIGH transition of this signal.

EBLANK Early BLANK (Output, TTL)
Early Blank is the OR of the two internal signals, HBLANK and VBLANK.

BLANK BLANK (Output, ECL)
BLANK is a delayed and translated version of EBLANK. The leading edge of BLANK occurs two CCLK periods after the leading edge of EBLANK, while the trailing edge of BLANK is four CCLK periods after the trailing edge of EBLANK.

$\overline{VC}$ Video Cycle (Input, TTL)
$\overline{VC}$ is a signal which indicates that the current CCLK cycle is a video cycle and that a new word of video data will have to be loaded into the video shift register at the end of the cycle. If $\overline{VC}$ is made active during the current CCLK cycle, then $\overline{LD}$ will be made active at the DCLK period prior to the next rising edge of CCLK. If $\overline{VC}$ is always active, then $\overline{LD}$ will be made active at the DCLK period before every rising edge of CCLK.

$\overline{LD}$ Load (Output, ECL)
$\overline{LD}$ will be made active when $\overline{VC}$ is active. $\overline{LD}$ is used to load the video word into a shift register from the Am81XX Shifter Family. The duration of $\overline{LD}$ is always one DCLK period.

EHSYNC External Horizontal SYNC (Input, TTL)
This active HIGH signal may be used to synchronize the VTC to an external horizontal synchronization signal.

EVSYNC External Vertical SYNC (Input, TTL)
This active HIGH signal may be used to synchronize the VTC to an external vertical synchronization signal.

C/$\overline{D}$ Control/$\overline{Data}$ (Input, TTL)
During a register load operation, this pin is used to select between the control register and one of the data registers. A TTL HIGH selects the control register. A TTL LOW selects one of the data registers (the specific data register will be indicated by the contents of bits 3-0 of the control register).

$\overline{REGEN}$ Register Enable (Input, TTL)
$\overline{REGEN}$ is used to load data into the control register or one of the data registers. The data is latched into the register on the LOW-to-HIGH transition of $\overline{REGEN}$.

$D_0 - D_7$ $Data_0 - Data_7$ (Inputs (8), TTL)
These inputs are used to specify the data to be loaded into the appropriate register. D_7 is the Most Significant Bit (MSB).

FUNCTIONAL DESCRIPTION

Dot Clock Generation

The Am8158 allows the Dot Clock to be generated from three different sources. The first source is an on-chip oscillator with an external crystal. The second source is a TTL clock input, and the third source is an ECL clock input.

On-chip Oscillator: When an external crystal and the internal oscillator are used, a crystal is connected between the X1 and X2 inputs. The Dot Clock signal is generated at 5 times the crystal frequency using an internal Phase Locked Loop. In this configuration the X3 pin should be connected to a 0.47-μF capacitor to ground. The EXTDCLK input should be left open (see Figure 1-1).

External (times 5): When a TTL clock input is used the TTL signal should be connected to the X1 input. The Dot Clock signal is generated at 5 times the TTL clock frequency using an internal Phase Locked Loop. In this configuration the X2 pin should be left open and the X3 pin should be connected to a 0.47-μF capacitor to ground. The EXTDCLK input should be left open (see Figure 1-2).

External (times 1): When an ECL clock input is used the ECL signal should be connected to the EXTDCLK input. The Dot Clock signal is generated at this frequency without using the internal PLL. In this configuration the X1 and X3 pins should be connected to ground. The X2 pin should be left open (see Figure 1-3).

Mode	Input Pin Connections				DCLKOUT
	X1	X2	X3	EXTDCLK	
On-chip Oscillator	(Crystal) (n MHz)		0.47 μF Capacitor to GND	Open	5n MHz (ECL)
External (times 5)	TTL Clock (n MHz)	Open	0.47 μF Capacitor to GND	Open	5n MHz (ECL)
External (times 1)	GND	Open	GND	ECL Clock (n MHz)	n MHz (ECL)

Character Clock Timing Generation

The Character Clock output (CCLK) is generated by dividing the Dot Clock. The relative frequencies of DCLK and CCLK are determined by the CCKR data register. The number of DCLK cycles in a CCLK cycle is equal to (contents of the CCKR register + 2) times 2. CCLK is intended as a signal to start a RAM cycle to read out a pixel word. The length of a pixel word is equal to the number of DCLK cycles in a CCLK cycle.

The VTC Registers

The Am8158 contains nine write-only data registers, eight video registers, and one CCKR register. It also contains one write-only control register.

The control register is loaded by bringing $\overline{\text{REGEN}}$ LOW, and then HIGH again, while holding C/$\overline{\text{D}}$ HIGH.

A data register is selected by loading its address into bits 0-3 of the control register, and is loaded by bringing $\overline{\text{REGEN}}$ LOW, and then HIGH again, while holding C/$\overline{\text{D}}$ LOW. See Figure 3 for register addresses. register addresses.

CCKR Register

The CCKR register indicates the number of dot clocks in half a CCLK period. The number of dot clocks in a CCLK period is equal to (content of CCKR register + 2) times 2. A CCLK period is the period during which a pixel word is output from the memory. Register values of 0, 1, and 31 are not permitted.

Horizontal Sync Registers

The contents of the HSFE, HSRE, HBFE and HBRE registers are expressed in terms of CCLKs.

HSFE (Horizontal Sync Falling Edge) – This five-bit register contains the number of CCLKs within the active HSYNC pulse.

HSRE (Horizontal Sync Rising Edge) – This eight-bit register contains the number of CCLKs in the HSYNC period.

HBFE (Horizontal Blank Falling Edge) – This six-bit register contains the number of CCLKs from HSYNC rising edge to HBLANK falling edge.

HBRE (Horizontal Blank Rising Edge) – This eight-bit register contains the number of CCLKs from HSYNC rising edge to HBLANK rising edge.

Vertical Sync Registers

The contents of the VSFE, VSRE, VBFE, and VBRE registers are expressed in terms of HSYNC periods.

VSFE (Vertical Sync Falling Edge) – This six-bit register contains the number of HSYNC periods within the active VSYNC pulse.

VSRE (Vertical Sync Rising Edge) – This twelve-bit register contains the number of HSYNC periods in the VSYNC period.

VBFE (Vertical Blank Falling Edge) – This seven-bit register contains the number of HSYNC periods from VSYNC rising edge to VBLANK falling edge.

VBRE (Vertical Blank Rising Edge) – This twelve-bit register contains the number of HSYNC periods from VSYNC rising edge to VBLANK rising edge.

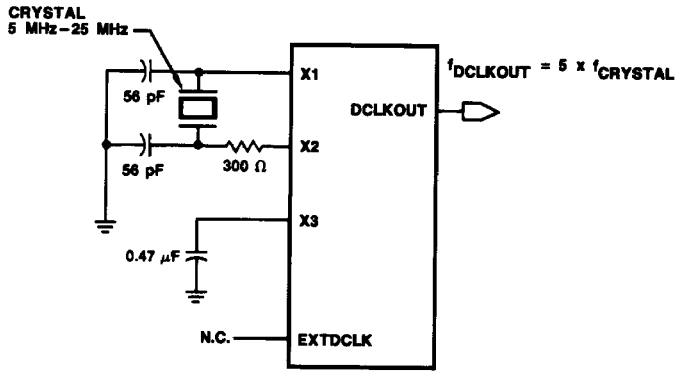


Figure 1-1. On-Chip Oscillator (with PLL)

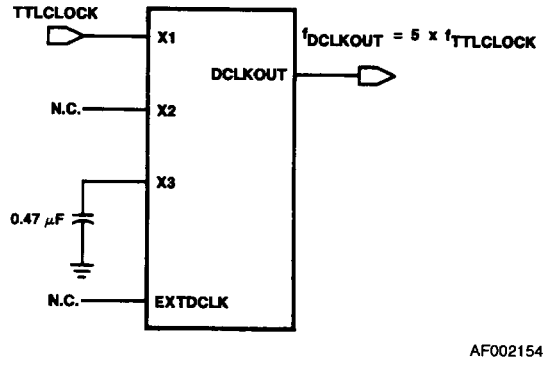


Figure 1-2. External (times 5) (with PLL)

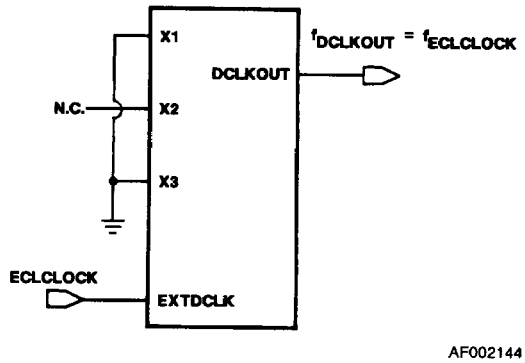


Figure 1-3. External (times 1) (without PLL)

Horizontal Timing Generation

Two signals are generated to control horizontal timing. These are HSYNC and HBLANK (which is used internally). Both of these signals are generated by counting CCLK. HSYNC is used to synchronize the monitor's horizontal sweep oscillator with the pixel data. HBLANK is used internally to generate EBLANK. HBLANK must be programmed to be a minimum of two CCLK cycles.

The Horizontal Timing Nomenclature (Figure 2) may be used as an aid to understanding the relationship between the register values and the actual timing. The top waveform conforms to RS-343A and shows composite video. The bottom traces show HBLANK and HSYNC. The top nomenclature items are the terms that monitor manufacturers often use:

MONITOR PARAMETERS		DESCRIPTION
HFP	Horizontal Front Porch	HBLANK↑ to HSYNC↑
HSYNC	Horizontal SYNC Width	HSYNC↑ to HSYNC↓
HBP	Horizontal Back Porch	HSYNC↓ to HBLANK↓
HAV	Horizontal Active Video	HBLANK↓ to HBLANK↑

The bottom nomenclature are the terms used for the Am8158 VTC. These names follow the register names.

REGISTER NAME		DESCRIPTION
HSFE	Horizontal Sync Falling Edge	HSYNC
HBFE	Horizontal Blank Falling Edge	HSYNC + HBP
HBRE	Horizontal Blank Rising Edge	HSYNC + HBP + HAV
HSRE	Horizontal Sync Rising Edge	HSYNC + HBP + HAV + HFP

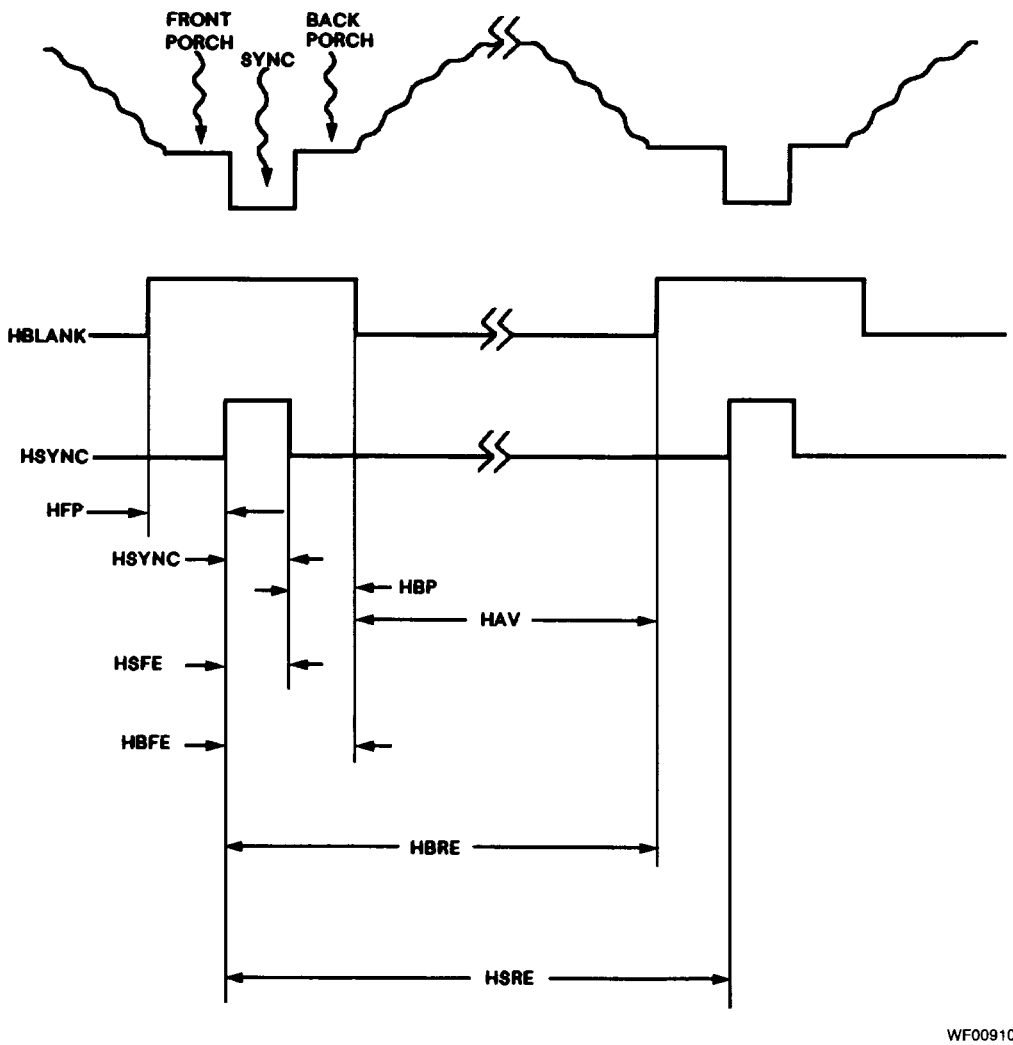


Figure 2. Horizontal Timing Nomenclature

Vertical Timing Generation

Two signals are generated to control vertical timing. These are VSYNC and VBLANK (which is used internally). Both of these signals are generated by counting HSYNC. VSYNC is used to synchronize the monitor's vertical sweep oscillator with the pixel data. VBLANK is used internally to generate EBLANK.

The Vertical Timing Nomenclature (Figure 3) may be used as an aid to understanding the relationship between the registers and the actual timing. The traces show VBLANK and VSYNC. The following nomenclature items are the terms that monitor manufacturers often use:

MONITOR PARAMETERS		DESCRIPTION
VFP	Vertical Front Porch	VBLANK↑ to VSYNC↑
VSYNC	Vertical SYNC width	VSYNC↑ to VSYNC↓
VBP	Vertical Back Porch	VSYNC↓ to VBLANK↓
VAV	Vertical Active Video	VBLANK↓ to VBLANK↑

The following nomenclature items are the terms used for the Am8158 VTC. These names follow the register names.

REGISTER NAME		DESCRIPTION
VSFE	Vertical Sync Falling Edge	VSYNC
VBFE	Vertical Blank Falling Edge	VSYNC + VBP
VBRE	Vertical Blank Rising Edge	VSYNC + VBP + VAV
VSRE	Vertical Sync Rising Edge	VSYNC + VBP + VAV + VFP

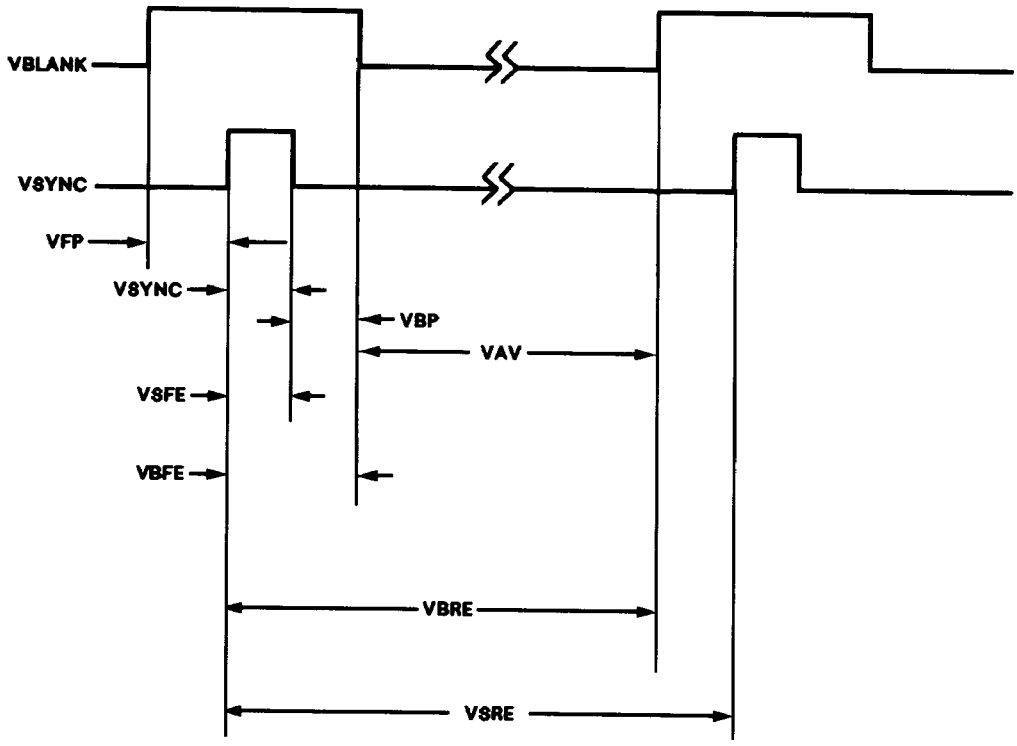


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Figure 3. Vertical Timing Nomenclature

CONTROL REGISTER DATA D_7 D_0	DATA REGISTER SELECTED	DATA REGISTER FORMAT D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 MSB LSB	NUMBER OF BITS ACCESSED IN DATA REGISTER
X X X X 0 0 0 0	CCKR		5
X X X X 0 0 0 1	HSRE		8
X X X X 0 0 1 0	HSFE		5
X X X X 0 0 1 1	HBRE		8
X X X X 0 1 0 0	HBFE		8
X X X X 0 1 0 1	VSREL	LOW	12
X X X X 0 1 1 0	VSREH	HIGH	
X X X X 0 1 1 1	VSFE		6
X X X X 1 0 0 0	VBREL	LOW	12
X X X X 1 0 0 1	VBREH	HIGH	
X X X X 1 0 1 0	VBFE		7
X X X X 1 0 1 1	RESET		
X X X X 1 1 0 0	RESERVED	NO EFFECT ON VTC WHEN ACCESSED	
X X X X 1 1 0 1	RESERVED		
X X X X 1 1 1 0	RESERVED		
X X X X 1 1 1 1	RESERVED		
X X X 1 X X X X	NONE	DISPLAY DISABLED (EBLANK HIGH)	

DON'T CARE BITS

TB095MMM

Figure 4. Register List

Blanking

The Am8158 supplies VSYNC and HSYNC signals to the system. HBLANK and VBLANK are internal to the VTC and are "ORed" internally to provide the EBLANK output. The VTC provides another blanking signal called BLANK which becomes active two CCLK cycles after the rising edge of EBLANK and inactive four CCLK cycles after the falling edge of EBLANK.

EBLANK is forced HIGH when bit four of the control register is set. This is a display disable bit and should be set while the CPU is initializing the VTC registers. This scheme prevents the CRT monitor from getting invalid video signals while register loading is in progress.

CPU Interface

Transactions between the CPU and the Am8158 VTC occur when the CPU is loading the VTC's timing registers. The Am8158 VTC must be programmed by the host to generate the desired timing. In order to load a register, the host must perform two write operations. The first write operation is directed to the control register (C/$\overline{D}$ HIGH) and specifies the address of the data register that is to be loaded. The second write operation is directed to the data register (C/$\overline{D}$ LOW) and specifies the data to be loaded into the register.

To program the Am8158, first write the value XXX1XXXX to the control register. This will force EBLANK active. Each register is then programmed with the appropriate value by writing its address to the control register and then writing the value to the data register. Each register is loaded by bringing $\overline{REGEN}$ LOW, and then HIGH again. Since the VBRE and VSRE registers are both twelve bits wide, they each require two load cycles. One load defines the least significant eight bits and the second load defines the most significant four bits.

When the VTC has been completely programmed, it may be reset (which does not change any of the register values) by writing XXXX1011 to the control register. Finally, bit four of the control register may be reset by writing zero to the control register, disabling EBLANK and BLANK.

External Sync Inputs

The Am8158 VTC can be synchronized to an external raster generator. This is useful for generating overlays.

The VTC detects an external horizontal sync by detecting the EHSYNC level on every LOW-to-HIGH transition on DCLK. The first DCLK to receive a valid EHSYNC HIGH will initiate the EHSYNC sequence. One DCLK period after detecting an external horizontal sync, the VTC will force CCLK LOW. Observe that the logic which uses CCLK must be able to handle a truncated CCLK. Four DCLK periods after detecting EHSYNC, CCLK will go HIGH and the Horizontal Counter will be reset. A reset Horizontal Counter corresponds to the start of horizontal sync and both HSYNC and EBLANK will go active.

The VTC detects an external vertical sync by detecting the EVSYNC level on every LOW-to-HIGH transition on DCLK. The first DCLK to receive a valid EVSYNC HIGH will initiate the EVSYNC sequence. When an external vertical sync is detected, the internal Vertical Counter corresponds to the start of vertical sync. On the next rising HSYNC edge following an external vertical sync, the VTC will set both VSYNC and EBLANK active.

Crystal Specification

The crystal used with the VTC may have the following specifications:

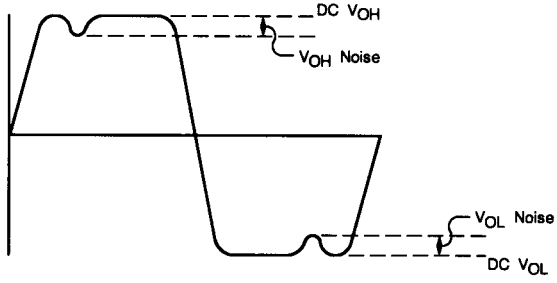
AT Cut
Series Resonant
Shunt Capacitance: 7 pF maximum

Simultaneous Switching Noise

Ceramic DIP parts, due to their longer lead frames, exhibit an internal ground noise which will modulate the ECL outputs. PLCC devices have much smaller lead frames and therefore show approximately 5 times less ground noise than Ceramic DIPs.

To minimize the ground noise on Ceramic DIPs, the best configuration is to terminate the output with 510 Ω to V_{EE} with minimum capacitive loading on the ECL outputs. Also, the grounding for the ECL ground pin must be optimum.

Under the above conditions, based on characterization with 7-pF capacitive loading, the worst-case noise seen on any ECL output (for the Ceramic DIP package) is shown below:



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DCLK Frequency	V_{OH} Noise	V_{OL} Noise
0 – 25 MHz	95 mV	100 mV
25 – 50 MHz	170 mV	170 mV
50 – 125 MHz	80 mV	100 mV

All noise spikes have a duration of no longer than 5 ns.

Phase Locked Loop Jitter

The Phase Locked Loop of the Am8158 is sensitive to noise generated inside the part due to input and output buffers switching. To minimize phase locked loop jitter, several steps may be taken. To reduce the noise due to the TTL outputs switching, the capacitive load on the output should be reduced and a series resistor added to minimize the current spike when the output switches (shown in Figure 5). To reduce the noise due to ECL outputs switching, the capacitive load on the outputs should be reduced (shown in Figure 6). To reduce the noise due to X_1 input switching when a TTL clock drives the Am8158, the circuit in Figure 7 should be used. The requirements for the signal at V_{IN} are also shown in Figure 7.

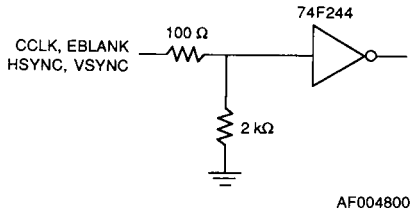


Figure 5. Noise Reduction, TTL Outputs

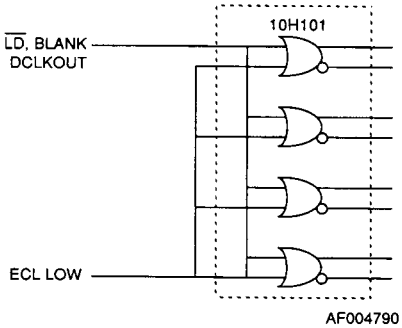
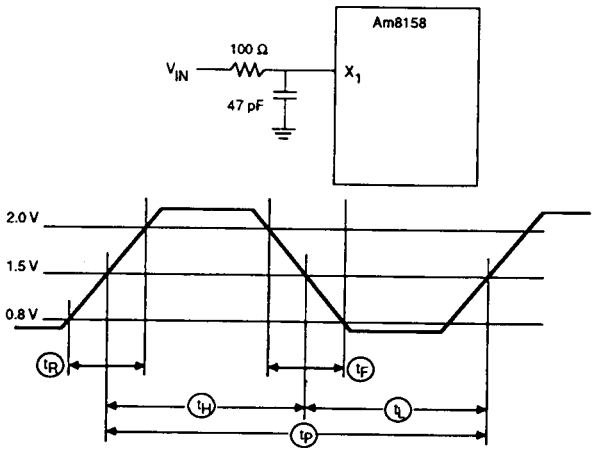


Figure 6. Noise Reduction, ECL Outputs



Parameter	Min.	Typ.	Max.	Unit
V_{IH}	2.4	3.3	V_{CC}	V
V_{IL}	−0.5	0.2	0.5	V
t_R, t_F	–	2.0	5.0	ns
t_P	40	–	200	ns
t_H	16	–	–	ns
t_L	16	–	–	ns
t_H, t_L	0.3	0.5	–	% of t_P

Figure 7. Noise Reduction, X_1 Input

APPLICATIONS

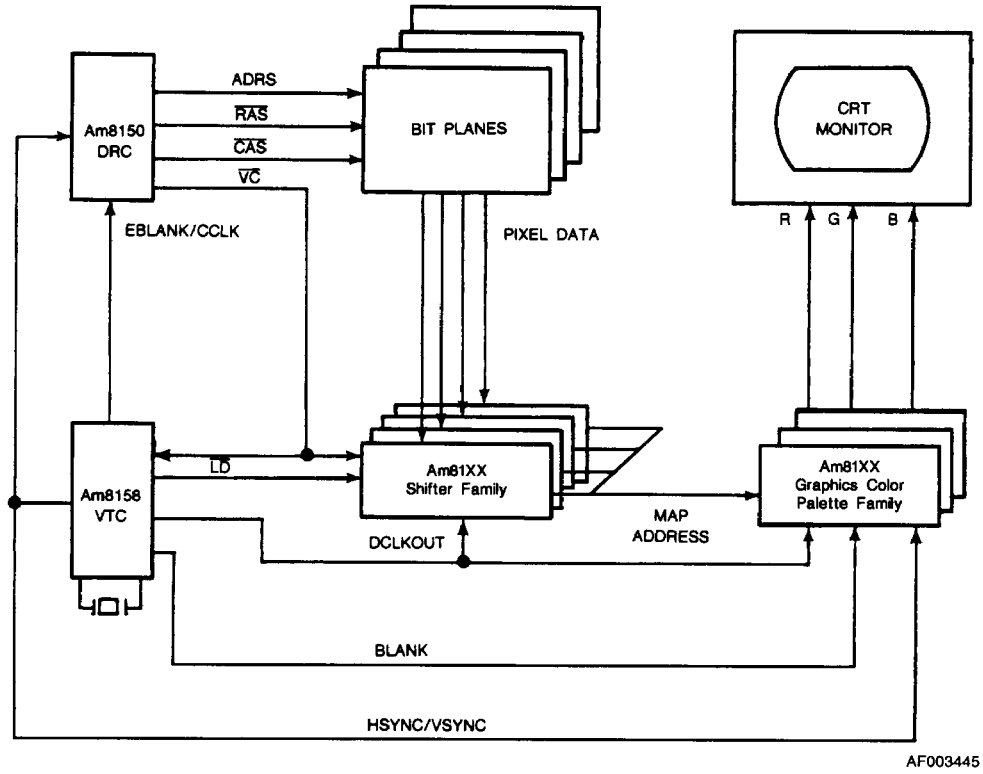


Figure 8. Typical Application

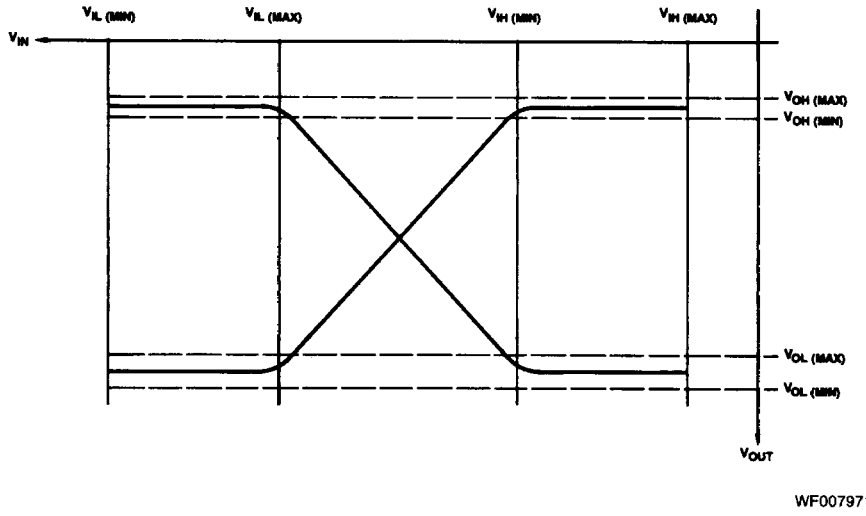


Figure 9. Am8158 ECL

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous (V_{CC}) ..... −0.5 to +7.0 V
Supply Voltage to Ground Potential
Continuous (V_{EE}) ..... +0.5 to −7.0 V
DC Voltage Applied to Outputs for
High Output State (TTL) ..... −0.5 V to +V_{CC} Max.
DC Input Voltage (TTL) ..... −0.5 to +7.0 V
DC Output Current, into Outputs (TTL) ..... 30 mA
DC Input Current (TTL) ..... −30 to +5.0 mA
DC Input Voltage (ECL) ..... +0.5 to V_{EE}
DC Output Current, into
Outputs (ECL) ..... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) (Note 2) ..... 0 to +70°C
Supply Voltage
Positive (V_{CC}) ..... +5 V ±5%
Negative (V_{EE}) ..... −5.2 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (TTL)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Max.	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., V_{IH} = 2.0 V I_{OH} = −1.0 mA, V_{IL} = 0.8 V	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. All I_{OL} = 16 mA		0.55	V
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage for All inputs	2.0		V
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage for All inputs		0.8	V
V_I	Input Clamp Voltage	V_{CC} = Max., I_I = −18 mA		−1.2	V
I_I	Input Current at Maximum Input Voltage, Except X1	V_{CC} = Max., V_I = 5.5 V		1.0	mA
I_{IH}	Input HIGH Current, All TTL Inputs Except X1	V_{CC} = Max., V_{IH} = 2.4 V		100	μA
I_{IHX1}	Input HIGH Current, X1	V_{CC} = Max., V_{IH} = 2.4 V		200	μA
I_{IL}	Input LOW Currents, Inputs $D_0 - D_4$, EVSYNC	V_{CC} = Max., V_{IL} = 0.4 V		−750	μA
I_{IL}	Input LOW Current, Any Other TTL Input	V_{CC} = Max., V_{IL} = 0.4 V		−550	μA
I_{SC}	Output Short-Circuit Current (Note 1)	V_{CC} = Max.	−15	−100	mA
I_{CC}	TTL Supply Current	V_{CC} = Max.; Outputs Open		300	mA
I_{EE}	ECL Supply Current	V_{EE} = Max.; Outputs Open		80	mA

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
2. A combination of skewing the limits and adjusting the pulse test ambient temperature is used to ensure that the data sheet steady state limits are met at the temperatures specified.
3. Guaranteed with transverse air flow exceeding 500 linear F.P.M. and two minute warm-up period. Typical thermal resistance values of the package are:

	Ceramic DIP	PLCC
θ_{JA} Junction-to-Ambient (still air) °C/Watt	30	35
θ_{JA} Juntion-to-Ambient (at 500 F.P.M. air flow) °C/Watt	19	
θ_{JA} Juntion-to-Case °C/Watt	19	
Equivalent Gate Count	313	
Die Size	.189" x .199"	

DC CHARACTERISTICS over operating range (ECL)

Parameters	Test Conditions	0°C	25°C	70°C	Unit
V_{OH} (Max.)	50 Ω to −2 V	−840	−810	−730	mV
V_{OH} (Min.)		−1000	−960	−910	mV
V_{OL} (Max.)	50 Ω to −2 V	−1665	−1650	−1630	mV
V_{OL} (Min.)		−1870	−1850	−1835	mV
V_{IH} (Max.)	V_{CC} = Max.	−840	−810	−730	mV
V_{IH} (Min.)	V_{EE} = Min.	−1145	−1105	−1055	mV
V_{IL} (Max.)	V_{CC} = Max.	−1490	−1475	−1455	mV
V_{IL} (Min.)	V_{EE} = Min.	−1870	−1850	−1835	mV
I_{IH}	V_{EE} = Max. V_{IN} = V_{IH} (Max.)	200	200	200	μA
I_{IL}	V_{EE} = Max. V_{IN} = V_{IH} (Min.)	150	150	150	μA

SWITCHING CHARACTERISTICS over operating range

Number	Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	t_{CLK}	EXTDCLK PERIOD (PLL disabled) (Note 7)	8		ns
2	t_{SKEW}	DCLKOUT ↑ TO CCLK ↑		12	ns
	t_{SKEW}	DCLKOUT ↑ TO CCLK ↓		12	ns
3	t_S	C/$\overline{D}$ VALID TO $\overline{REGEN}$ ↓	15		ns
4	t_H	$\overline{REGEN}$ ↑ TO C/$\overline{D}$	10		ns
5	t_S	DATA VALID TO $\overline{REGEN}$ ↑	15		ns
6	t_{PW}	$\overline{REGEN}$ PULSE WIDTH	40		ns
7	t_H	$\overline{REGEN}$ ↑ TO DATA	15		ns
8	t_{SKEW}	CCLK ↑ TO EBLANK ↑		25	ns
	t_{SKEW}	CCLK ↑ TO EBLANK ↓		25	ns
9	t_{SKEW}	CCLK ↑ TO HSYNC ↑		25	ns
	t_{SKEW}	CCLK ↑ TO HSYNC ↓		25	ns
10	t_{PLH}	EXTDCLK ↓ TO DCLKOUT ↑	0	8	ns
	t_{PHL}	EXTDCLK ↓ TO DCLKOUT ↓	0	8	ns
11	t_{SKEW}	HSYNC ↑ TO VSYNC ↑	2	2	CCLK
	t_{SKEW}	HSYNC ↑ TO VSYNC ↓	2	2	CCLK
12	t_{SKEW}	CCLK ↑ TO BLANK ↑		6	ns
	t_{SKEW}	CCLK ↑ TO BLANK ↓		6	ns
13	t_{SKEW}	EBLANK ↑ TO BLANK ↑	2	2	CCLK
	t_{SKEW}	EBLANK ↓ TO BLANK ↓	4	4	CCLK
14	t_S	$\overline{VC}$ ↓ TO CCLK ↑	2	2	DCLK
15	t_S	$\overline{VC}$ ↑ TO CCLK ↑	15		ns
16	t_S	EHSYNC ↑ TO DCLKOUT ↑ (Note 5)	8		ns
17	t_H	DCLKOUT ↑ TO EHSYNC ↓ (Note 5)	4		ns
18	t_{SKEW}	HSYNC ↑ TO EBLANK ↑ (Note 4)		8	ns
19	t_{SKEW}	DCLKOUT ↑ TO CCLK ↓ (Note 6)		15	ns
20	t_S	EVSYNC ↑ TO DCLKOUT ↑ (Note 5)	8		ns
21	t_H	DCLKOUT ↑ TO EVSYNC ↓ (Note 5)	4		ns
22	t_S	HSYNC ↑ TO EVSYNC ↑	2	2	CCLK
23	t_{CLK}	CLOCK PERIOD AT X1 (TTL) (Note 7)	40		ns
24	t_{CLK}	CLOCK PERIOD AT X1, X2 (CRYSTAL) (Note 7)	40		ns
25	t_{CLK}	DCLKOUT PERIOD (with PLL) (Note 7)	8	40	ns

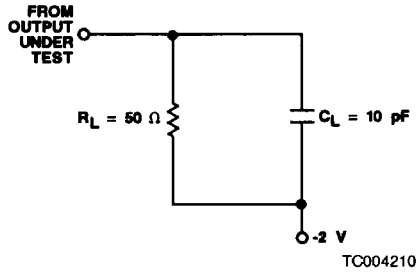
Table continued on following page.

SWITCHING CHARACTERISTICS (Cont'd.)

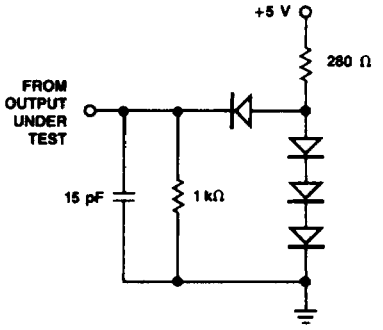
Number	Parameter Symbol	Parameter Description	0°C		25°C		70°C		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
26	t_{SKEW}	DCLKOUT ↑ to $\overline{LD}$ ↑ (Note 7)	1.7	5.5	1.8	5.5	2.4	6.4	ns
	t_{SKEW}	DCLKOUT ↑ to $\overline{LD}$ ↓ (Note 7)	1.0	5.4	1.2	5.7	1.3	6.2	ns
27	t_{SKEW}	DCLKOUT ↑ to BLANK ↑ (Note 7)	2.8	5.8	2.9	5.9	3.0	6.3	ns
	t_{SKEW}	DCLKOUT ↑ to BLANK ↓ (Note 7)	2.2	5.3	2.4	5.3	2.8	5.9	ns

Notes: 4. When EHSYNC occurs before EBLANK is active.
5. Setup and hold times for guaranteed response to EHSYN or EVSYNC within that DCLK cycle.
6. Applicable only during external horizontal synchronization
7. These parameters are guaranteed by device characterization or tested using bench-top equipment.

SWITCHING TEST CIRCUITS



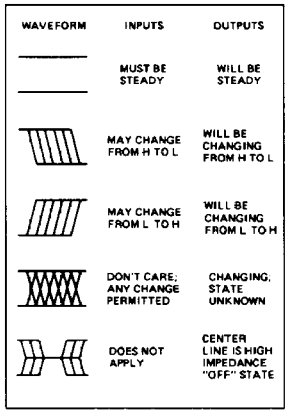
A. ECL Test Load



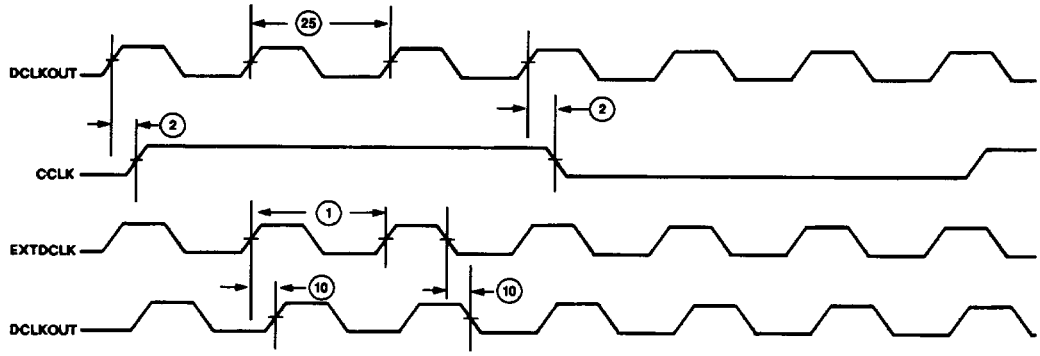
B. TTL Test Load

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

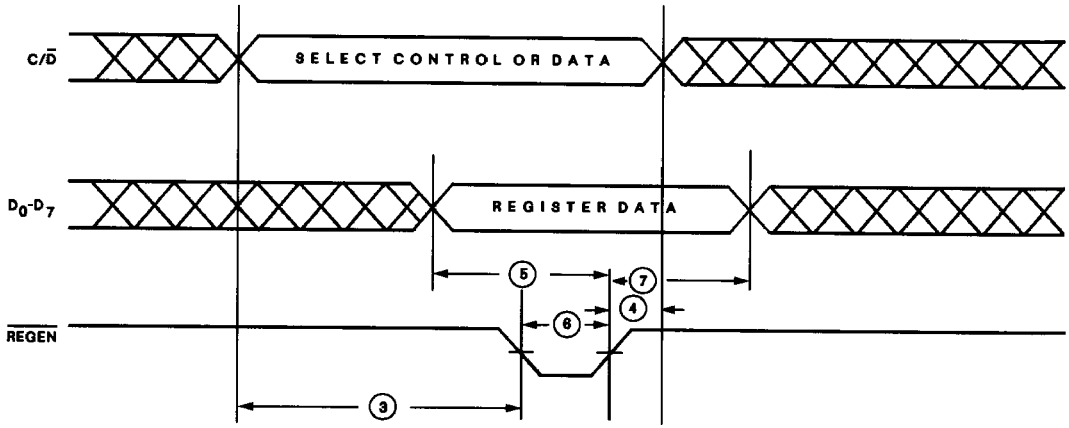


SWITCHING WAVEFORMS (Cont'd.)



WF009124

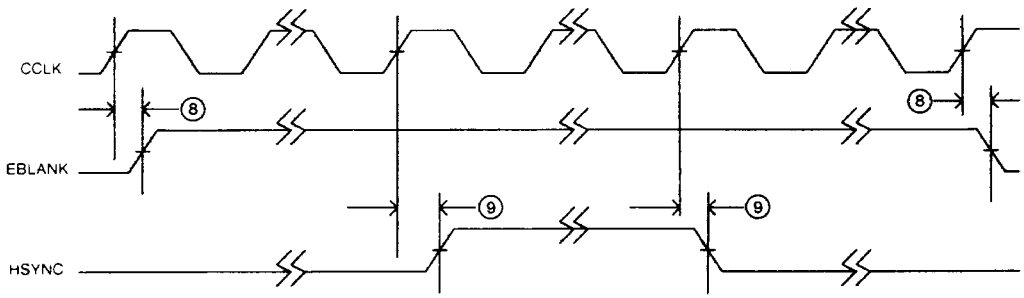
CCLK Timing



WF009131

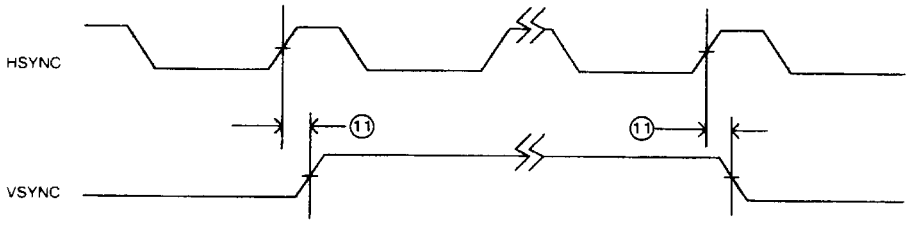
CPU Interface Timing

SWITCHING WAVEFORMS (Cont'd.)



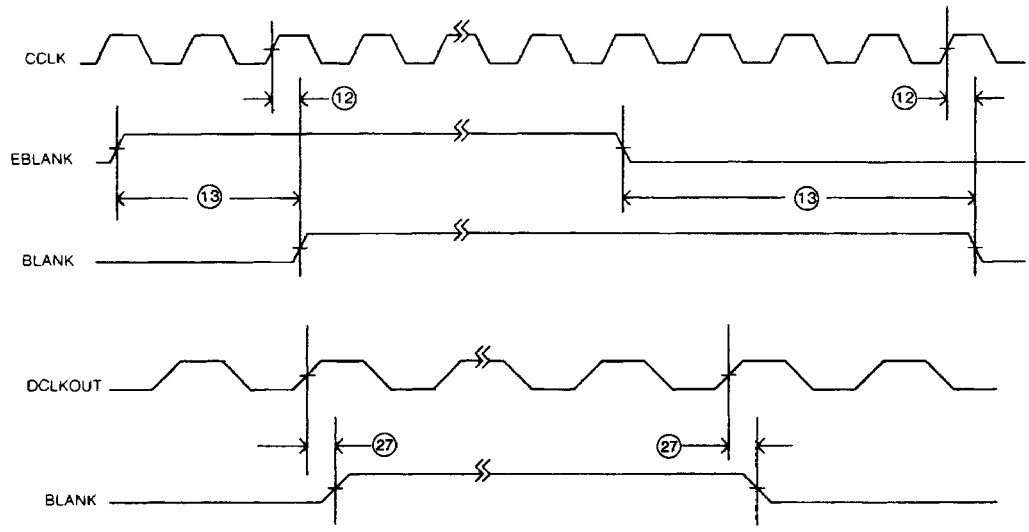
WF024340

Horizontal Sync Timing



WF024351

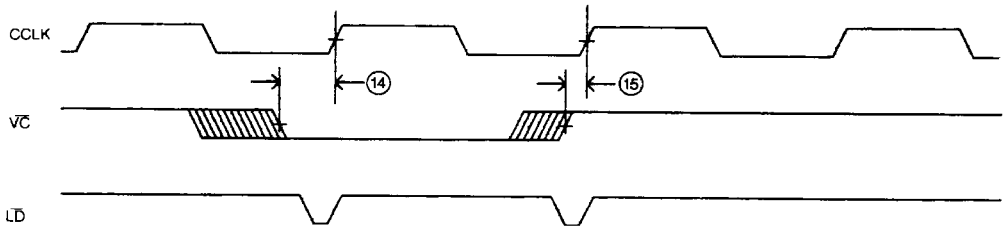
Vertical Sync Timing



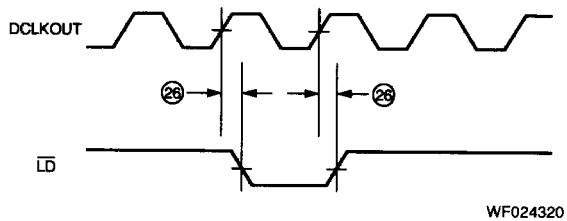
WF024361

Video Blanking Timing

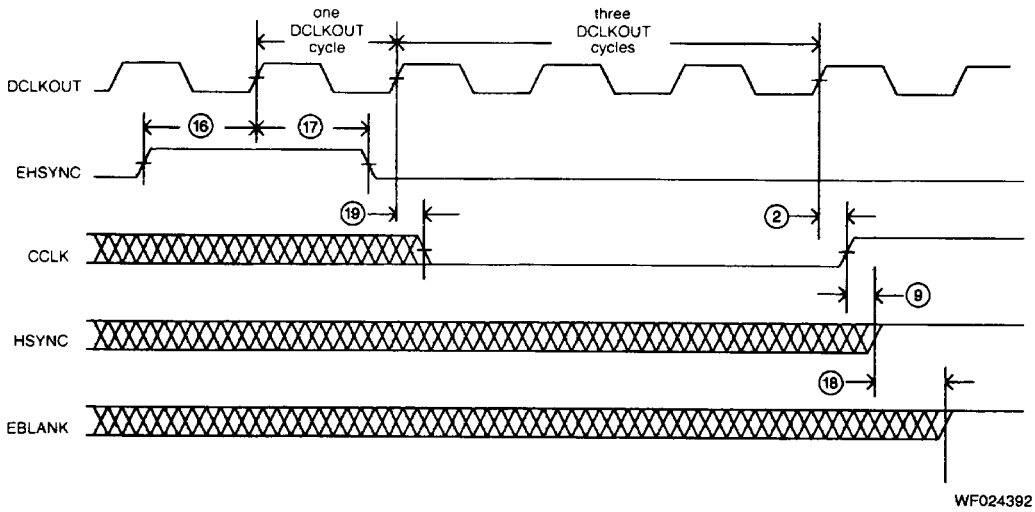
SWITCHING WAVEFORMS (Cont'd.)



LD Output
(VC Comes From an External Source)

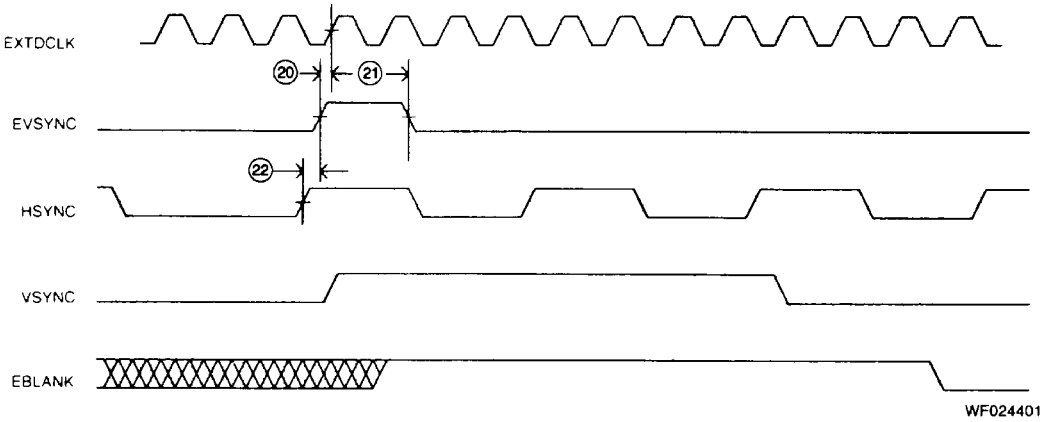


LD Output Timing
(With VC Tied Low)

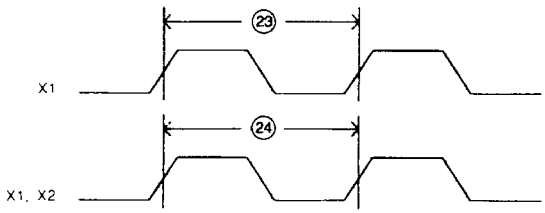


External HSYNC

SWITCHING WAVEFORMS (Cont'd.)



External VSYNC

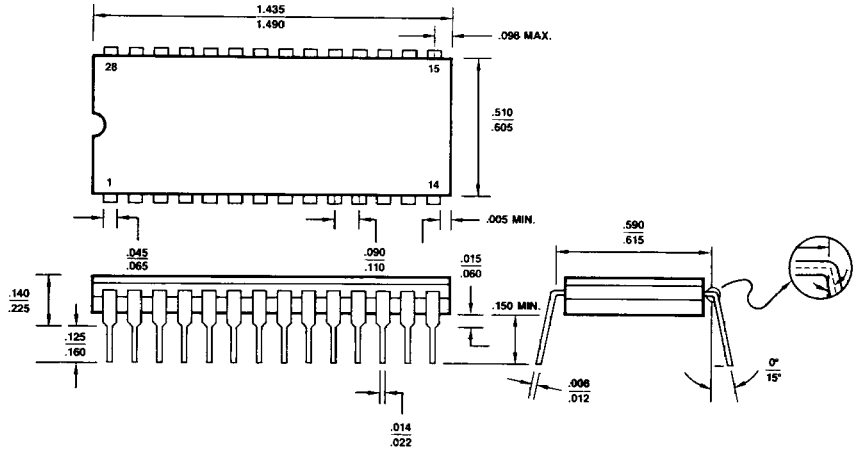


WF024411

X1, X2 Timing

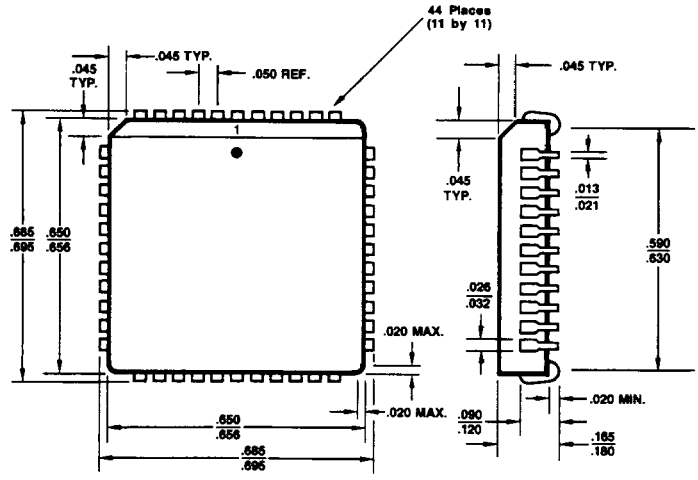
PHYSICAL DIMENSIONS*

CD 028



PID # 06837A

PL 044



PID # 06752B

*For reference only.

ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450

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