Am9064

65,536 x 1 Dynamic RAM

DISTINCTIVE CHARACTERISTICS

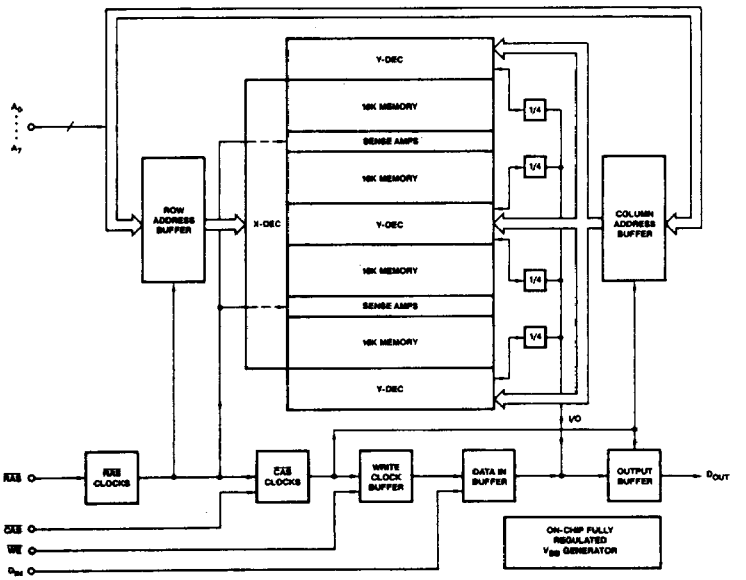
- High speed $\overline{RAS}$ access of 100 and 120ns
- Single +5V ±10% power supply
- Low power 22mW standby
  - 330mW active — 220ns cycle time
  - 385mW active — 190ns cycle time
- Read, Write, Read-Modify-Write, Page-Mode and $\overline{RAS}$-Only refresh capability
- $\overline{CAS}$ controlled three-state output
- Fast cycle times of 190 and 220ns

GENERAL DESCRIPTION

The Am9064 is a high speed, high-performance dynamic RAM, organized 65,536 x 1 and manufactured using advanced NMOS silicon-gate technology. The design is optimized for both high speed and low power dissipation, and only a single +5V supply is needed because the on-chip substrate-bias generator (compensated for temperature and supply variations) provides the necessary back bias.

The Am9064 features multiplexed addressing, and all input signals, including clocks, are TTL-compatible; input and output signals are the same polarity, and the three-state output buffer is $\overline{CAS}$ controlled. The Hi-C single-transistor memory cell is used to enhance signal margin and reduce the α-particle-induced soft-error rate.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Part Number	Am9064-10	Am9064-12	Am9064-15
$\overline{RAS}$ Access Time	100	120	150
$\overline{CAS}$ Access Time	55	65	75

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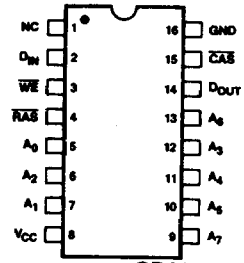
CONNECTION DIAGRAM
TOP VIEW



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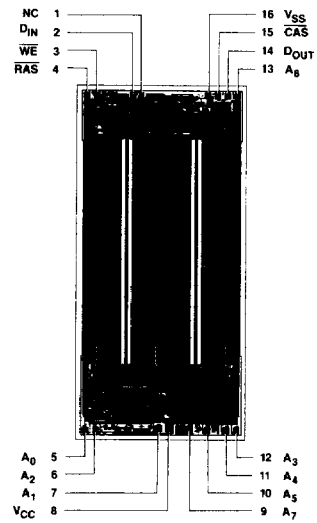
Note: Pin 1 is marked for orientation

Metallization and Pad Layout



Die Size
(Incl. Strip-Chip)
145 Mils x 313 Mils

ORDERING INFORMATION

Am9064-10 P C

- C — Temperature
  - C – Commercial (0°C to +70°C)
- P — Package
  - D – 16-pin CERDIP
  - P – 16-pin plastic
- 10 — Speed Select
  - 10 – 100ns
  - 12 – 120ns
  - 15 – 150ns
- Am9064 — Device Type
  - 64k x 1 DRAM

Valid Combinations	
Am9064-10 Am9064-12 Am9064-15	PC, DC

PIN DESCRIPTION

$A_0 - A_7$ Eight multiplexed inputs, first provide eight row address inputs and then eight column address inputs, all within one normal memory cycle. The eight row address inputs (meeting the setup and hold times t_{ASR} and t_{RAH}) are latched in by $\overline{RAS}\downarrow$. The eight column address inputs, (meeting the setup and hold times t_{ASC}, t_{CAH} and t_{AR} are latched in by $\overline{CAS}\downarrow$. The combined row and column address inputs (16 total) will select one of 65,536 memory bits for Read, Write, or Read-Modify-Write operation. In addition, the memory refresh function is also performed in any memory cycle (including $\overline{RAS}$ only refresh cycle), on two of 256 rows specified by $A_0 - A_6$, while A_7 is not used. Page-mode cycles excluded.)

D_{IN} The Data Input. The data input, (meeting setup and hold times t_{DS}, t_{DH} and t_{DHR}) is latched in by either $\overline{WE}\downarrow$ or $\overline{CAS}\downarrow$ whichever comes later, while $\overline{RAS}$ is LOW.

$\overline{RAS}$ The Row-Address-Strobe control clock. $\overline{RAS}\downarrow$ latches the row address on $A_0 - A_7$ and activates a memory cycle. $\overline{RAS}\uparrow$ ends the active memory cycle and precharges the memory's dynamic circuits. Memory cycle time, as defined by the $\overline{RAS}$ clock, has a very large operating range; however $\overline{RAS}$ LOW pulse width (t_{RAS}) and $\overline{RAS}$ HIGH pulse width (t_{RP} must satisfy the specified minimum and maximum values in order to maintain continuous memory operation and data retention. $\overline{RAS}$ alone controls memory refresh function.

$\overline{CAS}$ The Column-Address-Strobe control clock. With $\overline{RAS}$ LOW, $\overline{CAS}\downarrow$ latches the column address and activates the memory input and output operations. With $\overline{WE}$ LOW, $\overline{CAS}$ controls the input timing; with $\overline{WE}$ HIGH, $\overline{CAS}$ controls the timing of valid output. $\overline{CAS}$ HIGH turns off D_{OUT} (D_{OUT} = high impedance). In page-mode, $\overline{CAS}$ cycle time defines the page-mode cycle time.

$\overline{WE}$ The Write Enable Control Clock. $\overline{WE}$ timing relative to $\overline{CAS}$ and $\overline{RAS}$ will define one of three memory cycles. 1) $\overline{RAS}$ and $\overline{CAS}$ both LOW, and $\overline{WE}$ HIGH will define a read cycle; 2) $\overline{WE}$ LOW (meeting the setup and hold times t_{WCS}, t_{WCH} and t_{WCR}) will define an Early Write Cycle; 3) $\overline{WE}$ first HIGH and then LOW (meeting t_{CWD} and t_{RWD} delay times) will define a Read-Write/Read-Modify-Write Cycle.

D_{OUT} The three-state output. The D_{OUT} is controlled mainly by $\overline{CAS}$. Valid output appears on D_{OUT} in a Read Cycle after access time has elapsed (t_{CAC} or t_{RAC}, whichever applies). Last valid D_{OUT} remains valid as long as $\overline{CAS}$ is LOW. D_{OUT} can be turned off only with $\overline{CAS}\uparrow$.

APPLICATION INFORMATION

DEVICE DESCRIPTION

The Am9064 is a state-of-the-art high performance 64K DRAM combining the fastest DRAM speed available (100ns access time) with low power (standby current < 4mA). It is designed to operate with a single +5V power supply, and all inputs/output voltage levels are TTL compatible, making the Am9064 easy to integrate into a wide range of systems. The Am9064 is offered in two grades of operating ambient temperature range, the commercial grade (Am9064-12DC) covers from 0 to +70°C and the extended grade (Am9064-12CDC) covers from −55 to +110°C military applications. Where the memory system reliability is of primary importance, the Am9064 design provides the solution with the following safety features:

The Am9064:

- Allows V_{CC} power-up with floating input levels without causing excess I_{CC} current surges (see Initialization).

Can tolerate real time V_{CC} fluctuation between 4.5 and 5.5V while memory chip is in operation.

- Accepts input voltage transition overshoot (V_{CC} +1V) and undershoot (−2V).
- Is fabricated with an NMOS technology that is optimized to provide very high 64K DRAM device latch-up voltage, typically in excess of 10V; (however, it is not recommended to operate Am9064 with V_{CC} over +7V; see Maximum Ratings).

The fast switching characteristics of the Am9064 are designed to fit into memory system constraints. For a fast Read Cycle, Am9064 offers fast t_{CAC} (about 50 to 55% of t_{RAC}), thus providing 45 to 50% of t_{RAC} access time for address multiplexing on a memory board. For a Write operation, fast t_{RWL} and t_{CWL} allow fast Read-Write or Read-Modify-Write cycles, useful for memory systems which include Error Detection/Correction (EDC) schemes to boost memory reliability. (For a detailed reference on EDC, see "Am2960 Series Dynamic Memory Support Handbook," AMD Application.)

The Am9064 includes all standard 64K DRAM memory cycles: Read, Early Write (for the case of common I/O), Read-Write or Read-Modify-Write, $\overline{RAS}$-Only Refresh, and Page-Mode cycles. Two clock inputs ($\overline{RAS}$ and $\overline{CAS}$) are needed to latch the multiplexed row and column addresses on the eight address inputs, $A_0 - A_7$, and a third clock input ($\overline{WE}$) distinguishes between Read and Write cycles. Proper input or output operation on each memory bit requires all three timing control clocks ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$). Memory refresh operation is most efficient through the $\overline{RAS}$-Only Refresh Cycle when using a dynamic RAM controller like Am2964B. The Am9064 accomplishes 128 refresh cycles ($A_0 - A_6$) in 2ms and 256 refresh cycles ($A_0 - A_7$) in 4ms. Multiplexed address inputs allow the Am9064 to be packaged in a standard 16-pin DIP with pin 1 not connected. With pin 1 uncommitted, the Am9064 is compatible with the JEDEC standards for the 64K DRAM and allows for future expansion to 256K DRAM.

DEVICE INITIALIZATION

An initial pause of 100μs is required after V_{CC} power-up. This time delay is needed for the on-chip substrate-bias generator to pump enough negative charge into the substrate to establish the operating back bias voltage. This is followed by a wake-up sequence of eight (8) $\overline{RAS}$ cycles to initialize the internal dynamic circuits. If the device remains in standby

mode for more than 2ms while V_{CC} is on, the wake-up sequence of any eight $\overline{RAS}$ cycles will be necessary prior to normal operation. A power-up safety feature has been designed into the Am9064; special circuits within the chip prevent current surges during initial system power-up. These circuits allow the Am9064 to be powered up to a standby mode (where current is low and output is in high impedance) independent of the initial $\overline{RAS}$ input logic level. (See Figures 1 and 2). The power-up circuit is completely transparent to normal circuit operation.

Figure 1. V_{CC} Supply Current Waveform during V_{CC} Power up, $\overline{RAS} = \overline{CAS} = V_{CC}$

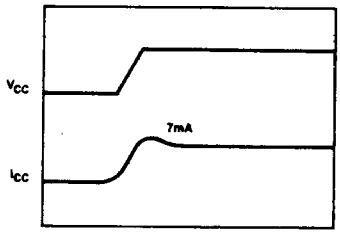


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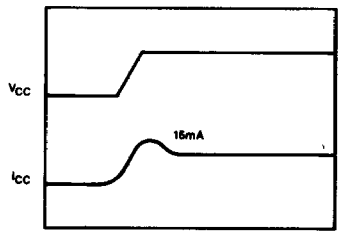
Figure 2. V_{CC} Supply Current Waveform during V_{CC} Power Up, $\overline{RAS} = \overline{CAS} = V_{SS}$



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ADDRESSING

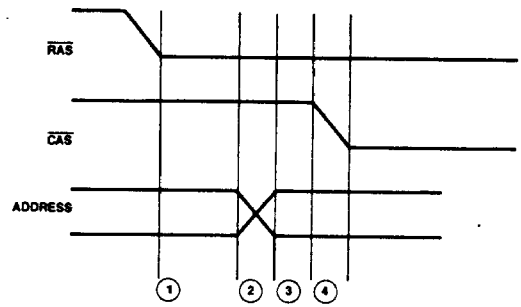
Eight address inputs are multiplexed to provide 16 address bits. The first set of eight address inputs (Row address) is latched by $\overline{RAS}$, and the second set (Column address) is latched by $\overline{CAS}$. Together, the 16 address bits will decode one of 65,536 cell locations.

Proper address multiplexing requires that $\overline{CAS}$ follow $\overline{RAS}$ by a specified delay time (t_{RCD}). Minimum t_{RCD} is determined by the following equation:

t_{RCD} (min) = $t_{RAH} + 2t_T + t_{ASC}$ where t_{RAH} and t_{ASC} are specified DRAM characteristics, and $2t_T$ are the address and $\overline{CAS}$ transition times, dependent on the memory board design. The maximum t_{RCD} is derived from the access time limits.

t_{RCD} (max) = $t_{RAC} - t_{CAC}$. If t_{RCD} (max) is exceeded, the access time will be determined by t_{CAC}. The multiplex timing window of interest for system design is t_{RCD} (max) — t_{RAH} (see Figure 3).

Figure 3. Address Multiplex Timing Window t_{RCD} (Max) - $t_{RAH} \geq 2$ (t_T + Skew) + t_{ASC}



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① t_{RAH}
② t_T + skew (address input A_0-A_7 relative to $\overline{RAS}$)
③ t_{ASC}
④ t_T + skew ($\overline{CAS}$ relative to $\overline{RAS}$)

OPERATING CYCLES

READ CYCLE

The Memory Read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from HIGH to LOW. The $\overline{CAS}$ clock must also make a transition from HIGH to LOW at the specified t_{RCD} timing limits when the column addresses are latched. These clocks are linked in such a manner that the access time of the device is independent of the address multiplex window, however the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum for an access (data valid) from the $\overline{RAS}$ clock edge to be valid (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as shown in the functional block diagram. This gating feature on the $\overline{CAS}$ clock allows the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and thus defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses to generate the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for certain minimums (t_{RAS} for the $\overline{RAS}$ clock; t_{CAS} for the $\overline{CAS}$ clock) and the $\overline{RAS}$ clock must stay inactive for a minimum time (t_{RP}). The former is for the completion of the cycle in progress and the latter allows the device internal circuitry to be precharged for the next active cycle.

D_{OUT} is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the high impedance mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10ns (t_{CRP}) into the next cycle. To perform a Read Cycle, the Write Enable ($\overline{WE}$) input must be held HIGH from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive mode (t_{RCH}).

WRITE CYCLE

A Write Cycle is similar to a Read Cycle except that the Write Enable ($\overline{WE}$) clock must go active LOW at or before the time that the $\overline{CAS}$ clock goes active. In this case the cycle in progress is referred to as an early Write Cycle. In an early Write Cycle, the Write Clock and D_{IN} are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the Write Cycle: the

column-strobe-to-write lead time (t_{CWL}) and the row-strobe-to-write lead time (t_{RWL}). These are the minimum times that the $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{WE}$ clock LOW).

It is also possible to perform a late Write Cycle. For this cycle, the Write Clock is activated after $\overline{CAS}$ goes LOW, which is beyond t_{WCS} minimum time so the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early Write Cycle and a late Write Cycle is that in a late Write Cycle the Write Enable clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — ($t_{RWL} + t_{RP} + 2t_T$).

At the start of a Write Cycle. D_{OUT} is in a Hi-Z condition and remains so throughout the cycle. It remains Hi-Z because the active transition of the Write Enable clock prevents the $\overline{CAS}$ clock from enabling the output buffers, as shown in the Functional Block Diagram. This characteristic can be effectively utilized in a system that has a common input/output bus, with the only stipulation being the system must use only the early write mode.

READ-MODIFY-WRITE AND READ-WRITE CYCLES

As the name implies, both a Read and a Write Cycle are accomplished at the same cell location during a single access. The Read-Modify-Write Cycle is similar to the late Write Cycle discussed above.

For the Read-Modify-Write Cycle, a normal Read Cycle is initiated with the $\overline{WE}$ clock HIGH. After the data is read, $\overline{WE}$ is transitioned to LOW and D_{IN} is setup and held with respect to the active edge of $\overline{WE}$. This cycle assumes a zero modify time between read and write.

Another variation of the Read-Modify-Write Cycle is the Read-Write Cycle, in which the two parameters, t_{RWD} and t_{CWD} play an important role. A Read-Write Cycle starts as a normal Read Cycle with the $\overline{WE}$ clock being transitioned at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before D_{OUT} occurs. In this case, D_{IN} is set up with respect to the $\overline{WE}$ clock active edge.

PAGE-MODE CYCLES

Page-mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) on the Am9064 is typically half the regular $\overline{RAS}$ clock access (t_{RAC}). Page-mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit address field. There are two controlling factors which serve to limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on-time limits the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal Read or Write cycle, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time, (t_{CAS}) the $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to Read and Write cycles, a Read-Modify-Write Cycle can also be performed in a page-mode operation. For a Read-Modify-Write or Read-Write type cycle, the conditions normal to that mode of operation will apply in the page-mode also. Any combination of Read, Write and Read-Modify-Write cycles can be performed to suit any particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature; therefore, to retain the correct information, the bits need to be refreshed at least once every 2ms. This is accomplished by sequentially cycling through the 128 row address locations every 2ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with the particular row decoded.

$\overline{RAS}$-Only Refresh

When the memory component is in standby, the $\overline{RAS}$-Only Refresh scheme is employed. This refresh method performs a $\overline{RAS}$-Only cycle on all 128 row addresses every 2ms; the row addresses are latched with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. The $\overline{CAS}$ clock is not required and should be inactive, or HIGH, to conserve power.

DATA OUTPUT OPERATION

The Am9064 has a $\overline{CAS}$ controlled three-state data output (D_{OUT}) which remains valid from the access time as long as $\overline{CAS}$ is LOW. d_{OUT} can be turned off to the high impedance state only when $\overline{CAS}$ is HIGH, and remains in Hi-Z as long as $\overline{CAS}$ stays HIGH. The output data is the same polarity as the input data. The following table summarizes the D_{OUT} state for various cycles.

Type of Cycle		D_{OUT}
Read Cycle		Data from Addressed Memory Cell
Early Write Cycle		Hi-Z
Delayed Write Cycle		Indeterminate, until after t_{RAC} and t_{CAC}
$\overline{RAS}$ Refresh Cycles	$\overline{CAS}$ HIGH	Hi-Z
	$\overline{CAS}$ LOW	Data from Last Read Cycle
$\overline{CAS}$-Only Cycle $\overline{RAS}$ HIGH		Hi-Z
Read-Modify-Write Cycle		Data from Addressed Memory Cell

ON-CHIP SUBSTRATE-BIAS GENERATOR

The Am9064 has an on-chip substrate-bias (V_{BB}) generator integrated into the DRAM peripheral circuitry. This accomplishes three purposes:

1. It allows the use of single +5V supply (V_{CC}), so it does away with the need for an external V_{BB} supply. This has become the standard for all NMOS DRAMs 64K and higher.
2. It maintains the high performance of the N-channel MOSFET by providing a stable negative voltage bias (−3V) on the p-type substrate, reducing the parasitic PN junction capacitance and the body effect of the MOSFET threshold voltage.
3. It avoids minority charge injection from a node voltage undershoot to −2V on all inputs.

In addition to the above design features, the fact that the bias generator* is incorporated on-chip makes it possible to shield the V_{BB} bias level from any fluctuations of the external V_{CC} power supply. This on-chip generator has the following characteristics:

1. V_{BB} level is independent of V_{CC}, for $V_{CC} \geq 3V$.
2. V_{BB} level is compensated for temperature variation.
3. Upper and lower levels of V_{BB} are regulated.

In summary, the V_{BB} bias-generator can tolerate a V_{CC} range of 3 to 8V, temperature range of −55 to +110°C, and cycle dependent capacitive coupling.

ALPHA-PARTICLE-INDUCED SOFT ERRORS

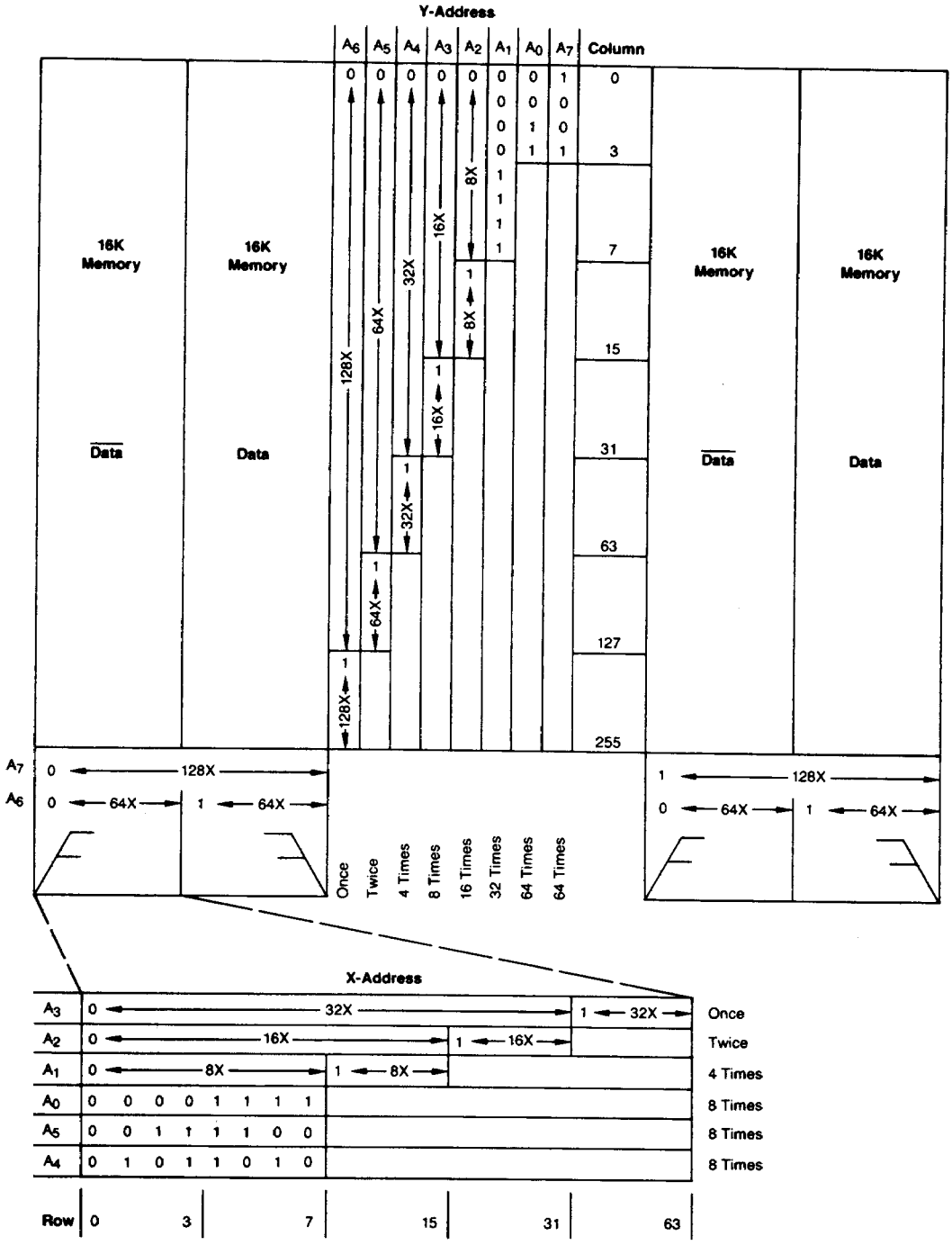
One of the primary causes of soft errors in DRAMs is due to the presence of alpha-particles emitted from the decay of uranium and thorium in the IC packaging materials. When an alpha-particle enters the silicon chip substrate, approximately one million electron-hole pairs are created in the bulk silicon. These generated carriers diffuse and the electrons are collected by depletion layers resulting in the partial or total filling of initially empty potential wells. If the "collection efficiency" times the number of generated carriers exceeds the critical charge in the memory cell a "soft error" will result. A recently published study (*"Drift Collection of Alpha Generated Carriers and Design Implications,"* C. Hu, ISSCC 82) shows that the "collection efficiency" is directly proportional to the width of the depletion layers. Solutions to the alpha problem are implemented in the Am9064 in the following ways:

1. Incorporation of new process technology for the Hi-C* capacitor memory cell.
2. Using low-alpha-source packaging materials.

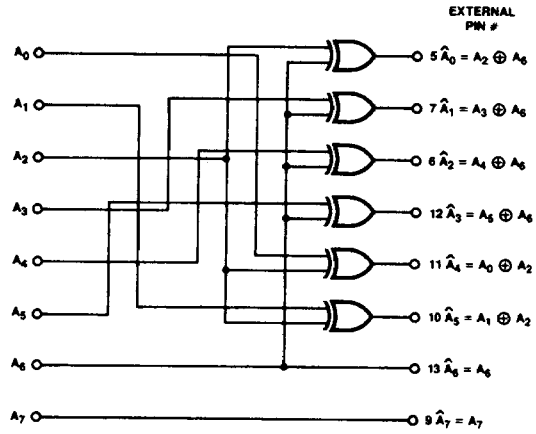
The Hi-C* capacitor memory cell helps solve the alpha problem in two significant ways. First, it increases the memory charge storage by ~ 30%, thus boosting up the "critical charge." Second, it reduces the memory cell junction depletion width by a factor of ~5 to 10, thus reducing the collection efficiency significantly.

*Patent pending.

AM9064 TOPOLOGICAL BIT MAP



ROW TOPOLOGICAL DESCRAMBLE



Ân = EXTERNAL OR PIN ADDRESS
An = INTERNAL ADDRESS

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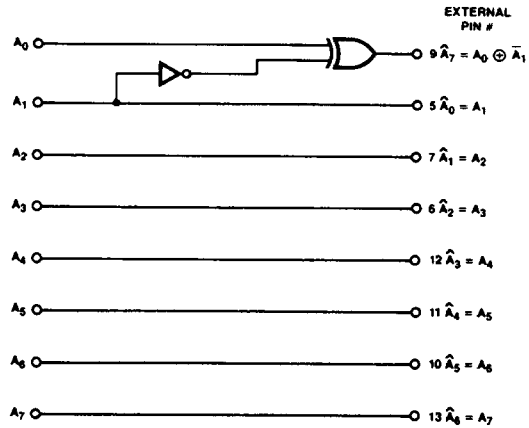
COLUMN TOPOLOGICAL DESCRAMBLE



Ân = EXTERNAL OR PIN ADDRESS
An = INTERNAL ADDRESS

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −10°C to +80°C
Voltage on any pin with
respect to ground ..... −2V to +7.5V
Supply Voltage ..... −1V to +7.5V
Power Dissipation 1.0W
Short Circuit Output Current 50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES

Temperature ..... 0°C to +70°C

Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

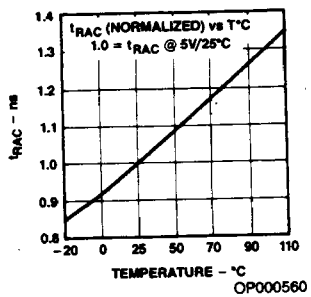
DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CC1}	Operating Current (Note 1) Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = Min	Am9064-10	–	70	mA
			AM9064-12	–	60	
			Am9064-15	–	55	
I_{CC2}	Standby Current Power Supply Current	$\overline{RAS} = \overline{CAS} = V_{IH}$		–	4.0	mA
I_{CC3}	Refresh Current (Note 1) Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min	Am9064-10	–	55	mA
			Am9064-12	–	50	
			Am9064-15	–	45	
I_{CC4}	Page Mode Current (Note 1) Average Power Supply Current	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; t_{PC} = Min	Am9064-10	–	50	mA
			Am9064-12	–	45	
			Am9064-15	–	40	
I_{ILK}	Input Leakage Current	Any Input; $V_{SS} \leq V_{IN} \leq V_{CC}$		−10	+10	µA
I_{OLK}	Output Leakage Current	Data Out Disabled, $V_{SS} \leq V_{OUT} \leq V_{CC}$		−10	+10	µA
V_{OH}	Output High Voltage	I_{OH} = −5.0mA		2.4		–
V_{OL}	Output Low Voltage	I_{OL} = +4.2mA		–	0.4	V
C_{IN1}	Input Capacitance $A_0 - A_7, D_{IN}$				5	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$				7	pF
C_{OUT}	Output Capacitance D_{OUT}				6	pF

Note: $1I_{CC}$ is depedent on output loading and cycle time. Specified values are measured with output open.

DC OPERATING CHARACTERISTICS

Typical Access Time (Normalized) t_{RAC} versus Case Temperature



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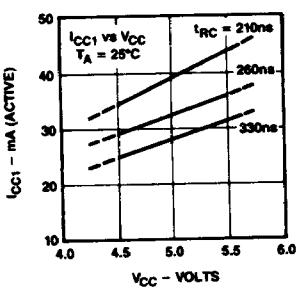
Typical Operating Current I_{CC1} versus V_{CC}



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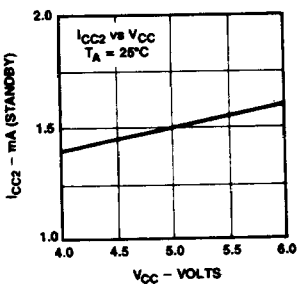
Typical Standby Current I_{CC2} versus V_{CC}



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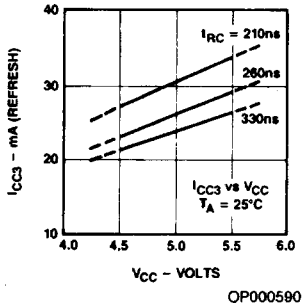
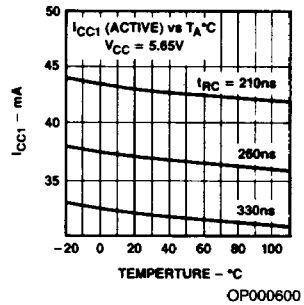
DC OPERATING CHARACTERISTICS (Cont.)

Typical Refresh Current I_{CC3} versus V_{CC}



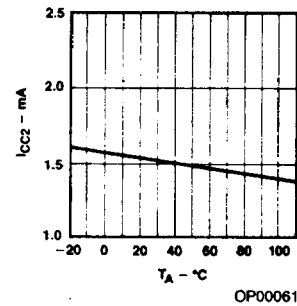
OP000590

Typical Operating Current I_{CC1} versus Case Temperature



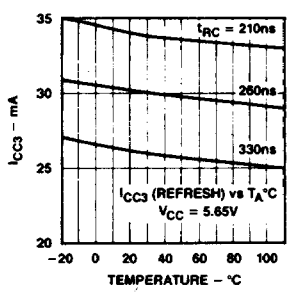
OP000600

Typical Standby Current I_{CC2} versus Case Temperature



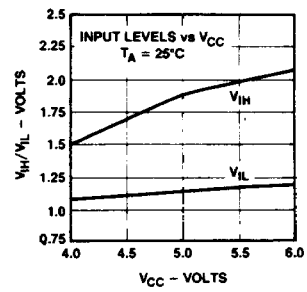
OP000610

Typical Refresh Current I_{CC3} versus Case Temperature



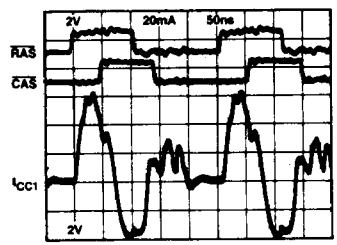
OP000620

Input Voltage Levels versus V_{CC}



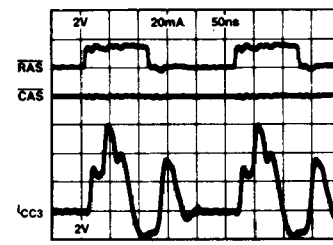
OP000630

$\overline{RAS}/\overline{CAS}$ Cycle



OP000010

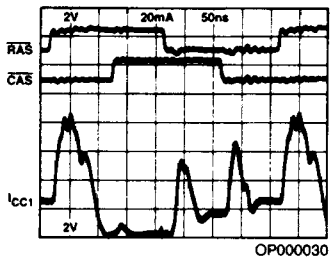
Long $\overline{RAS}/\overline{CAS}$ Cycle



OP000020

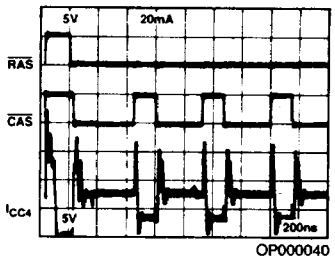
DC OPERATING CHARACTERISTICS (Cont.)

$\overline{RAS}$ Only Cycle



OP000030

Page-Mode Only



OP000040

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Symbol	Description	Am9064-10 Min	Am9064-10 Max	Am9064-12 Min	Am9064-12 Max	Am9064-15 Min	Am9064-15 Max	Units
1	t_{RAC}	Access Time from $\overline{RAS}$ (Notes 6 and 7)		100		120		150	ns
2	t_{CAC}	Access Time from $\overline{CAS}$ (Notes 6 and 7)		55		65		75	ns
3	t_{REF}	Time Between Refresh		2		2		2	ms
4	t_{RP}	$\overline{RAS}$ Precharge Time	80		90		100		ns
5	t_{CPN}	$\overline{CAS}$ Precharge Time (Non-Page Cycles)	30		30		30		ns
6	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-10		-10		-10		ns
7	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Notes 6 and 8)	25	45	30	55	30	75	ns
8	t_{RSH}	$\overline{RAS}$ Hold Time	55		65		75		ns
9	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		ns
10	t_{ASR}	Row Address Setup Time	0		0		0		ns
11	t_{RAH}	Row Address Hold Time	15		20		20		ns
12	t_{ASC}	Column Address Setup Time	0		0		0		ns
13	t_{CAH}	Column Address Hold Time	25		25		30		ns
14	t_{AR}	Column Address Hold Time to $\overline{RAS}$	70		80		105		ns
15	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns
16	t_{OFF}	Output Buffer Turn Off Delay (Note 9)	0	35	0	40	0	40	ns
Read and Refresh Cycles									
17	t_{RC}	Random Read Cycle Time	190		220		260		ns
18	t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns
19	t_{CAS}	$\overline{CAS}$ Pulse Width	55	10,000	65	10,000	75	10,000	ns
20	t_{RCS}	Read Command Setup Time	0		0		0		ns
21	t_{RCH}	Read Command Hold Time to $\overline{CAS}$ (Note 10)	0		0		0		ns
22	t_{RRH}	Read Command Hold Time to $\overline{RAS}$ (Note 10)	0		0		0		ns
Write Cycle									
23	t_{RC}	Random Write Cycle Time	190		220		260		ns
24	t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns
25	t_{CAS}	$\overline{CAS}$ Pulse Width	55	10,000	65	10,000	75	10,000	ns
26	t_{WCS}	Write Command Setup Time (Note 11)	0		-10		-10		ns
27	t_{WCH}	Write Command Hold Time	20		25		35		ns
28	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	65		80		110		ns
29	t_{WP}	Write Command Pulse Width	20		25		35		ns
30	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		40		45		ns
31	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		40		45		ns
32	t_{DS}	Data in Setup Time (Note 12)	0		0		0		ns
33	t_{DH}	Data In Hold Time (Note 12)	20		25		35		ns
34	t_{DHR}	Data In Hold Time to $\overline{RAS}$	65		80		110		ns
Read-Modify-Write Cycle									
35	t_{RWC}	Read-Modify-Write Cycle Time	205		240		280		ns
36	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay (Note 11)	80		95		120		ns
37	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay (Note 11)	35		40		45		ns
Page-Mode Cycle									
38	t_{PC}	Page-Mode Read or Write Cycle	105		120		145		ns
39	t_{CP}	$\overline{CAS}$ Precharge Time, Page-Mode	40		45		60		ns
40	t_{CAS}	$\overline{CAS}$ Pulse Width	55	10,000	65	10,000	75	10,000	ns

Notes:

1. I_{CC} is dependent on output loading and cycle time. Specified values are measured with output open.
2. Capacitance measured with a Boonton Meter or calculated from the equation: $C = 1\Delta t/\Delta V$.
3. An initial pause of 100μsec is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. AC characteristics assume $t_T = 5$ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between these two levels.
6. Maximum t_{RCD} is specified as a reference point only. If $t_{RCD} \leq$ maximum allowed, access time is t_{RAC}. If $t_{RCD} > t_{RCD}$ (max), either access time is controlled exclusively by t_{CAC}, or t_{RAC} will increase by the amount that t_{RCD} exceeds the specified maximum.
7. Output load is equivalent to two standard TTL loads and 100pF.
8. t_{RCD} (min) = $t_{RAH} + t_{ASC} + 2t_T$.
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
11. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points and are not restrictive operating parameters. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early Write Cycle and the

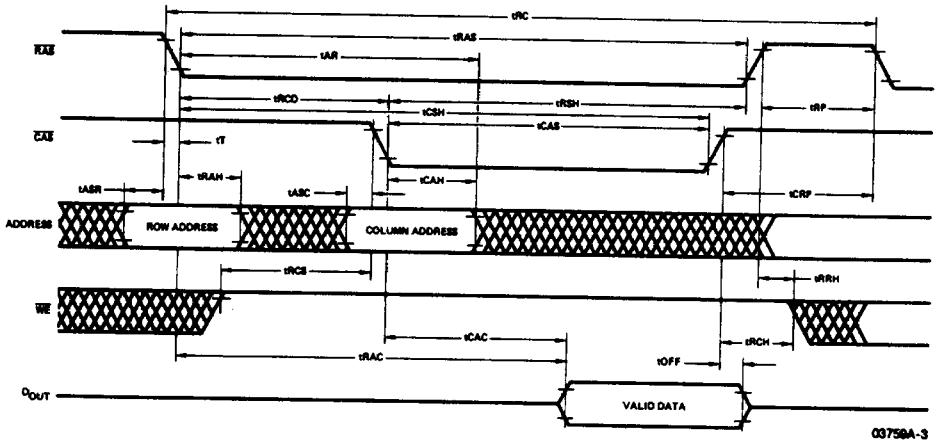
SWITCHING CHARACTERISTICS (Cont.)

D_{OUT} pin will remain Hi-Z throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is Read-Write Cycle and D_{OUT} will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of D_{OUT} (at access time) is indeterminate.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early Write cycles and to $\overline{WE}$ leading edge in delayed Write or Read-Modify-Write cycles.

SWITCHING WAVEFORMS

READ CYCLE



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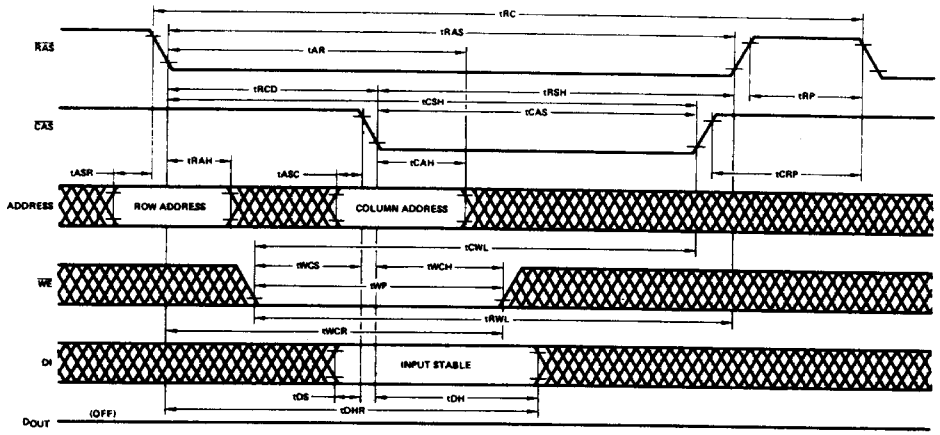
WRITE CYCLE



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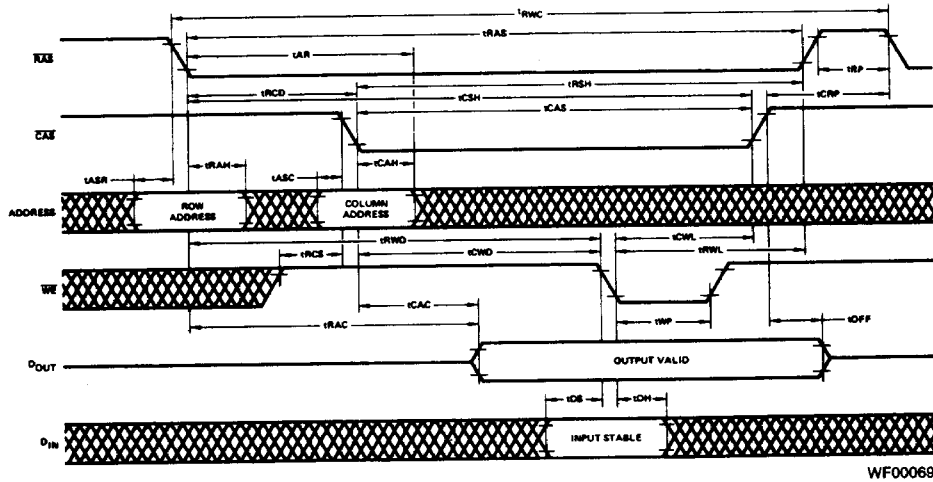
SWITCHING WAVEFORMS (Cont.)

READ-WRITE/READ-MODIFY-WRITE CYCLE



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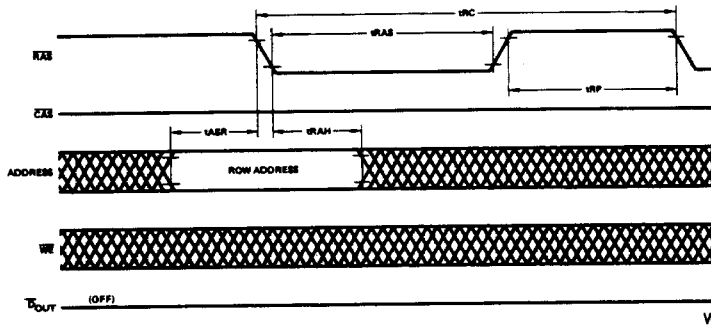
RAS-ONLY REFRESH CYCLE



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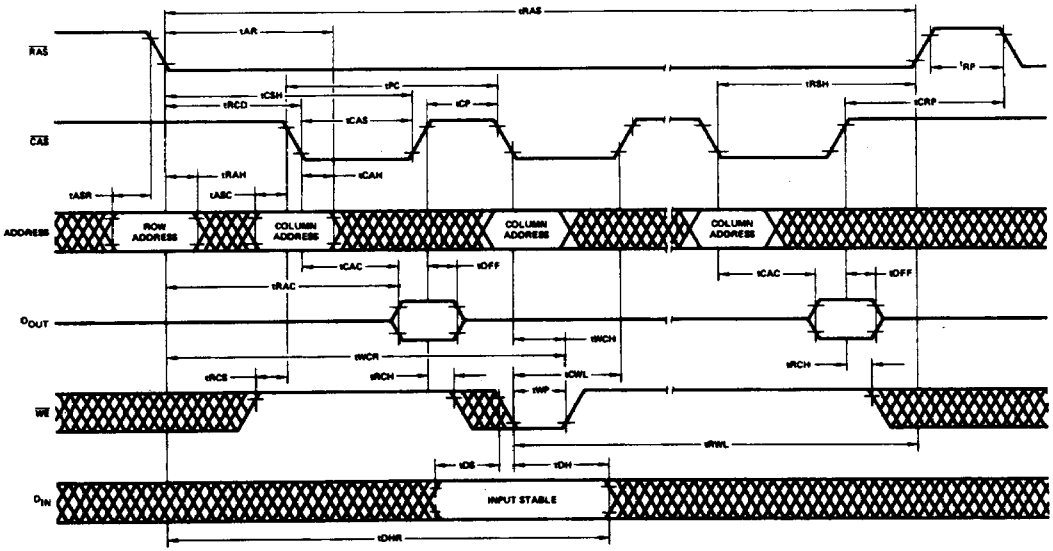
SWITCHING WAVEFORMS (Cont.)

PAGE-MODE CYCLE



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