Am9101/Am91L01/Am2101 FAMILY

256x4 Static R/W Random Access Memories

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PART NUMBER	Am2101	Am2101-2	Am9101A Am91L01A Am2101-1	Am9101B Am91L01B	Am9101C Am91L01C	Am9101D
ACCESS TIME	1000ns	650ns	500ns	400ns	300ns	250ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply —
  tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

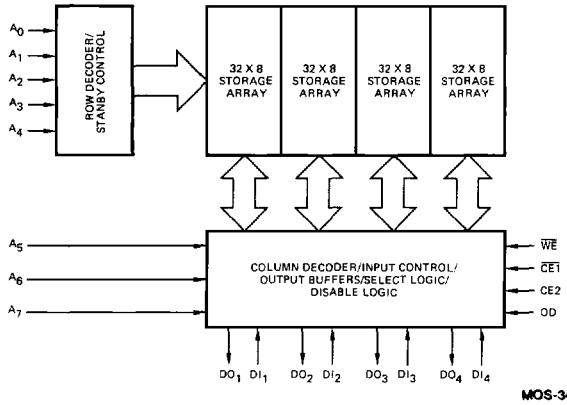
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84 percent of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9101 BLOCK DIAGRAM



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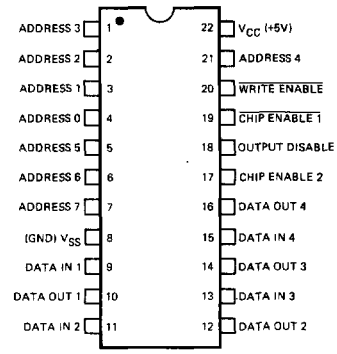
CONNECTION DIAGRAM
Top View



Note: Flat Pack version available in 24-pin package.

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ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times					
			1000ns	650ns	500ns	400ns	300ns	250ns
0°C to +70°C	Molded DIP	Standard	P2101	P2101-2	P2101-1 AM9101APC	AM9101BPC	AM9101CPC	AM9101DPC
		Low			AM91L01APC	AM91L01BPC	AM91L01CPC	
	Hermetic DIP	Standard	C2101	C2101-2	C2101-1 AM9101ADC	AM9101BDC	AM9101CDC	AM9101DDC
		Low			AM91L01ADC	AM91L01BDC	AM91L01CDC	
−55°C to +125°C	Hermetic DIP	Standard			AM9101ADM	AM9101BDM	AM9101CDM	
		Low			AM91L01ADM	AM91L01BDM	AM91L01CDM	
	Hermetic Flat Pack	Standard			AM9101AFM	AM9101BFM		
		Low			AM91L01AFM	AM91L01BFM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9101PC, Am9101DC, Am91L01PC, Am91L01DC, Am2101: T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions			Am9101/Am91L01 Family Min.	Am9101/Am91L01 Family Max.	Am2101 Family Min.	Am2101 Family Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.		I_{OH} = −200μA	2.4				Volts
				I_{OH} = −150μA			2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN.		I_{OL} = 3.2mA		0.4			Volts
				I_{OL} = 2.0mA				0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.2	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.25V				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		5.0		15	μA
				V_{OUT} = 0.4V		−10		−50	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9101A/B		50		60	mA
				Am9101C/D/E		55			
				Am91L01A/B		31			
				Am91L01C		34			
I_{CC2}			T_A = 0°C	Am9101A/B		55		70	
				Am9101C/D/E		60			
				Am91L01A/B		33			
				Am91L01C		36			

ELECTRICAL CHARACTERISTICS

Am9101DM, Am9101FM, Am91L01DM, Am91L01FM: T_A = −55°C to +125°C, V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions			Am9101/Am91L01 Family Min.	Am9101/Am91L01 Family Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{CC} = 4.75V	2.4		Volts
				V_{CC} = 4.5V	2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.5V				10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		10	μA
				V_{OUT} = 0.4V		−10	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9101A/B		50	mA
				Am9101C		55	
				Am91L01A/B		31	
				Am91L01C		34	
I_{CC3}			T_A = −55°C	Am9101A/B		60	
				Am9101C		65	
				Am91L01A/B		37	
				Am91L01C		40	

CAPACITANCE

Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	T_A = 25°C, f = 1MHz	Am2101	4.0	8.0	pF
			Am9101/Am91L01	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2101	8.0	12	pF
			Am9101/Am91L01	6.0	9.0	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

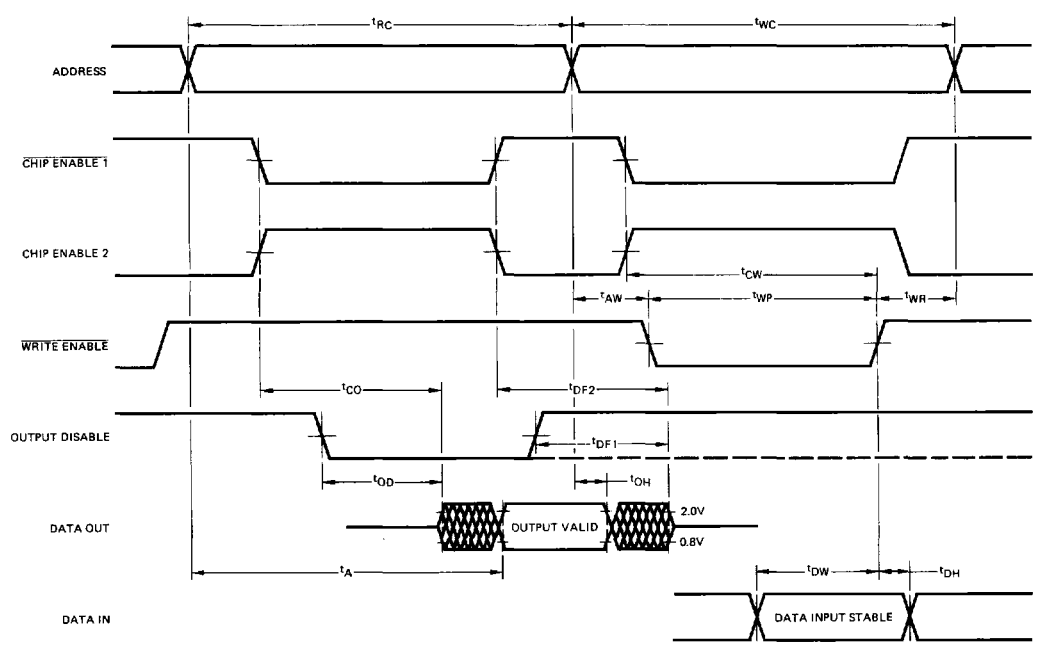
Output Load = 1 TTL Gate + 100pF — T_A = 0 to 70°C — V_{CC} = +5V ±5%
Transition Times = 10ns — T_A = −55 to +125°C — V_{CC} = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

Parameters	Description	2101 Min	2101 Max	2101-2 Min	2101-2 Max	2101-1 Min	2101-1 Max	9101A 91L01A Min	9101A 91L01A Max	9101B 91L01B Min	9101B 91L01B Max	9101C 91L01C Min	9101C 91L01C Max	9101D Min	9101D Max	Units
t_{RC}	Read Cycle Time	1000		650		500		500		400		300		250		ns
t_A	Access Time		1000		650		500		500		400		300		250	ns
t_{CO}	Chip Enable to Output ON Delay (Note 1)		800		400		350		200		175		150		125	ns
t_{OD}	Output Disable to Output ON Delay		700		350		300		175		150		125		100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		40		40		40		30		ns
t_{DF1}	Output Disable to Output OFF Delay	0	200	0	150	0	150	5.0	125	5.0	100	5.0	100	5.0	75	ns
t_{DF2}	Chip Enable to Output OFF Delay	0	200	0	150	0	150	10	125	10	125	10	100	10	100	ns
t_{WC}	Write Cycle Time	1000		650		500		500		400		300		250		ns
t_{AW}	Address Set-up Time	150		150		100		0		0		0		0		ns
t_{WP}	Write Pulse Width	750		400		300		175		150		125		100		ns
t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		175		150		125		100		ns
t_{WR}	Address Hold Time	50		50		50		0		0		0		0		ns
t_{DW}	Input Data Set-up Time	700		400		280		150		125		100		85		ns
t_{DH}	Input Data Hold Time	100		100		100		0		0		0		0		ns

Note: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

SWITCHING WAVEFORMS

READ CYCLE — WRITE CYCLE



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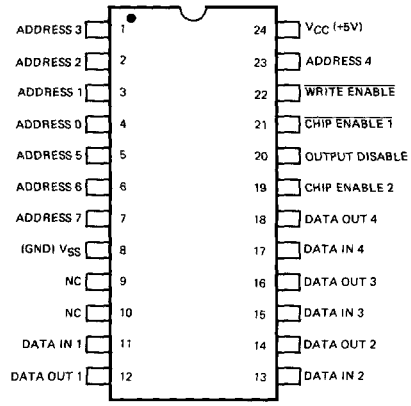
CONNECTION DIAGRAM
Top View

Flat Package



Pin 1 is marked for orientation.

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DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE1}$, **CE2** Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{OD} Output enable time. Delay time from falling edge of OD to output on.

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH} Minimum time which will elapse between change of address and any change of the data output.

t_{DF1} Time delay between output disable HIGH and output data float.

t_{DF2} Time delay between chip enable OFF and output data float.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

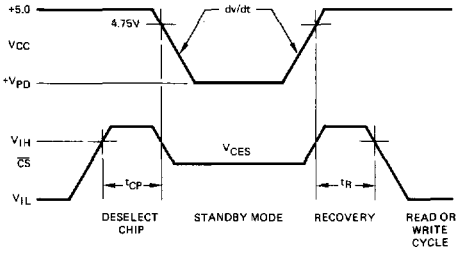
POWER DOWN STANDBY OPERATION

The Am9101/Am91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

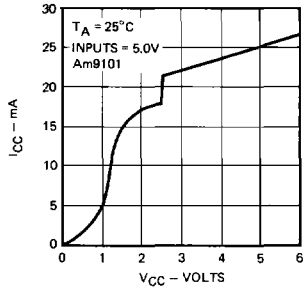
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

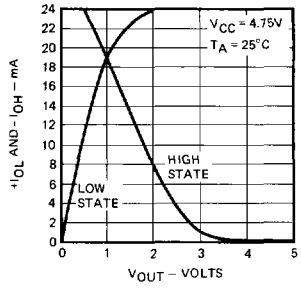
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	25	mA
				Am9101		13	31	
			$V_{PD} = 2.0V$	Am91L01		13	31	
				Am9101		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	28	mA
				Am9101		13	34	
			$V_{PD} = 2.0V$	Am91L01		13	34	
				Am9101		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



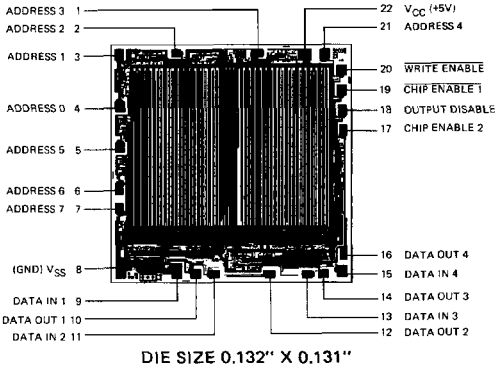
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage



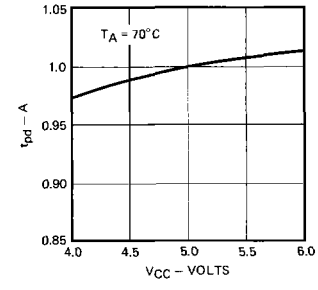
Metallization and Pad Layout



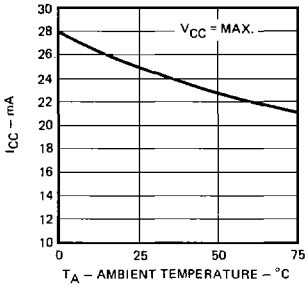
DIE SIZE 0.132" X 0.131"

(Pin numbers are for DIP configurations only)

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



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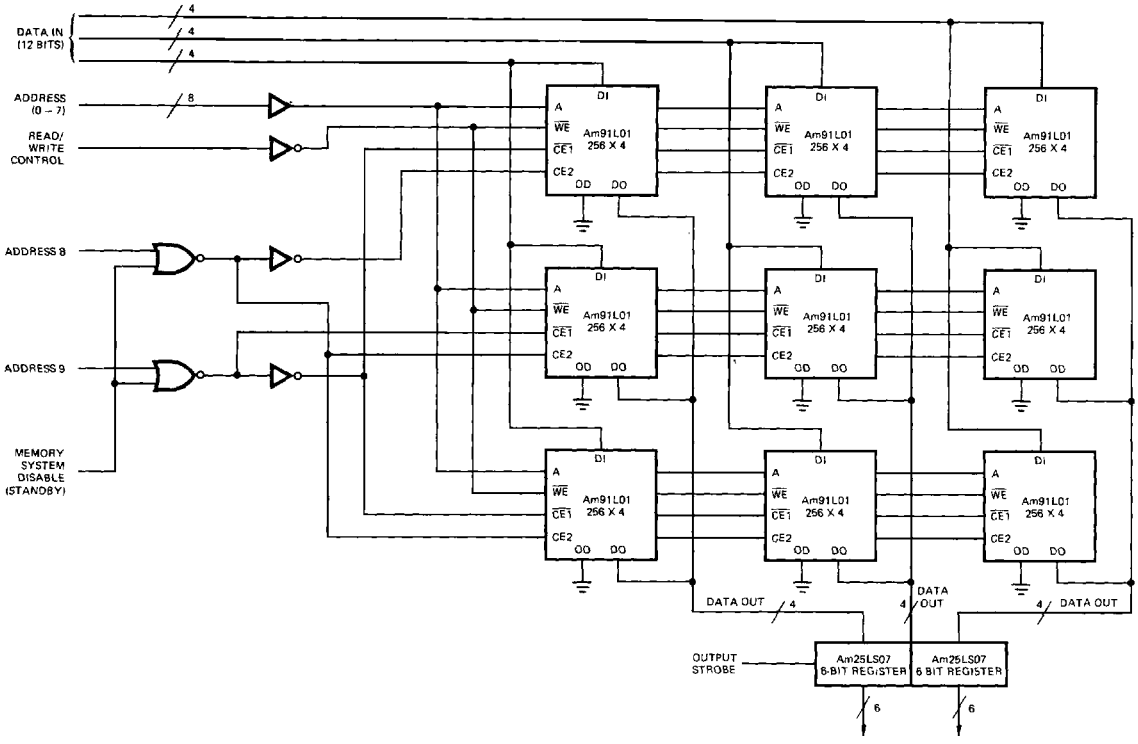
APPLICATIONS



MEMORY SYSTEM
768 WORDS BY 12 BITS PER WORD

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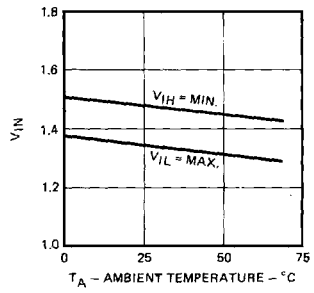
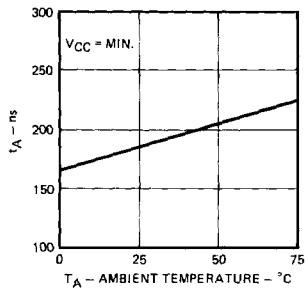
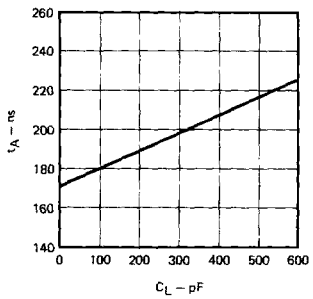
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L



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