AM9709, AM97C09, AH5009 Series Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches designed to economically fulfill a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

The AM97C09 series is specifically intended to be driven from CMOS providing the best performance at lowest cost.

Applications

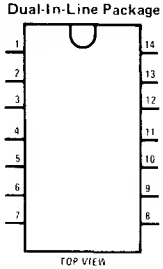
- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

Interfaces with standard TTL and CMOS	
On-resistance match	2 ohms
Low "ON" resistance	100 ohms
Very low leakage	50 pA
Large analog signal range	±10V peak
High switching speed	150 ns
Excellent isolation between channels	80 dB at 1 kHz

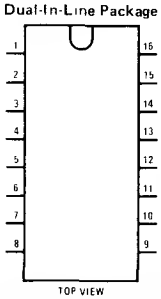
Connection Diagrams

Dual-In-Line Package



Order Number AM9709CN, AM9710CN, AM97C09CN, AM97C10CN, AH5009CN, AH5010CN, AH5013CN or AH5014CN
See Package 21

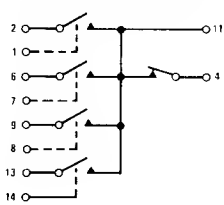
Dual-In-Line Package



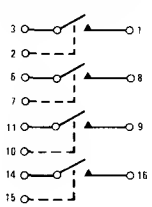
Order Number AM9711CN, AM9712CN, AM97C09CN, AM97C10CN, AH5011CN, AH5012CN, AH5015CN or AH5016CN
See Package 22

Functional and Schematic Diagrams (Additional type on other pages)

MUX Switches (4-Channel Version Shown)

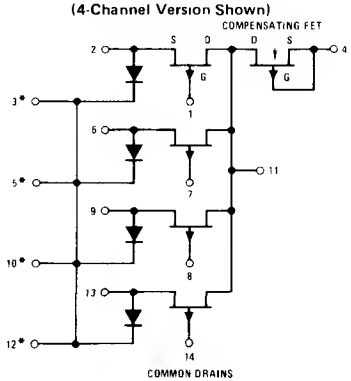


SPST Switches (Quad Version Shown)

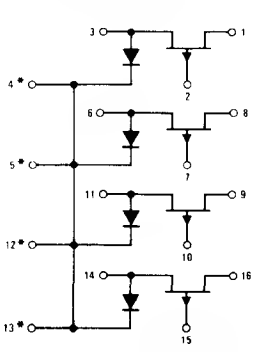


*Note: All diode cathodes are internally connected to the substrate.

MUX Switches (4-Channel Version Shown)



SPST Switches (Quad Version Shown)



Absolute Maximum Ratings

Input Voltage	
AM9709–12CN, AH5009–24CN	30V
AM97C09–12CN	25V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

AM9709, AM97C09, AH5009 (Notes 1 and 2)

PARAMETER		CONDITIONS	5V TTL AM9710CN AM9712CN		5V TTL AH5010–16 (EVEN SERIES)		5V–10V CMOS AM97C10CN AM9712CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V	0.01	0.2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 4.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} 0V, I_S = 1 mA	0.08	1	0.08	1	0.08	1	nA
		T_A = 85°C		200		200		200	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.13	5		1000	0.13	5	nA
		T_A = 85°C		10		10		10	µA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.1	10		100	0.10	10	nA
		T_A = 85°C		20		100		20	µA
$r_{DS(ON)}$	Drain Source Resistance	V_{GS} = 0.35V, I_S = 2 mA	90	150	90	150			Ω
		T_A = +85°C		240		240			Ω
$r_{DS(ON)}$	Drain Source Resistance	V_{GS} = 0V, I_S = 2 mA					90	150	Ω
		T_A = 85°C						240	Ω
V_{DIODE}	Forward Diode Drop	I_D 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	4	20		50	4	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Note 1: Test conditions 25°C unless otherwise noted.
Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

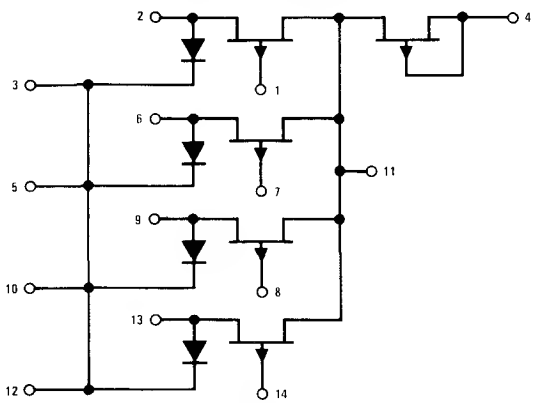
Electrical Characteristics (Continued)

PARAMETER		CONDITIONS	15V TTL AM9709CN AM9711CN		15V TTL AH5009–15 (DDD SERIES)		10–15V CMDS AM97C09CN AM97C11CN		UNITS
			TYP	MAX	TYP	MAX	TYP	MAX	
I_{GSX}	Input Current "OFF"	V_{GD} = 11V, V_{SD} = 0.7V	0.01	2	0.01	0.2			nA
		T_A = 85°C		100		10			nA
I_{GSX}	Input Current "OFF"	V_{GD} = 15V, V_{SD} = 0.7V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 9.3V					0.01	2	nA
		T_A = 85°C						100	nA
$I_{D(OFF}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 10.3V	0.01	2	0.01	0.2			nA
		T_A = 85°C		10		10			nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.04	0.5	0.04	0.5	0.04	0.5	nA
		T_A = 85°C		100		100		100	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.07	2		2	0.07	2	nA
		T_A = 85°C		1		2		1	μA
$I_{G(ON}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.05	5		100	0.05	5	nA
		T_A = 85°C		2		20		2	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0V, I_S = 2 mA					60	100	Ω
		T_A = 85°C						160	Ω
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 1.5V, I_S = 2 mA	60	100	60	100			Ω
		T_A = 85°C		160		160			Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8				0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, i_D = 1 mA	2	10		50	2	10	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	150	500	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	300	500	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		120		120		dB

Schematic Diagrams and Pin Connections

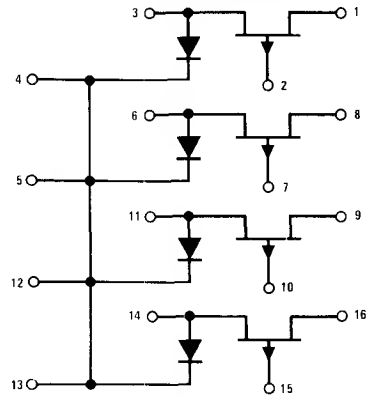
Four Channel

AM97C09CN ($R_{DS(DN)} \leq 100\Omega$, 10–15V CMOS)
AM97C10CN ($R_{DS(DN)} \leq 150\Omega$, 5–10V CMDS)
AM9709CN, AH5009CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AM9710CN, AH5010CN ($R_{DS(DN)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

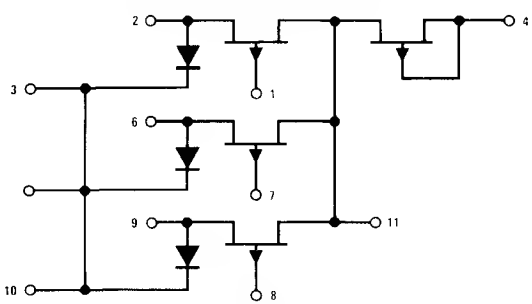
AM97C11CN ($R_{DS(DN)} \leq 100\Omega$, 10–15V CMOS)
AM97C12CN ($R_{DS(DN)} \leq 150\Omega$, 5–10V CMDS)
AM9711CN, AH5011CN ($R_{DS(DN)} \leq 100\Omega$, 15V TTL)
AM9712CN, AH5012CN ($R_{DS(ON)} \leq 150\Omega$, 5V TTL)



16-Pin DIP

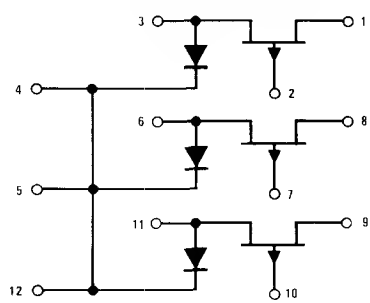
Three-Channel

AH5013CN ($R_{DS(DN)} \leq 100\Omega$, 15V TTL)
AH5014CN ($R_{DS(DN)} \leq 150\Omega$, 5V TTL)



14-Pin DIP

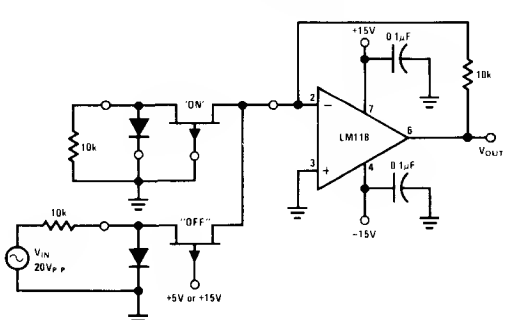
AH5015CN ($R_{DS(ON)} \leq 100\Omega$, 15V TTL)
AH5016CN ($R_{DS(DN)} \leq 150\Omega$, 5V TTL)



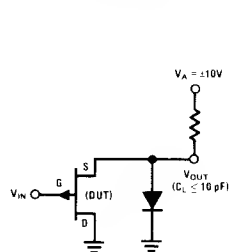
16-Pin DIP

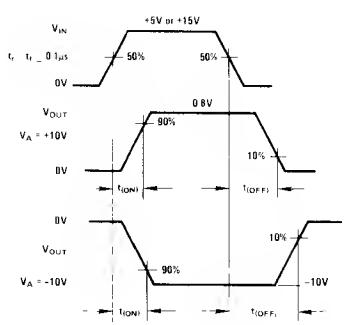
Test Circuits and Switching Time Waveforms

Cross Talk Test Circuit



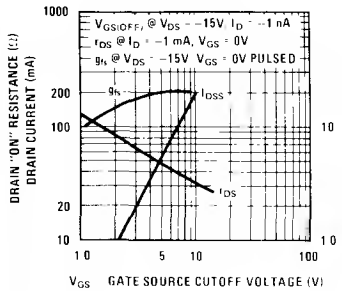
ac Test Circuit



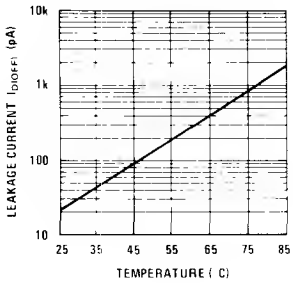


Typical Performance Characteristics

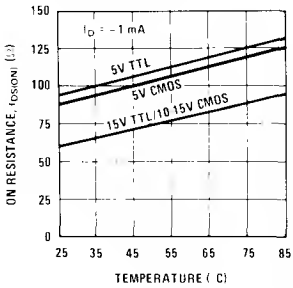
Parameter Interaction



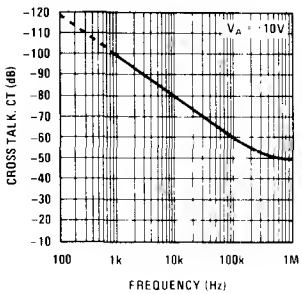
Leakage Current, $I_{D(OFF)}$ vs Temperature



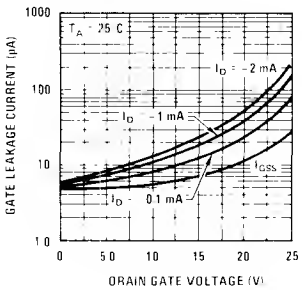
On Resistance, $r_{DS(ON)}$ vs Temperature



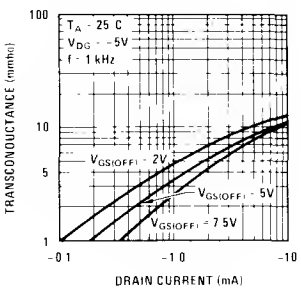
Cross Talk, CT vs Frequency



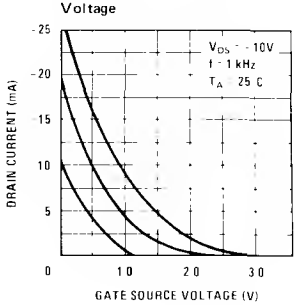
Leakage Current vs Drain Gate Voltage



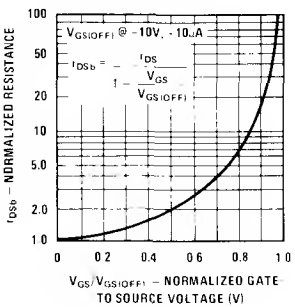
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



Applications Information

Theory of Operation

The AM/AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL (AM9710), 5V–10V CMOS (AM97C10), open collector 15V TTL (AM9709), and 10–15V CMOS (AM97C09).

Two basic switch configurations are available: multiple independent switches (N by SPST) and multiple pole switches used for multiplexing (NPST-MUX). The MUX versions such as the AM9709 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

5

Applications Information (Continued)

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AM/AH series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2,* $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \qquad (2a)$$

or

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is worse.

Where $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

≃ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AM9710. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3,* the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\, A_D}{(N)\, I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AM9709, $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

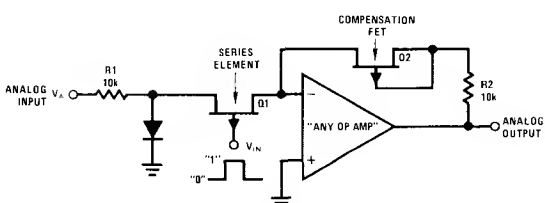


FIGURE 1. Use of Compensation FET

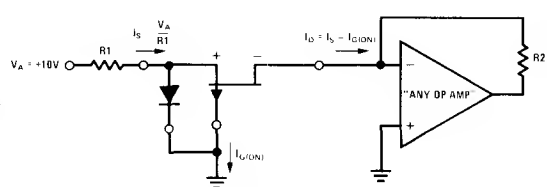


FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

TTL Compatibility

Two input logic drive versions of AM/AH series are available: the even numbered part types are specified to be driven from standard 5V-TTL logic and the odd numbered types from 15V open collector TTL.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AM9710, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5*. In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} and the expense of power dissipation in the low state.

CMOS Compatibility

The cost effective AM97C09 series of switches is optimized for CMOS drive without resistor pull-up. The AM97C10's and AM97C12's are specified for 5V–10V operation while the AM97C09's and AM97C11's are specified for 10V–15V operation.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6*.

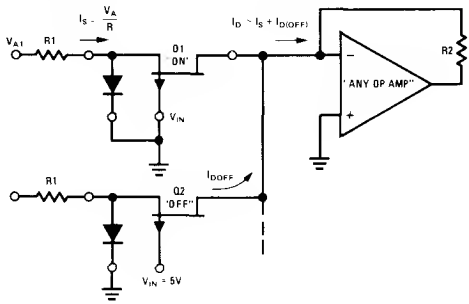


FIGURE 3.

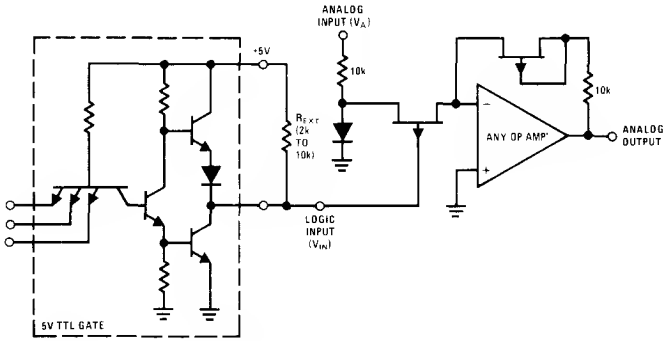


FIGURE 4. Interfacing with +5V TTL

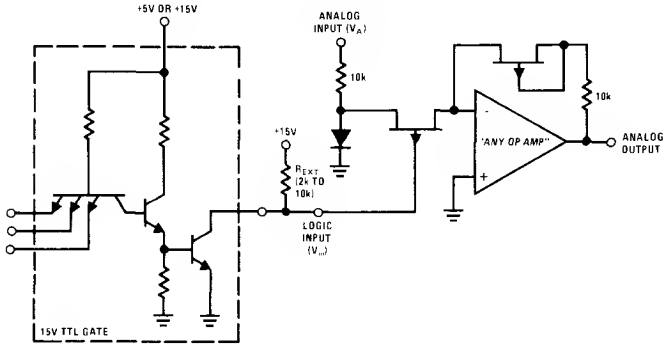


FIGURE 5. Interfacing with +15V Open Collector TTL

Applications Information (Continued)

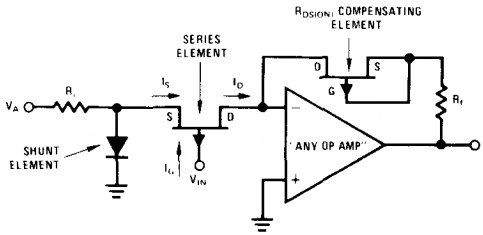
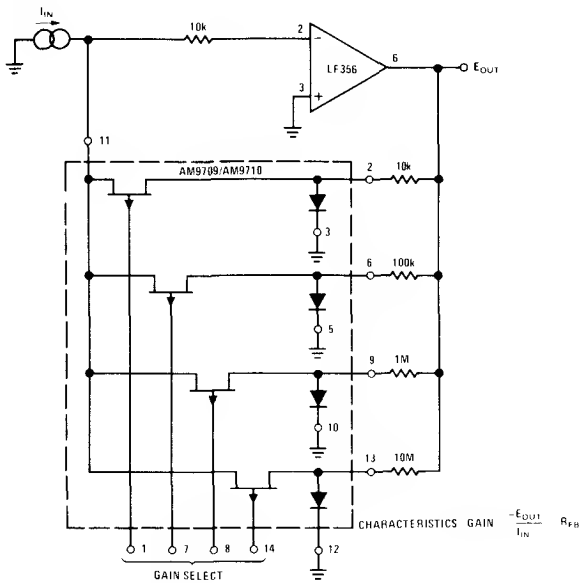


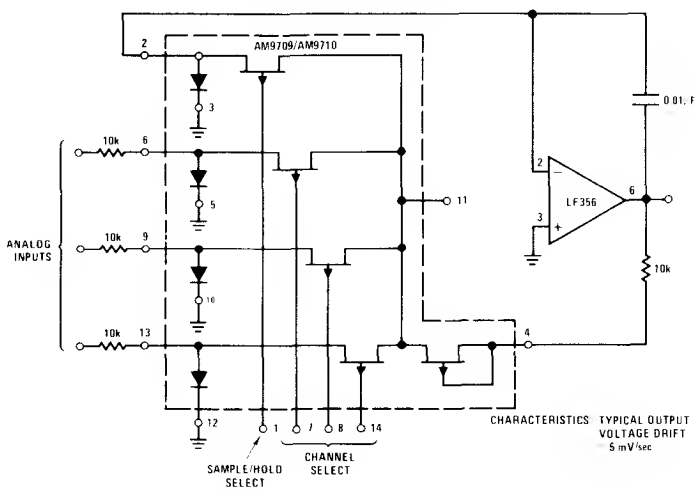
FIGURE 6. Definition of Terms

Typical Applications

Gain Programmable Amplifier

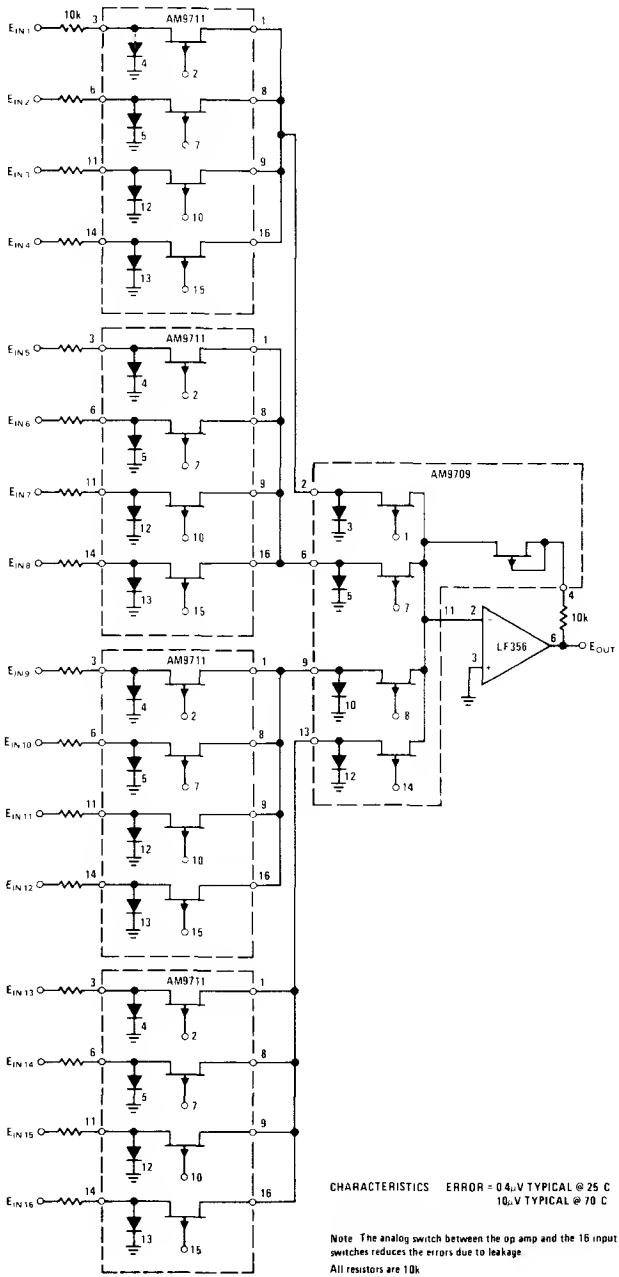


3-Channel Multiplexer with Sample and Hold



Typical Applications (Continued)

16-Channel Multiplexer



CHARACTERISTICS ERROR = 0.4μV TYPICAL @ 25 C
10μV TYPICAL @ 70 C

Note The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k

Typical Applications (Continued)

8-Bit Binary (BCD) Multiplying D/A Converter