

# AMC0x02R Precision, $\pm 50\text{-mV}$ Input, Basic and Reinforced Isolated Amplifiers With Single-Ended, Ratiometric Output

## 1 Features

- Linear input voltage range:  $\pm 50\text{mV}$
- Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Single-ended, ratiometric output
  - Reference Input: 2.7V to 5.5V
- Low DC errors:
  - Offset error:  $\pm 50\mu\text{V}$  (maximum)
  - Offset drift:  $\pm 1\mu\text{V}/^\circ\text{C}$  (maximum)
  - Gain error:  $\pm 0.2\%$  (maximum)
  - Gain drift:  $\pm 45\text{ppm}/^\circ\text{C}$  (maximum)
  - Nonlinearity: 0.04% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0202R: Basic isolation
  - AMC0302R: Reinforced Isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577
- Fully specified over the extended industrial temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

## 2 Applications

- Industrial motor drives
- Frequency inverters
- Server Power Supply Units (PSU)
- Power Factor Correction (PFC)

## 3 Description

The AMC0x02R is a precision, galvanically isolated amplifier with a  $\pm 50\text{mV}$ , differential input and single-ended, ratiometric output. The input is optimized for direct connection to a shunt resistor or other low-impedance signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to  $5\text{kV}_{\text{RMS}}$  (DWV package) and basic isolation up to  $3\text{kV}_{\text{RMS}}$  (D package) (60s).

The AMC0x02R outputs a single-ended signal proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0x02R is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

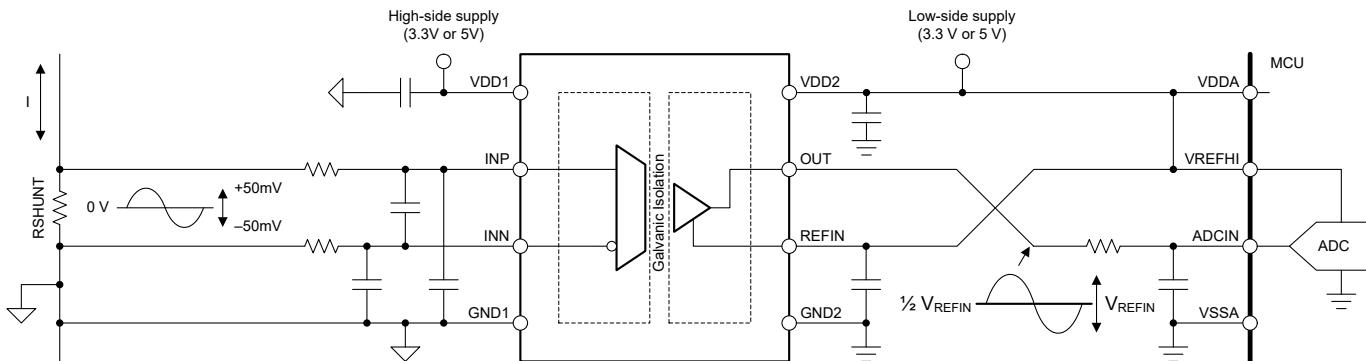
The AMC0x02R comes in 8-pin, wide- and narrow-body SOIC packages, and is fully specified over the temperature range from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

## Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| AMC0202R    | D (SOIC, 8)            | 4.9mm $\times$ 6mm          |
| AMC0302R    | DWV (SOIC, 8)          | 5.85mm $\times$ 11.5mm      |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



## Typical Application



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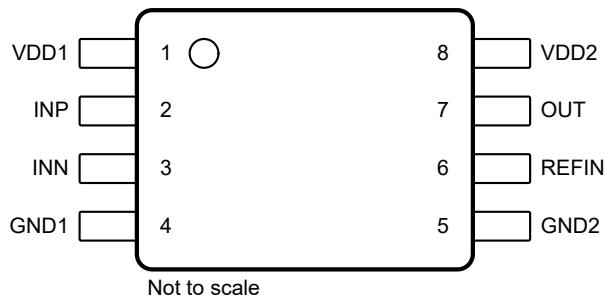
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## 4 Device Comparison Table

| PARAMETER                        | AMC0202R             | AMC0302R             |
|----------------------------------|----------------------|----------------------|
| Isolation rating per VDE 0884-17 | Basic                | Reinforced           |
| Package                          | Narrow-body SOIC (D) | Wide-body SOIC (DWV) |

## 5 Pin Configuration and Functions



**Figure 5-1. DWV and D Packages, 8-Pin SOIC (Top View)**

**Table 5-1. Pin Functions**

| PIN |       | TYPE             | DESCRIPTION  |
|-----|-------|------------------|--|
| NO. | NAME  |                  |  |
| 1   | VDD1  | High-side power  | High-side power supply <sup>(1)</sup>  |
| 2   | INP   | Analog input     | Noninverting analog input <sup>(2)</sup>   |
| 3   | INN   | Analog Input     | Inverting analog input <sup>(2)</sup>  |
| 4   | GND1  | High-side ground | High-side analog ground  |
| 5   | GND2  | Low-side ground  | Low-side analog ground   |
| 6   | REFIN | Analog input     | The voltage applied to this pin sets the full-scale output of the device.<br>Connect REFIN to a low-impedance source as described in the <a href="#">Connecting the REFIN Pin</a> section. |
| 7   | OUT   | Analog output    | Analog output  |
| 8   | VDD2  | Low-side power   | Low-side power supply <sup>(1)</sup>   |

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Input Filter Design](#) section for input filter design recommendations.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                         |  |            | MIN        | MAX | UNIT |
|-------------------------|--|------------|------------|-----|------|
| Power-supply voltage    | High-side VDD1 to GND1                       |            | -0.3       | 6.5 | V    |
|                         | Low-side VDD2 to GND2                        |            | -0.3       | 6.5 |      |
| Analog input voltage    | INP, INN to GND1                             | GND1 – 4   | VDD1 + 0.5 | V   |      |
| Reference input voltage | REFIN to GND2                                | GND2 – 0.5 | VDD2 + 0.5 | V   |      |
| Analog output voltage   | OUT to GND2                                  | GND2 – 0.5 | VDD2 + 0.5 | V   |      |
| Input current           | Continuous, any pin except power-supply pins | -10        | 10         | mA  |      |
| Temperature             | Junction, $T_J$                              |            | 150        | °C  |      |
|                         | Storage, $T_{stg}$                           | -65        | 150        |     |      |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|             |                         |   | VALUE      | UNIT |
|-------------|-------------------------|---|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | $\pm 2000$ | V    |
|             |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | $\pm 1000$ |      |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                          |   |                                   | MIN    | NOM  | MAX | UNIT |
|--------------------------|---|-----------------------------------|--------|------|-----|------|
| <b>POWER SUPPLY</b>      |   |                                   |        |      |     |      |
| VDD1                     | High-side power supply                                    | VDD1 to GND1                      | 3      | 5.0  | 5.5 | V    |
| VDD2                     | Low-side power supply                                     | VDD2 to GND2                      | 3      | 3.3  | 5.5 | V    |
| <b>ANALOG INPUT</b>      |   |                                   |        |      |     |      |
| $V_{Clipping}$           | Nominal differential input voltage before clipping output | $V_{IN} = V_{INP} - V_{INN}$      | -64    | 64   | 64  | mV   |
| $V_{FSR}$                | Specified linear differential input voltage               | $V_{IN} = V_{INP} - V_{INN}$      | -50    | 50   | 50  | mV   |
| $V_{CM}$                 | Operating common-mode input voltage                       | $(V_{INP} + V_{INN}) / 2$ to GND1 | -0.032 | 1    | 1   | V    |
| $C_{IN, EXT}$            | Minimum external capacitance connected to the input       | from INP to INN                   |        | 10   | 10  | nF   |
| <b>REFERENCE INPUT</b>   |   |                                   |        |      |     |      |
| $V_{REFIN}$              | Reference input voltage                                   | REFIN to GND2                     | 2.7    | VDD2 | V   |      |
| <b>ANALOG OUTPUT</b>     |   |                                   |        |      |     |      |
| $C_{LOAD}$               | Capacitive load   | OUT to GND2                       |        | 500  | 500 | pF   |
| $R_{LOAD}$               | Resistive load  | OUT to GND2                       | 10     | 1    | 1   | kΩ   |
| <b>TEMPERATURE RANGE</b> |   |                                   |        |      |     |      |
| $T_A$                    | Specified ambient temperature                             |                                   | -40    | 125  | 125 | °C   |

## 6.4 Thermal Information (D Package)

| THERMAL METRIC <sup>(1)</sup> |  | D (SOIC) | UNIT |
|-------------------------------|--|----------|------|
|                               |  | 8 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 116.5    | °C/W |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance    | 52.8     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 58.9     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 19.4     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 58.0     | °C/W |
| $R_{\theta JC(\text{bot})}$   | Junction-to-case (bottom) thermal resistance | N/A      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Thermal Information (DWV Package)

| THERMAL METRIC <sup>(1)</sup> |  | DWV (SOIC) | UNIT |
|-------------------------------|--|------------|------|
|                               |  | 8 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 102.8      | °C/W |
| $R_{\theta JC(\text{top})}$   | Junction-to-case (top) thermal resistance    | 45.1       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 63.0       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 14.3       | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 61.1       | °C/W |
| $R_{\theta JC(\text{bot})}$   | Junction-to-case (bottom) thermal resistance | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.6 Power Ratings

| PARAMETER |  | TEST CONDITIONS      | VALUE | UNIT |
|-----------|--|----------------------|-------|------|
| $P_D$     | Maximum power dissipation (both sides) | $VDD1 = VDD2 = 5.5V$ | 80    | mW   |
| $P_{D1}$  | Maximum power dissipation (high-side)  | $VDD1 = 5.5V$        | 38    | mW   |
| $P_{D2}$  | Maximum power dissipation (low-side)   | $VDD2 = 5.5V$        | 42    | mW   |

## 6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   | VALUE         | UNIT             |
|--|---|---|---------------|------------------|
| <b>GENERAL</b>   |   |   |               |                  |
| CLR  | External clearance <sup>(1)</sup>                     | Shortest pin-to-pin distance through air  | $\geq 4$      | mm               |
| CPG  | External creepage <sup>(1)</sup>                      | Shortest pin-to-pin distance across the package surface   | $\geq 4$      | mm               |
| DTI  | Distance through insulation                           | Minimum internal gap (internal clearance) of the insulation   | $\geq 15.4$   | $\mu\text{m}$    |
| CTI  | Comparative tracking index                            | DIN EN 60112 (VDE 0303-11); IEC 60112   | $\geq 600$    | V                |
|  | Material group  | According to IEC 60664-1  | I             |                  |
|  | Overvoltage category per IEC 60664-1                  | Rated mains voltage $\leq 300\text{V}_{\text{RMS}}$   | I-IV          |                  |
|  |   | Rated mains voltage $\leq 600\text{V}_{\text{RMS}}$   | I-III         |                  |
| <b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b> |   |   |               |                  |
| $V_{\text{IORM}}$                                      | Maximum repetitive peak isolation voltage             | At AC voltage   | 1130          | $V_{\text{PK}}$  |
| $V_{\text{IOWM}}$                                      | Maximum-rated isolation working voltage               | At AC voltage (sine wave)   | 800           | $V_{\text{RMS}}$ |
|  |   | At DC voltage   | 1130          | $V_{\text{DC}}$  |
| $V_{\text{IOTM}}$                                      | Maximum transient isolation voltage                   | $V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1\text{s}$ (100% production test)   | 4250          | $V_{\text{PK}}$  |
| $V_{\text{IMP}}$                                       | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1  | 5000          | $V_{\text{PK}}$  |
| $V_{\text{IOSM}}$                                      | Maximum surge isolation voltage <sup>(4)</sup>        | Tested in oil (qualification test),<br>1.2/50 $\mu\text{s}$ waveform per IEC 62368-1  | 10000         | $V_{\text{PK}}$  |
| $q_{\text{pd}}$  | Apparent charge <sup>(5)</sup>                        | Method a, after input/output safety test subgroups 2 and 3,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$ | $\leq 5$      | $\text{pC}$      |
|  |   | Method a, after environmental tests subgroup 1,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.3 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$             | $\leq 5$      |                  |
|  |   | Method b1, at preconditioning (type test) and routine test,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 1\text{s}$ , $V_{\text{pd}(\text{m})} = 1.5 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1\text{s}$   | $\leq 5$      |                  |
|  |   | Method b2, at routine test (100% production) <sup>(7)</sup> ,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}} = V_{\text{pd}(\text{m})}$ , $t_{\text{ini}} = t_{\text{m}} = 1\text{s}$  | $\leq 5$      |                  |
| $C_{\text{IO}}$  | Barrier capacitance, input to output <sup>(6)</sup>   | $V_{\text{IO}} = 0.5V_{\text{PP}}$ at 1MHz  | $\approx 1.5$ | pF               |
| $R_{\text{IO}}$  | Insulation resistance, input to output <sup>(6)</sup> | $V_{\text{IO}} = 500\text{V}$ at $T_A = 25^\circ\text{C}$   | $> 10^{12}$   | $\Omega$         |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  | $> 10^{11}$   |                  |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $T_S = 150^\circ\text{C}$  | $> 10^9$      |                  |
|  | Pollution degree                                      |   | 2             |                  |
|  | Climatic category                                     |   | 55/125/21     |                  |
| <b>UL1577</b>  |   |   |               |                  |
| $V_{\text{ISO}}$                                       | Withstand isolation voltage                           | $V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{s}$ (100% production test)   | 3000          | $V_{\text{RMS}}$ |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

## 6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  | VALUE         | UNIT             |
|--|---|--|---------------|------------------|
| <b>GENERAL</b>   |   |  |               |                  |
| CLR  | External clearance <sup>(1)</sup>                     | Shortest pin-to-pin distance through air   | $\geq 8.5$    | mm               |
| CPG  | External creepage <sup>(1)</sup>                      | Shortest pin-to-pin distance across the package surface  | $\geq 8.5$    | mm               |
| DTI  | Distance through insulation                           | Minimum internal gap (internal clearance) of the double insulation   | $\geq 15.4$   | $\mu\text{m}$    |
| CTI  | Comparative tracking index                            | DIN EN 60112 (VDE 0303-11); IEC 60112  | $\geq 600$    | V                |
|  | Material group  | According to IEC 60664-1   | I             |                  |
|  | Overvoltage category per IEC 60664-1                  | Rated mains voltage $\leq 300\text{V}_{\text{RMS}}$  | I-IV          |                  |
|  |   | Rated mains voltage $\leq 6000\text{V}_{\text{RMS}}$   | I-III         |                  |
| <b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b> |   |  |               |                  |
| $V_{\text{IORM}}$                                      | Maximum repetitive peak isolation voltage             | At AC voltage  | 2120          | $V_{\text{PK}}$  |
| $V_{\text{IOWM}}$                                      | Maximum-rated isolation working voltage               | At AC voltage (sine wave)  | 1500          | $V_{\text{RMS}}$ |
|  |   | At DC voltage  | 2120          | $V_{\text{DC}}$  |
| $V_{\text{IOTM}}$                                      | Maximum transient isolation voltage                   | $V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1\text{s}$ (100% production test)  | 7000          | $V_{\text{PK}}$  |
| $V_{\text{IMP}}$                                       | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1   | 7700          | $V_{\text{PK}}$  |
| $V_{\text{IOSM}}$                                      | Maximum surge isolation voltage <sup>(4)</sup>        | Tested in oil (qualification test),<br>1.2/50 $\mu\text{s}$ waveform per IEC 62368-1   | 10000         | $V_{\text{PK}}$  |
| $q_{\text{pd}}$  | Apparent charge <sup>(5)</sup>                        | Method a, after input/output safety test subgroups 2 and 3,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$            | $\leq 5$      | pC               |
|  |   | Method a, after environmental tests subgroup 1,<br>$V_{\text{pd}(\text{ini})} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ , $V_{\text{pd}(\text{m})} = 1.6 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$                        | $\leq 5$      |                  |
|  |   | Method b1, at preconditioning (type test) and routine test,<br>$V_{\text{pd}(\text{ini})} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = 1\text{s}$ , $V_{\text{pd}(\text{m})} = 1.875 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1\text{s}$ | $\leq 5$      |                  |
|  |   | Method b2, at routine test (100% production) <sup>(7)</sup><br>$V_{\text{pd}(\text{ini})} = V_{\text{pd}(\text{m})} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = t_{\text{m}} = 1\text{s}$  | $\leq 5$      |                  |
| $C_{\text{IO}}$  | Barrier capacitance, input to output <sup>(6)</sup>   | $V_{\text{IO}} = 0.5\text{V}_{\text{PP}}$ at 1MHz  | $\approx 1.5$ | pF               |
| $R_{\text{IO}}$  | Insulation resistance, input to output <sup>(6)</sup> | $V_{\text{IO}} = 500\text{V}$ at $T_A = 25^\circ\text{C}$  | $> 10^{12}$   | $\Omega$         |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$   | $> 10^{11}$   |                  |
|  |   | $V_{\text{IO}} = 500\text{V}$ at $T_S = 150^\circ\text{C}$   | $> 10^9$      |                  |
|  | Pollution degree                                      |  | 2             |                  |
|  | Climatic category                                     |  | 55/125/21     |                  |
| <b>UL1577</b>  |   |  |               |                  |
| $V_{\text{ISO}}$                                       | Withstand isolation voltage                           | $V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{s}$ (qualification test),<br>$V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{s}$ (100% production test)  | 5000          | $V_{\text{RMS}}$ |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.
- (7) Either method b1 or b2 is used in production.

## 6.9 Safety-Related Certifications (Basic Isolation)

| VDE   | UL  |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17),<br>EN IEC 60747-17,<br>DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ;<br>6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Basic insulation  | Single protection   |
| Certificate number: Pending   | File number: Pending  |

## 6.10 Safety-Related Certifications (Reinforced Isolation)

| VDE   | UL  |
|---|---|
| DIN EN IEC 60747-17 (VDE 0884-17),<br>EN IEC 60747-17,<br>DIN EN IEC 62368-1 (VDE 0868-1),<br>EN IEC 62368-1,<br>IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9 | Recognized under 1577 component recognition and<br>CSA component acceptance NO 5 programs |
| Reinforced insulation   | Single protection   |
| Certificate number: Pending   | File number: Pending  |

## 6.11 Safety Limiting Values (D Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER      |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|---|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current | R <sub>θJA</sub> = 116.5°C/W, VDDx = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 195  | mA   |
| P <sub>S</sub> | Safety input, output, or total power    | R <sub>θJA</sub> = 116.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C              |     |     | 1070 | mW   |
| T <sub>S</sub> | Maximum safety temperature              |  |     |     | 150  | °C   |

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum junction temperature.

P<sub>S</sub> = I<sub>S</sub> × VDD<sub>max</sub>, where VDD<sub>max</sub> is the maximum supply voltage for high-side and low-side.

## 6.12 Safety Limiting Values (DWV Package)

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER      |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|---|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current | R <sub>θJA</sub> = 102.8°C/W, VDDx = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 220  | mA   |
| P <sub>S</sub> | Safety input, output, or total power    | R <sub>θJA</sub> = 102.8°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C              |     |     | 1210 | mW   |
| T <sub>S</sub> | Maximum safety temperature              |  |     |     | 150  | °C   |

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum junction temperature.

P<sub>S</sub> = I<sub>S</sub> × VDD<sub>max</sub>, where VDD<sub>max</sub> is the maximum supply voltage for high-side and low-side.

## 6.13 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{\text{DD1}} = 3.0\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{DD2}} = 3.0\text{V}$  to  $5.5\text{V}$ ,  $V_{\text{REFIN}} = 3.3\text{V}$ ,  $V_{\text{INP}} = -50\text{mV}$  to  $+50\text{mV}$ , and  $V_{\text{INN}} = 0\text{V}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{\text{DD1}} = 5\text{V}$ ,  $V_{\text{DD2}} = 3.3\text{V}$ , and  $V_{\text{REFIN}} = 1.65\text{V}$  (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS  | MIN  | TYP  | MAX        | UNIT                  |                              |
|-----------------------------|--|--|--|------------|-----------------------|------------------------------|
| <b>ANALOG INPUT</b>         |  |  |  |            |                       |                              |
| $C_{\text{IN}}$             | Effective input sampling capacitance                                       |  | 8  |            | pF                    |                              |
| $R_{\text{IN}}$             | Input impedance  |  | 5.3  | 6.3        | k $\Omega$            |                              |
| $I_{\text{INP}}$            | $I_{\text{INP}} = (V_{\text{INP}} - V_{\text{INN}}) = V_{\text{FSR, MAX}}$ |  | 8  |            | $\mu\text{A}$         |                              |
| $I_{\text{INN}}$            | $I_{\text{INN}} = (V_{\text{INP}} - V_{\text{INN}}) = V_{\text{FSR, MAX}}$ |  | -8   |            | $\mu\text{A}$         |                              |
| CMTI                        | $ \text{GND1} - \text{GND2}  = 1\text{kV}$                                 | 150  |  |            | V/ns                  |                              |
| <b>REFERENCE INPUT</b>      |  |  |  |            |                       |                              |
| $R_{\text{REFIN}}$          | Input Impedance  | REFIN to GND2, $V_{\text{REFIN}} = 3.3\text{V}$ , $T_A = 25^\circ\text{C}$   | 65.3   | 76.8       | 88.3                  |                              |
|                             |  | REFIN to GND2, $V_{\text{REFIN}} = 5\text{V}$ , $T_A = 25^\circ\text{C}$   | 62   | 72.9       | 83.9                  |                              |
| $\text{TCR}_{\text{REFIN}}$ | Input Impedance thermal drift  |  | -235   |            | ppm/ $^\circ\text{C}$ |                              |
| <b>ANALOG OUTPUT</b>        |  |  |  |            |                       |                              |
|                             | Nominal Gain   |  | $V_{\text{REFIN}} / 2 /  V_{\text{Clipping}} $ |            | V/V                   |                              |
| $R_{\text{OUT}}$            | Output resistance  |  | <0.2   |            | $\Omega$              |                              |
|                             | Output short-circuit current   | OUT pin, sourcing or sinking, $\text{INN} = \text{INP} = \text{GND1}$ or $\text{VDD1}$ , output shorted to either $\text{GND2}$ or $\text{VDD2}$ | 11   |            | mA                    |                              |
| <b>DC ACCURACY</b>          |  |  |  |            |                       |                              |
| $V_{\text{OS}}$             | Offset voltage <sup>(1) (2)</sup>  | $T_A = 25^\circ\text{C}$ , $\text{INP} = \text{INN} = \text{GND1}$   | -50  | $\pm 4$    | 50                    | $\mu\text{V}$                |
| $\text{TCV}_{\text{OS}}$    | Offset drift <sup>(1) (2) (4)</sup>  |  | -1   | $\pm 0.15$ | 1                     | $\mu\text{V}/^\circ\text{C}$ |
| $E_{\text{G}}$              | Gain error <sup>(1)</sup>  | $T_A = 25^\circ\text{C}$   | -0.2%  | $\pm 0.04$ | 0.2%                  |                              |
| $\text{TCE}_{\text{G}}$     | Gain drift <sup>(1) (5)</sup>  |  | -45  | $\pm 5$    | 45                    | ppm/ $^\circ\text{C}$        |
|                             | Nonlinearity <sup>(1)</sup>  |  | -0.04%   |            | 0.04%                 |                              |
|                             | Nonlinearity <sup>(1)</sup>  |  | -0.04  |            | 0.04                  | %                            |
|                             | Output noise   | $\text{INP} = \text{INN} = \text{GND1}$ , $f_{\text{IN}} = 0\text{Hz}$ , $\text{BW} = 100\text{kHz}$ brickwall filter                            | 270  |            |                       | $\mu\text{V}_{\text{RMS}}$   |
| CMRR                        | Common-mode rejection ratio  | $f_{\text{IN}} = 0\text{Hz}$ , $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$   | -100   |            |                       | dB                           |
|                             |  | $f_{\text{IN}} = 10\text{kHz}$ , $V_{\text{CM min}} \leq V_{\text{CM}} \leq V_{\text{CM max}}$   | -97  |            |                       |                              |
| PSRR                        | Power-supply rejection ratio <sup>(2)</sup>                                | VDD1 DC PSRR, $\text{INP} = \text{INN} = \text{GND1}$ , VDD1 from 3V to 5.5V   | -113   |            |                       | dB                           |
|                             |  | VDD1 AC PSRR, $\text{INP} = \text{INN} = \text{GND1}$ , VDD1 with 10kHz / 100mV ripple   | -94  |            |                       |                              |
|                             |  | VDD2 DC PSRR, $\text{INP} = \text{INN} = \text{GND1}$ , VDD2 from 3V to 5.5V   | -116   |            |                       |                              |
|                             |  | VDD2 AC PSRR, $\text{INP} = \text{INN} = \text{GND1}$ , VDD2 with 10kHz / 100mV ripple   | -94  |            |                       |                              |
| <b>AC ACCURACY</b>          |  |  |  |            |                       |                              |
| BW                          | Output bandwidth   |  | 220  | 295        |                       | kHz                          |
| THD                         | Total harmonic distortion <sup>(3)</sup>                                   | $f_{\text{IN}} = 10\text{kHz}$   |  | -80        |                       | dB                           |
| SNR                         | Signal-to-noise ratio  | $f_{\text{IN}} = 1\text{ kHz}$ , $\text{BW} = 10\text{kHz}$  | 80   | 84         |                       | dB                           |
|                             | Signal-to-noise ratio  | $f_{\text{IN}} = 10\text{kHz}$ , $\text{BW} = 100\text{kHz}$   |  | 75         |                       |                              |
| <b>POWER SUPPLY</b>         |  |  |  |            |                       |                              |

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $VDD1 = 3.0\text{V}$  to  $5.5\text{V}$ ,  $VDD2 = 3.0\text{V}$  to  $5.5\text{V}$ ,  $V_{REFIN} = 3.3\text{V}$ ,  $V_{INP} = -50\text{mV}$  to  $+50\text{mV}$ , and  $V_{INN} = 0\text{V}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $VDD1 = 5\text{V}$ ,  $VDD2 = 3.3\text{V}$ , and  $V_{REFIN} = 1.65\text{V}$  (unless otherwise noted)

| PARAMETER          |  | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|--------------------|--|-----------------|-----|------|-----|------|
| IDD1               | High-side supply current                   |                 |     | 5.6  | 6.9 | mA   |
| IDD2               | Low-side supply current                    |                 |     | 5.0  | 7.6 | mA   |
| VDD1 <sub>UV</sub> | High-side undervoltage detection threshold | VDD1 rising     | 2.5 | 2.6  | 2.7 | V    |
|                    |  | VDD1 falling    | 1.9 | 2.0  | 2.1 |      |
| VDD2 <sub>UV</sub> | Low-side undervoltage detection threshold  | VDD2 rising     | 2.3 | 2.5  | 2.7 | V    |
|                    |  | VDD2 falling    | 1.9 | 2.05 | 2.2 |      |

- (1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:  

$$TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$$
 where  $V_{OS,MAX}$  and  $V_{OS,MIN}$  refer to the maximum and minimum  $V_{OS}$  values measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:  

$$TCE_G \text{ (ppm)} = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$$
 where  $E_{G,MAX}$  and  $E_{G,MIN}$  refer to the maximum and minimum  $E_G$  values (in %) measured within the temperature range ( $-40$  to  $125^\circ\text{C}$ ).

## 6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|-----------|--|---|-----|-----|-----|---------------|
| $t_r$     | Output signal rise time                          |   |     | 1.7 |     | $\mu\text{s}$ |
| $t_f$     | Output signal fall time                          |   |     | 1.7 |     | $\mu\text{s}$ |
|           | $V_{INX}$ to $V_{OUTX}$ signal delay (50% - 10%) | Unfiltered output   | 0.8 | 1.3 |     | $\mu\text{s}$ |
|           | $V_{INX}$ to $V_{OUTX}$ signal delay (50% - 50%) | Unfiltered output   | 1.6 | 2.1 |     | $\mu\text{s}$ |
|           | $V_{INX}$ to $V_{OUTX}$ signal delay (50% - 90%) | Unfiltered output   | 2.5 | 3   |     | $\mu\text{s}$ |
| $t_{AS}$  | Analog settling time                             | $VDD1$ step to $3.0\text{V}$ with $VDD2 \geq 3.0\text{V}$ , $V_{REFIN} = 3.3\text{V}$ , to $V_{OUT}$ valid, 0.1% settling | 30  | 100 |     | $\mu\text{s}$ |

## 6.15 Timing Diagram

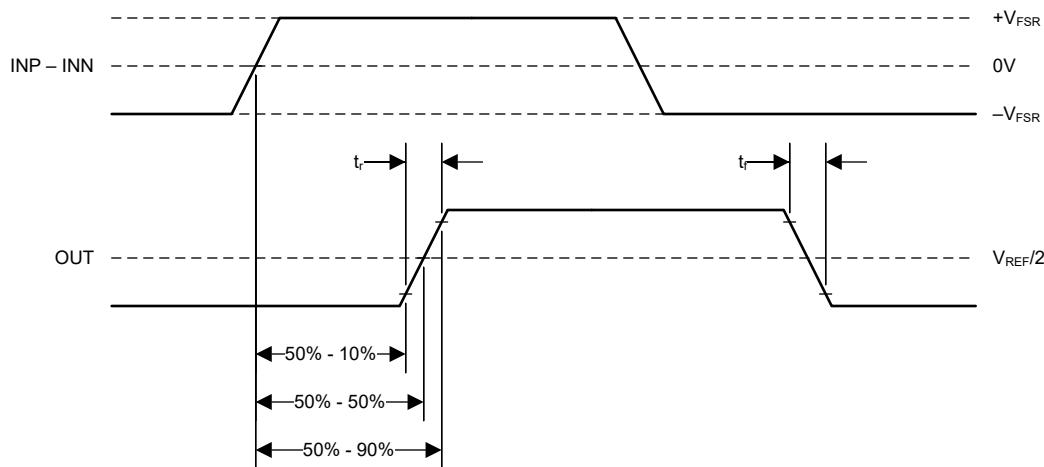


Figure 6-1. Rise, Fall, and Delay Time Waveforms

## 6.16 Insulation Characteristics Curves

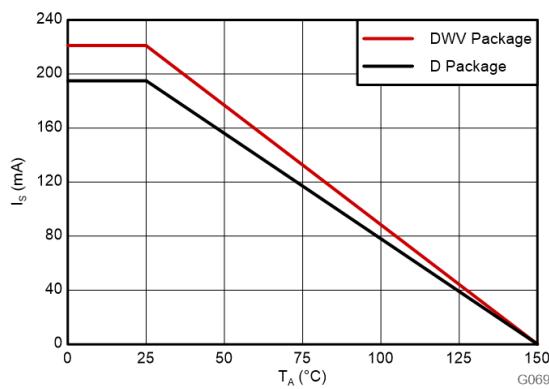


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

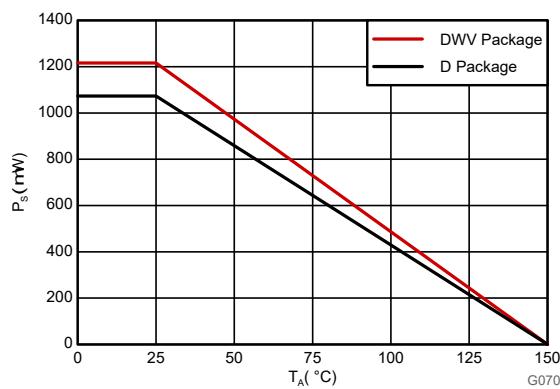
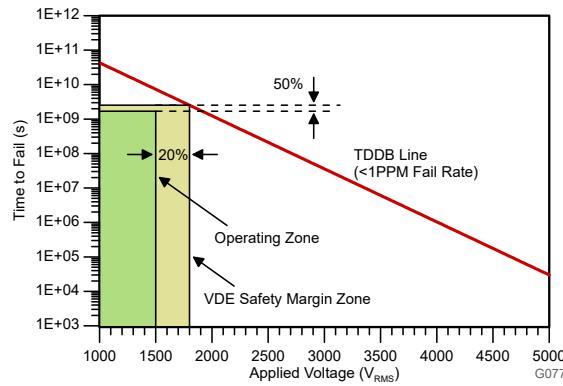
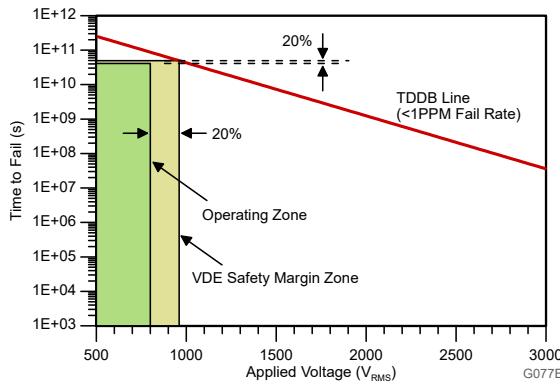


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



$T_A$  up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V<sub>RMS</sub>, projected operating lifetime  $\geq$  50 years

Figure 6-4. Isolation Capacitor Lifetime Projection (Reinforced Isolation)



$T_A$  up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 800V<sub>RMS</sub>, projected operating lifetime  $>> 100$  years

Figure 6-5. Isolation Capacitor Lifetime Projection (Basic Isolation)

## 6.17 Typical Characteristics

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

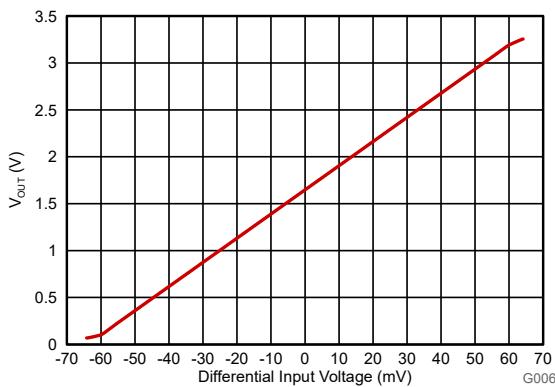
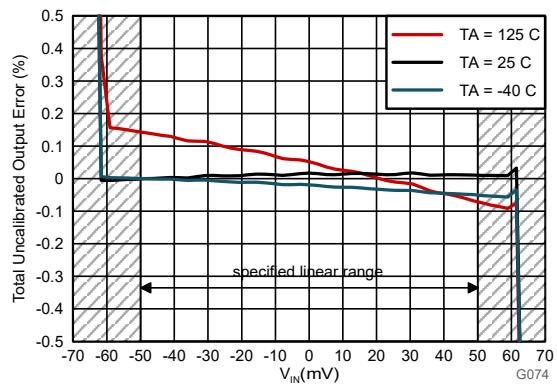


Figure 6-6. Output Voltage vs Input Voltage



Total uncalibrated output error is defined as:  $((V_{OUT\_Measured} - V_{OUT\_Expected}) / V_{REFIN}) \times 100$ , where  $V_{OUT\_Expected} = V_{IN} / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2$ ,  $V_{REFIN} = 3.3V$  and  $V_{Clipping} = 0.064V$

Figure 6-7. Unadjusted Error vs Input Voltage

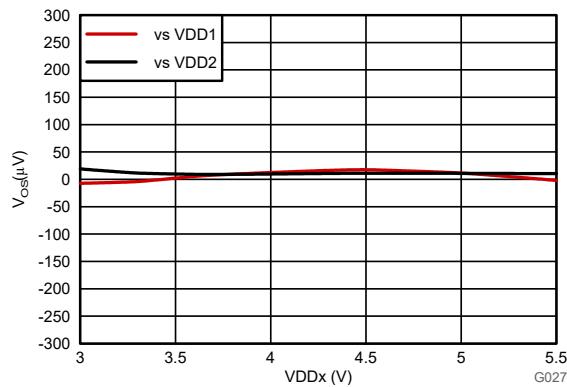


Figure 6-8. Input Offset Voltage vs Supply Voltage

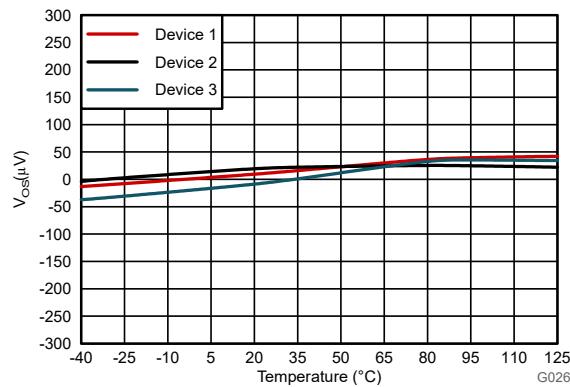


Figure 6-9. Input Offset Voltage vs Temperature

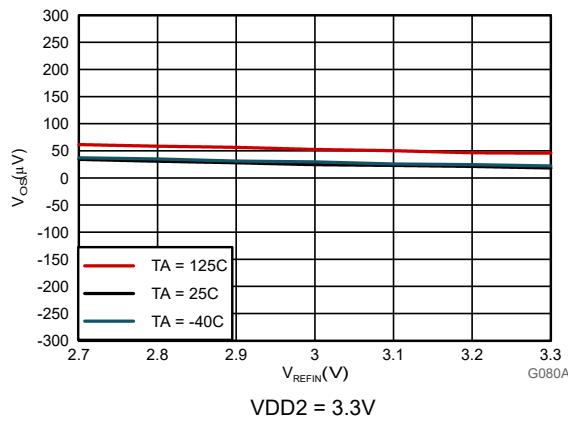


Figure 6-10. Input Offset Voltage vs VREFIN

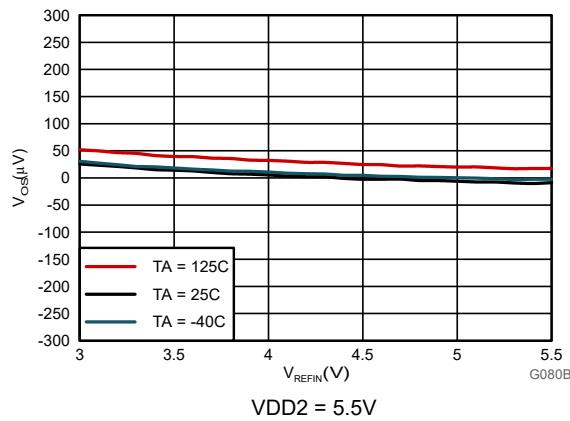
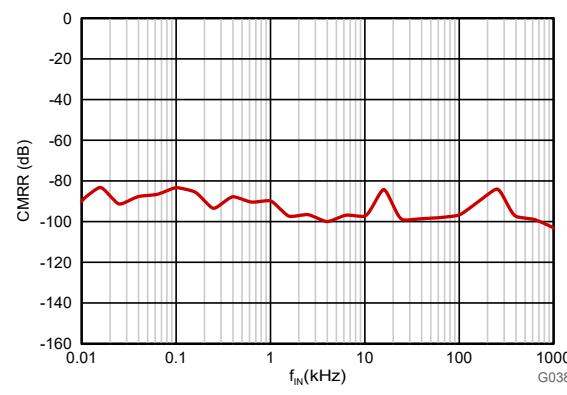
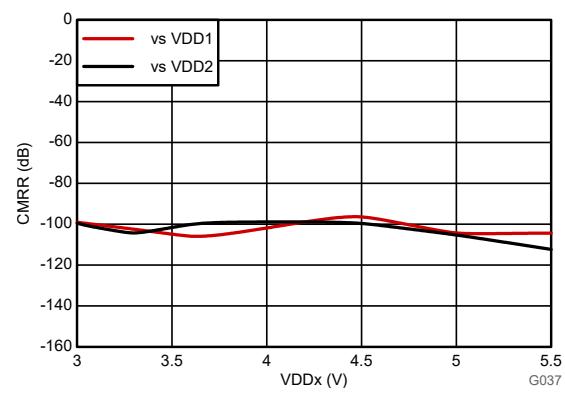
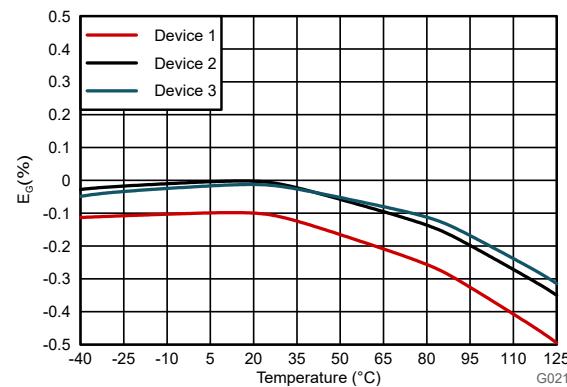
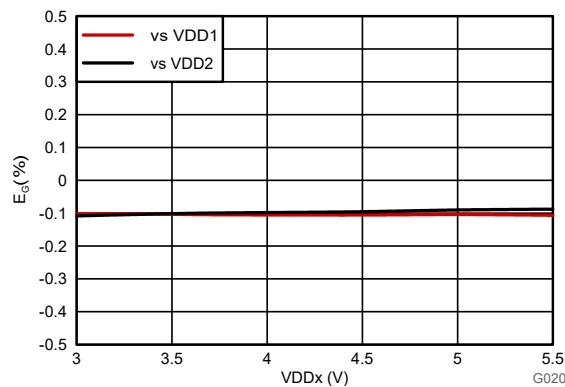
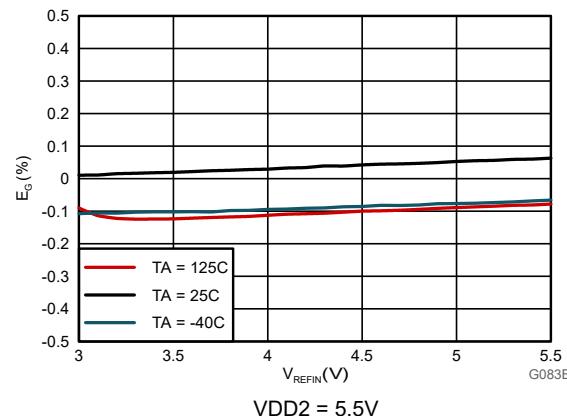
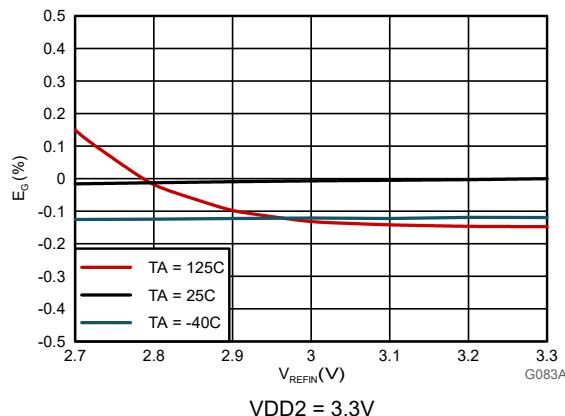


Figure 6-11. Input Offset Voltage vs VREFIN

## 6.17 Typical Characteristics (continued)

at  $VDD1 = 5V$ ,  $VDD2 = 3.3V$ ,  $VREFIN = 3.3V$ ,  $VINP = -50mV$  to  $50mV$ ,  $VINN = 0V$ , and  $f_{IN} = 10kHz$  (unless otherwise noted)



## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and  $f_{IN} = 10\text{kHz}$  (unless otherwise noted)

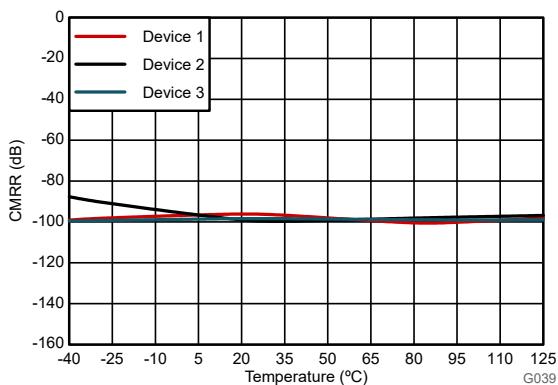


Figure 6-18. Common-Mode Rejection Ratio vs Temperature

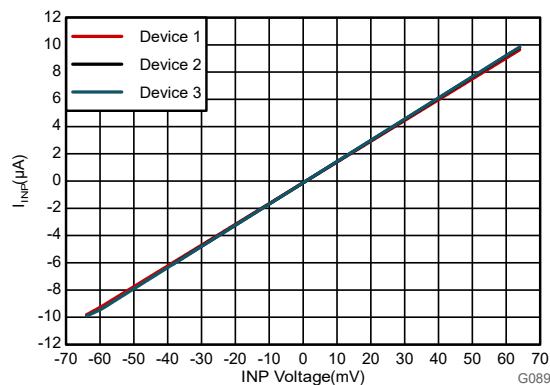


Figure 6-19. Input Current vs Input Voltage

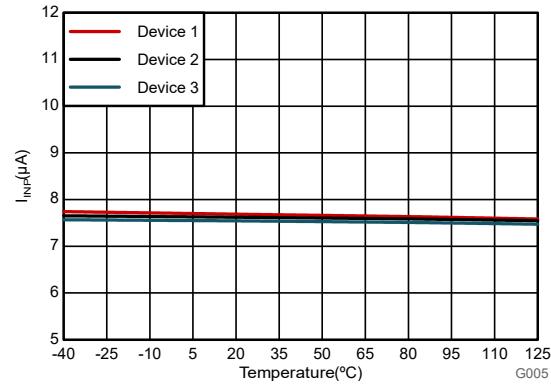


Figure 6-20. Input Current vs Temperature

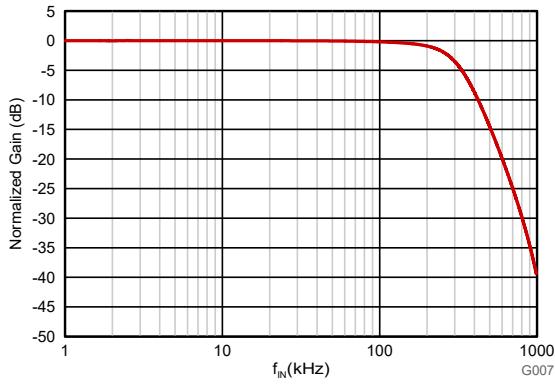


Figure 6-21. Normalized Gain vs Input Frequency

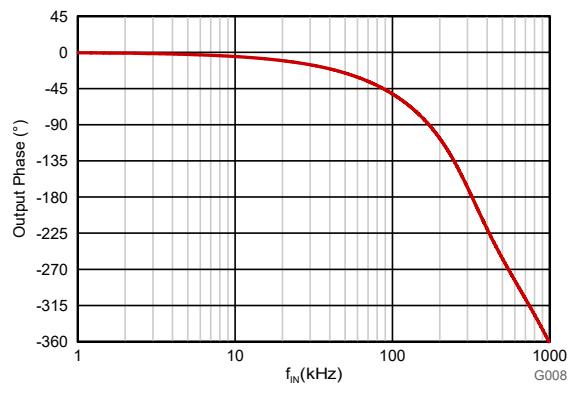


Figure 6-22. Output Phase vs Input Frequency

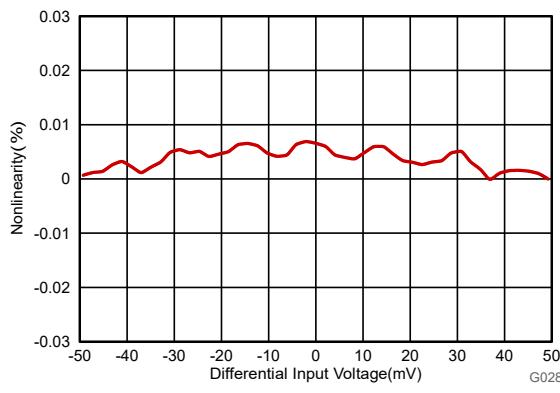


Figure 6-23. Nonlinearity vs Input Voltage

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

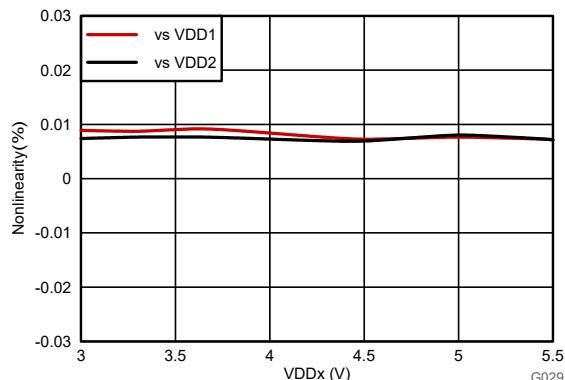


Figure 6-24. Nonlinearity vs Supply Voltage

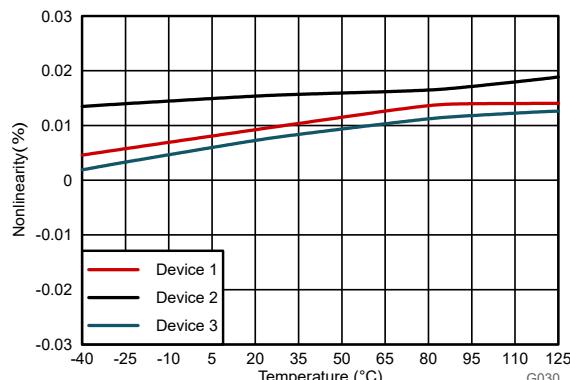


Figure 6-25. Nonlinearity vs Temperature

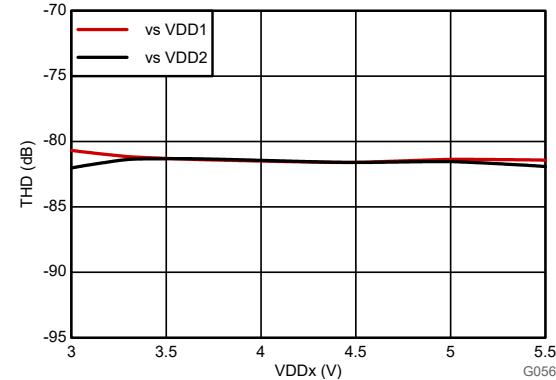


Figure 6-26. Total Harmonic Distortion vs Supply Voltage

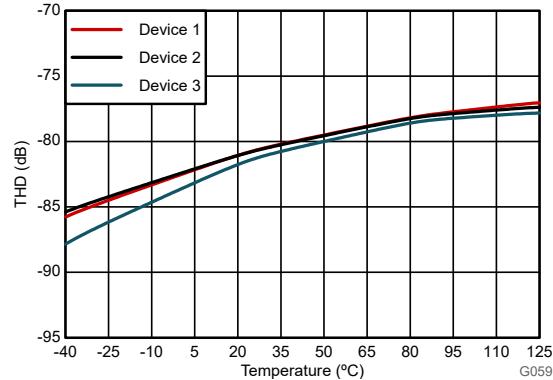


Figure 6-27. Total Harmonic Distortion vs Temperature

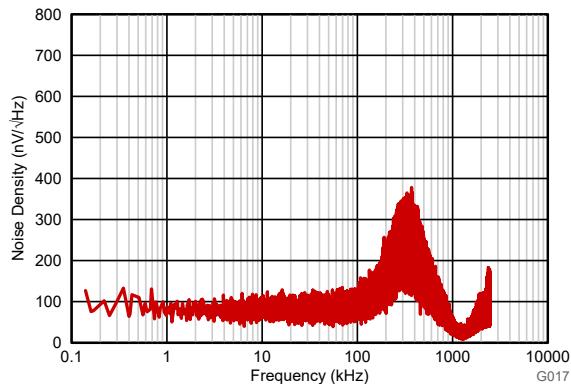


Figure 6-28. Input-Referred Noise Density vs Frequency

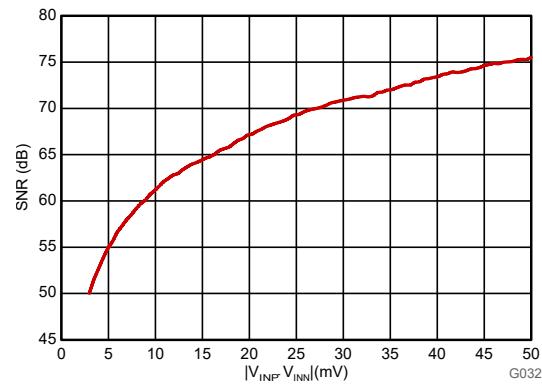


Figure 6-29. Signal-to-Noise Ratio vs Input Voltage

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

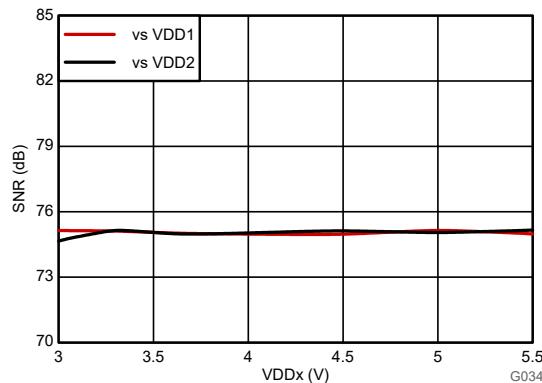


Figure 6-30. Signal-to-Noise Ratio vs Supply Voltage

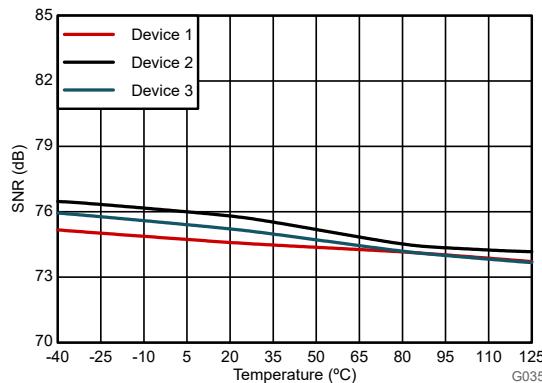


Figure 6-31. Signal-to-Noise Ratio vs Temperature

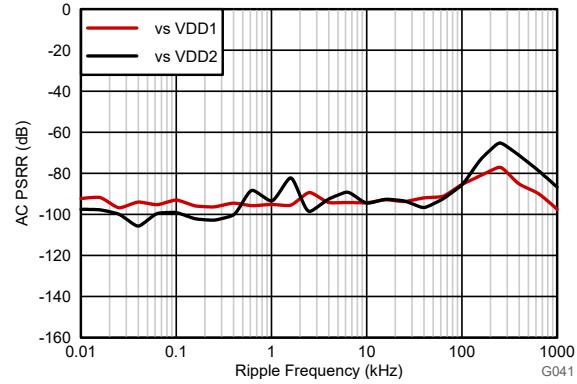


Figure 6-32. Power-Supply Rejection Ratio vs Ripple Frequency

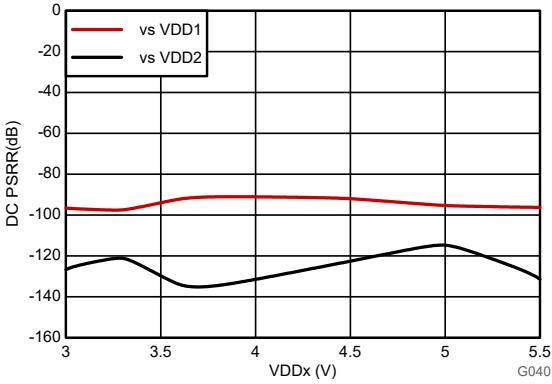


Figure 6-33. Power-Supply Rejection Ratio vs Supply Voltage

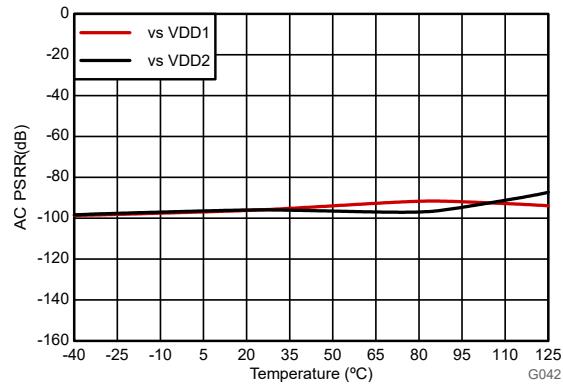


Figure 6-34. Power-Supply Rejection Ratio vs Temperature

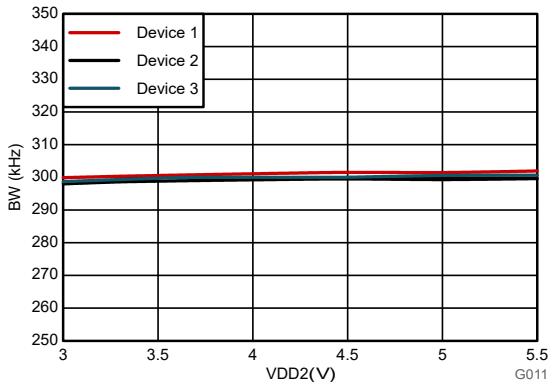


Figure 6-35. Output Bandwidth vs Low-Side Supply Voltage

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

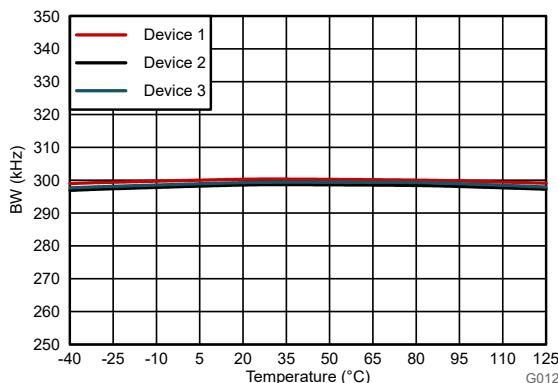


Figure 6-36. Output Bandwidth vs Temperature

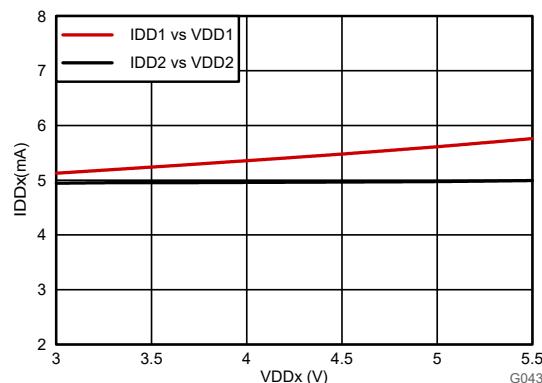


Figure 6-37. Supply Current vs Supply Voltage

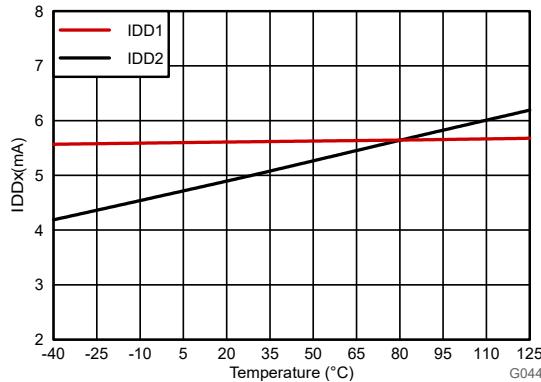


Figure 6-38. Supply Current vs Temperature

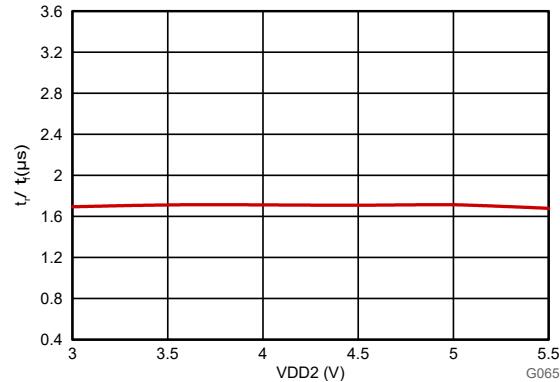


Figure 6-39. Output Rise and Fall Time vs Low-Side Supply

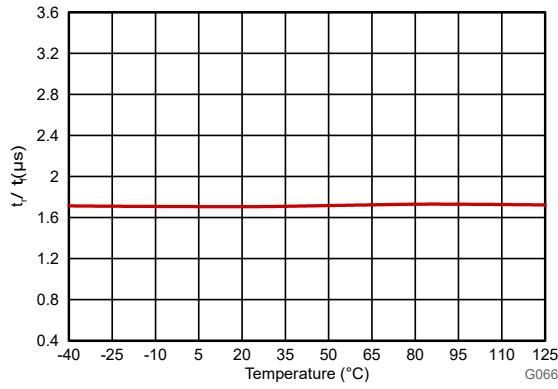


Figure 6-40. Output Rise and Fall Time vs Temperature

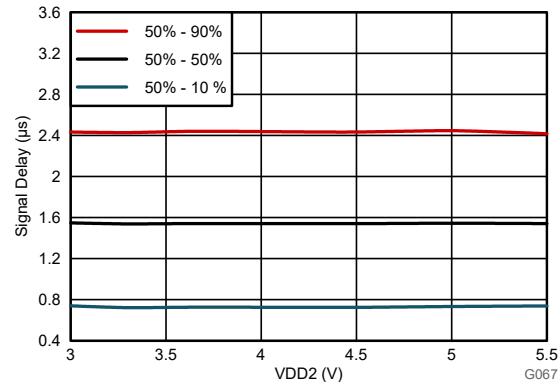


Figure 6-41. V<sub>IN</sub> to V<sub>OUT</sub> Signal Delay vs Low-Side Supply Voltage

## 6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f<sub>IN</sub> = 10kHz (unless otherwise noted)

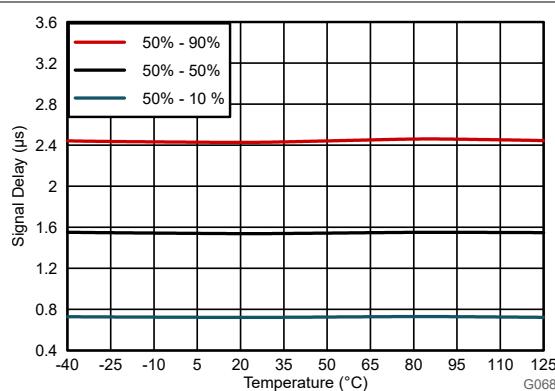


Figure 6-42. V<sub>IN</sub> to V<sub>OUT</sub> Signal Delay vs Temperature

## 7 Detailed Description

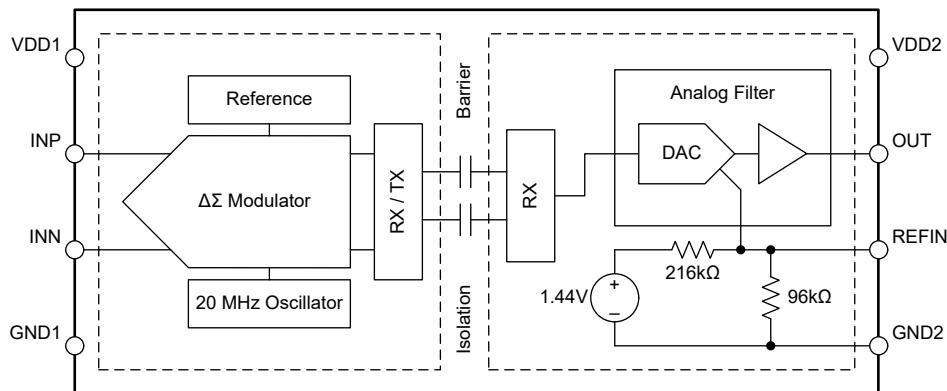
### 7.1 Overview

The AMC0x02R is a precision, galvanically isolated amplifier with a  $\pm 50\text{mV}$ , differential input and single-ended, ratiometric output. The input stage of the device drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The full-scale output voltage of the isolated amplifier is equal to the voltage applied to the REFIN pin.

The  $\text{SiO}_2$ -based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#). The digital modulation used in the AMC0x02R transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

### 7.2 Functional Block Diagram

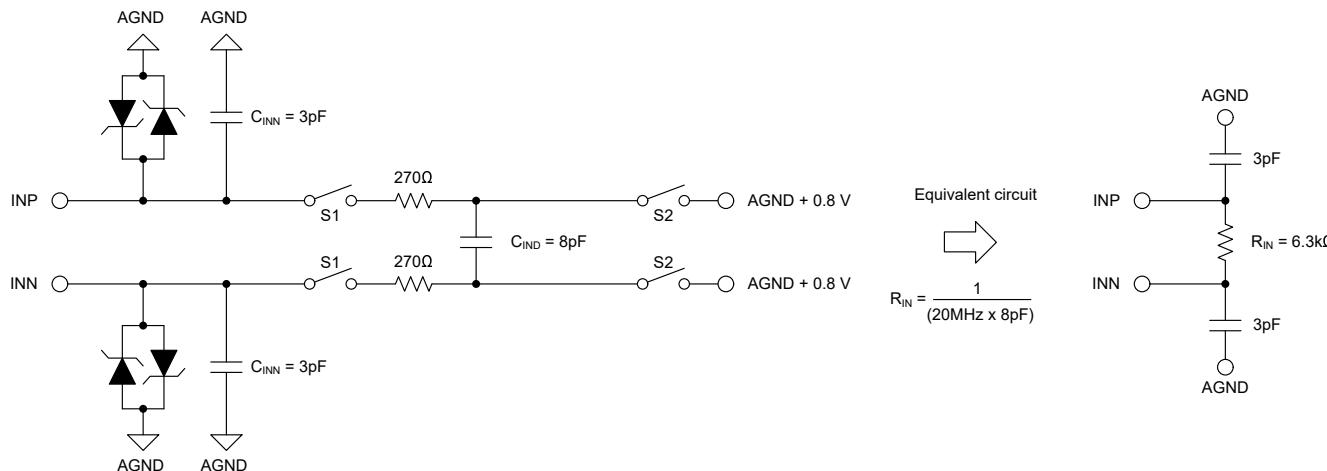


### 7.3 Feature Description

#### 7.3.1 Analog Input

As shown in [Figure 7-1](#), input of the AMC0x02R has a fully differential, switched-capacitor circuit with a dynamic input impedance of  $6.3\text{k}\Omega$ .

The sampling capacitor is continuously charged and discharged with a frequency of 20MHz. With the S1 switches closed,  $C_{IND}$  charges to the voltage difference across  $V_{INP}$  and  $V_{INN}$ . For the discharge phase, both S1 switches open first and then both S2 switches close.  $C_{IND}$  discharges to approximately  $AGND + 0.8\text{V}$  during this phase.



**Figure 7-1. Equivalent Input Circuit**

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. There are two restrictions on the analog input signals (INP and INN).

- First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, limit the input current to the absolute maximum value. This is to prevent device input electrostatic discharge (ESD) diode damage due to high current.
- Second, keep the differential analog input voltage within the specified full-scale range ( $V_{FSR}$ ) and input common-mode voltage range ( $V_{CM}$ ) ranges.  $V_{FSR}$  and  $V_{CM}$  are specified in the *Recommended Operating Conditions* table. The device noise and linearity performance is guaranteed only in this range.

### 7.3.2 Isolation Channel Signal Transmission

As shown in [OOK-Based Modulation Scheme](#), the AMC0x02R uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the  $\text{SiO}_2$ -based isolation barrier. The transmit driver (TX) is illustrated in the [Functional Block Diagram](#). TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital one. However, TX does not send a signal to represent a digital zero. The nominal frequency of the carrier used inside the AMC0x02R is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0x02R transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

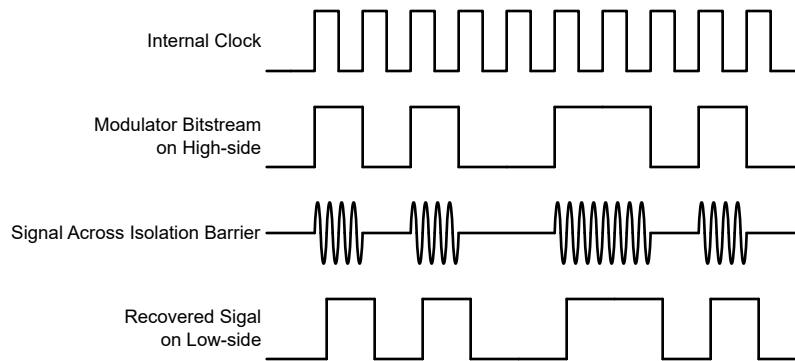


Figure 7-2. OOK-Based Modulation Scheme

### 7.3.3 Analog Output

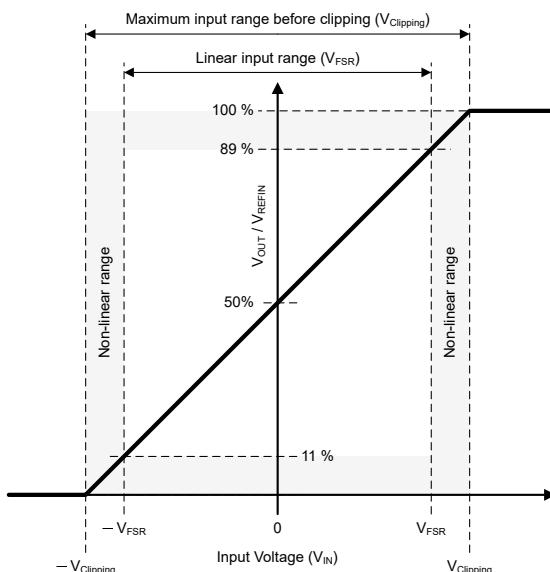
The AMC0x02R provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The full-scale output voltage is set by the REFIN pin. For any input voltage within the specified linear input range, the device outputs a voltage equal to:

$$V_{OUT} = V_{IN} / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 = (V_{IN} - V_{INN}) / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 \quad (1)$$

Connect REFIN to the same reference voltage as a downstream ADC to match the ADC dynamic input voltage range. With a shared reference voltage, the ADC outputs a negative full-scale code when the negative clipping voltage is applied to the input of the AMC0x02R. The ADC outputs the mid-range code when 0V is applied to the input of the AMC0x02R. The ADC outputs a positive full-scale code when the positive clipping voltage is applied to the input of the AMC0x02R.

The device is linear within the specified linear full-scale range. Beyond the linear full-scale range, the output continues to follow the input, but with reduced linearity performance. The output clips when the input voltage reaches the clipping voltage. [Figure 7-3](#) shows the input-to-output transfer characteristic.



**Figure 7-3. Input-to-Output Transfer Curve of the AMC0x02R**

### 7.4 Device Functional Modes

The AMC0x02R operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the  $V_{DD2_{UV}}$  threshold. The device is not responsive. OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating conditions. The high-side supply (VDD1) is below the  $V_{DD1_{UV}}$  threshold. The OUT pin is driven to  $V_{REFIN} / 2$ .
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage  $V_{IN}$  is above the maximum clipping voltage  $V_{Clipping, MAX}$ . The device outputs  $V_{REFIN}$  at the OUT pin.
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage  $V_{IN}$  is below the minimum clipping voltage  $V_{Clipping, MIN}$ . The OUT pin is driven to GND2.
- Normal operation: VDD1, VDD2, and  $V_{IN}$  are within the recommended operating conditions. The device outputs a voltage that is proportional to the input voltage.

Table 7-1 lists the operating modes.

**Table 7-1. Device Operational Modes**

| OPERATING CONDITION      | VDD1                      | VDD2                      | V <sub>IN</sub>                              | DEVICE RESPONSE   |
|--------------------------|---------------------------|---------------------------|--|---|
| Off                      | Don't care                | VDD2 < VDD2 <sub>UV</sub> | Don't care                                   | OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes. |
| Missing high-side supply | VDD1 < VDD1 <sub>UV</sub> | Valid <sup>(1)</sup>      | Don't care                                   | The OUT pin is driven to V <sub>REFIN</sub> / 2.  |
| Input overrange          | Valid <sup>(1)</sup>      | Valid <sup>(1)</sup>      | V <sub>IN</sub> > V <sub>Clipping, MAX</sub> | The device outputs V <sub>REFIN</sub> at the OUT pin.                                       |
| Input underrange         | Valid <sup>(1)</sup>      | Valid <sup>(1)</sup>      | V <sub>IN</sub> < V <sub>Clipping, MIN</sub> | The OUT pin is driven to GND2.  |
| Normal operation         | Valid <sup>(1)</sup>      | Valid <sup>(1)</sup>      | Valid <sup>(1)</sup>                         | The device outputs a voltage that is proportional to the input voltage.                     |

(1) *Valid* denotes operation within the recommended operating conditions.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

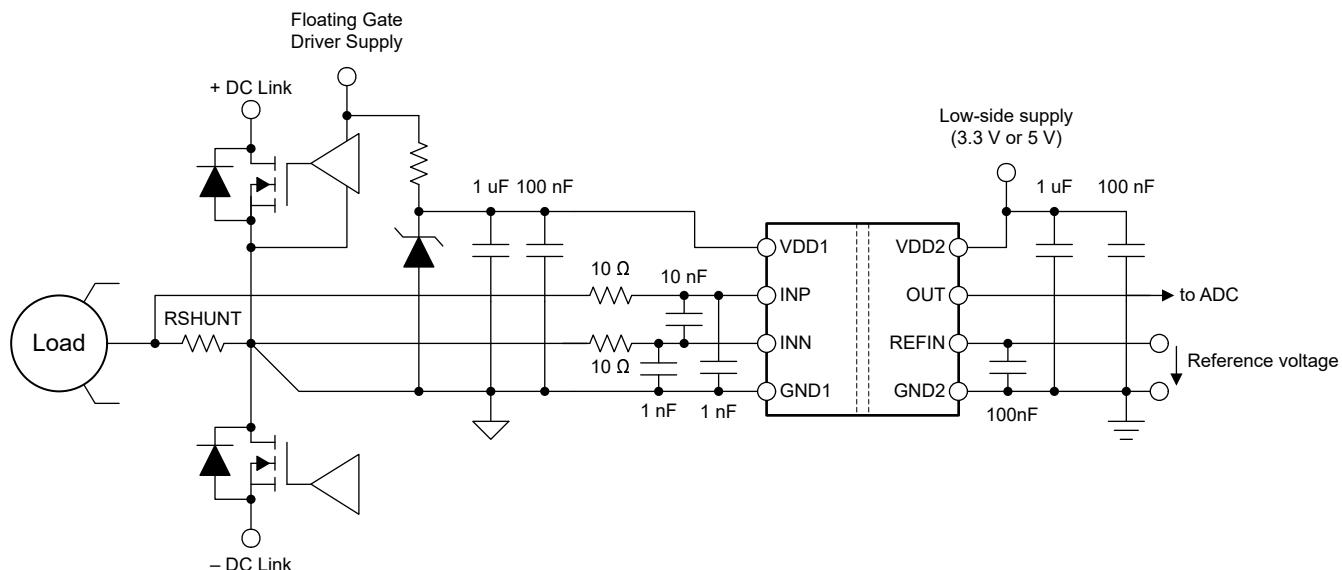
### 8.1 Application Information

The AMC0x02R has low analog input voltage range, high accuracy, low temperature drift, and high common-mode transient immunity. The AMC0x02R is primarily designed for shunt-based current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC0x02R is preferred for isolated current sensing in motor drives, frequency inverters, and uninterruptible power-supply applications.

### 8.2 Typical Application

The following image shows the AMC0x02R in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop. The AMC0x02R high-side circuitry senses the voltage drop across the shunt resistor, then digitizes and transfers data across the isolation barrier to the low side. Low-side circuitry reconstructs the digitized data into an analog signal and provides the signal as single-ended ratiometric voltage on the output pin.

The differential input, single-ended ratiometric output, and high common-mode transient immunity (CMTI) of the AMC0x02R provide reliable and accurate operation even in high-noise environments.



**Figure 8-1. Using the AMC0x02R for Current Sensing in a Typical Application**

### 8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

**Table 8-1. Design Requirements**

| PARAMETER  | VALUE                       |
|--|-----------------------------|
| High-side supply voltage                         | 3.3V or 5V                  |
| Low-side supply voltage                          | 3.3V or 5V                  |
| Voltage drop across RSHUNT for a linear response | $\pm 50\text{mV}$ (maximum) |

### 8.2.2 Detailed Design Procedure

In the *Typical Application* figure, the high-side power supply (VDD1) for the AMC0x02R is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC0x02R (INN). If a four-pin shunt is used, the inputs of the AMC0x02R are connected to the inner leads. GND1 is then connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. Do not short GND1 to INN directly at the device input; see the *Layout Example* section for more details.

Use Ohm's Law to calculate the voltage drop across the shunt resistor ( $V_{\text{SHUNT}}$ ) for the desired measured current:

$$V_{\text{SHUNT}} = I \times R_{\text{SHUNT}} \quad (2)$$

Select a RSHUNT value to satisfy the following two conditions:

- First, the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range of  $V_{\text{SHUNT}} \leq \pm 50\text{mV}$ .
- Secondly, the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output. Keep  $V_{\text{SHUNT}} \leq V_{\text{Clipping}}$ .

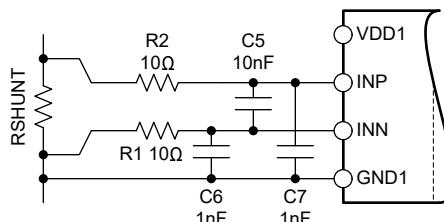
#### 8.2.2.1 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20MHz) of the  $\Delta\Sigma$  modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

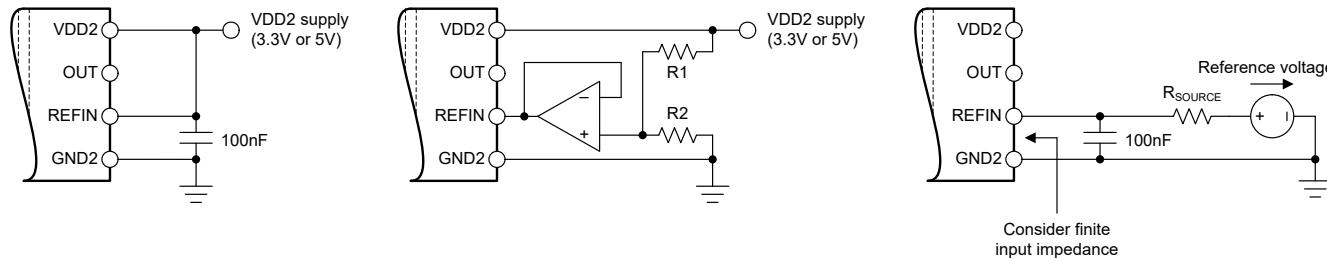
For most applications, the structure shown in Figure 8-2 achieves excellent performance.



**Figure 8-2. Input Filter**

### 8.2.2.2 Connecting the REFIN Pin

The reference input has a finite input impedance as shown in the *Functional Block Diagram*. Consider this impedance when driving the REFIN pin from a high-impedance source. Connect a 100nF capacitor from REFIN to GND2 to filter out high-frequency noise at the reference input. Figure 8-3 shows different options for connecting the REFIN pin.



**Figure 8-3. Connecting the REFIN Pin**

In the first example, REFIN is shorted to VDD2. In the second example,  $V_{REFIN}$  is derived from VDD2 through a buffered resistive divider. In the third example, an external voltage source drives the reference input pin.

### 8.2.3 Application Curves

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC0x02R.

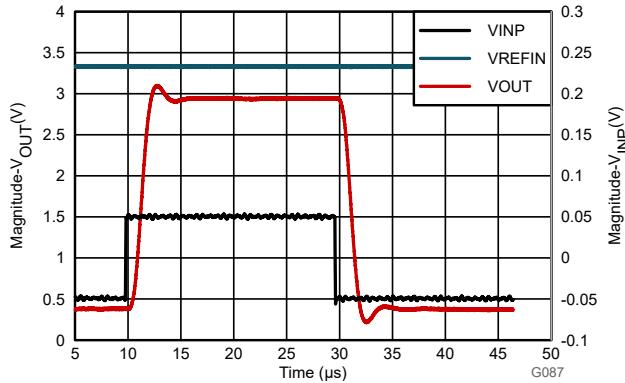


Figure 8-4. Output Step Response of the AMC0x02R

Figure 8-5 shows the typical step response of the AMC0x02R when a transient step is applied on its reference input pin with INP and INN connected to GND1.

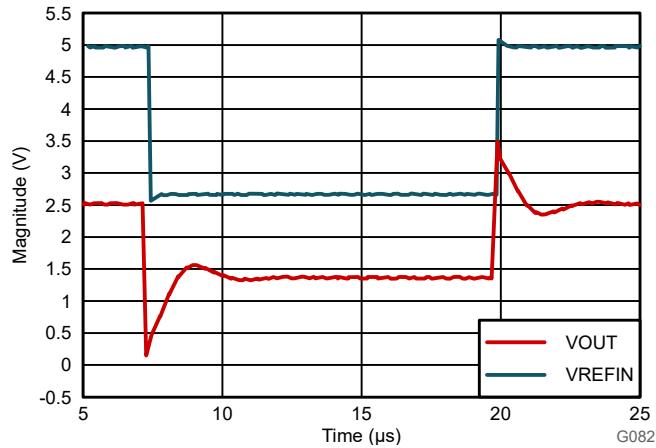


Figure 8-5. Reference Input Step Response of the AMC0x02R

## 8.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the [Layout Example](#) section for more details.

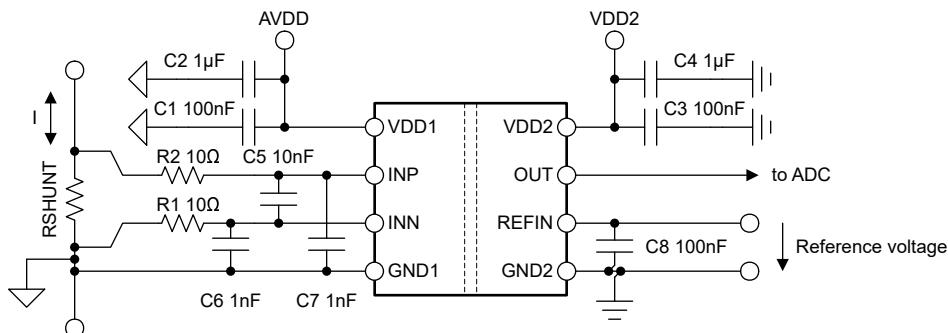
Do not leave the inputs of the AMC0x02R unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current potentially drives the inputs to a positive value that exceeds the operating common-mode input voltage. This condition causes the device to output the fail-safe voltage described in the [Analog Output](#) section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the [Recommended Operating Conditions](#) table.

## 8.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x02R is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver [SN6501](#) and a transformer that supports the desired isolation voltage ratings.

The AMC0x02R does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. [Figure 8-6](#) shows a decoupling diagram for the AMC0x02R.



**Figure 8-6. Decoupling of the AMC0x02R**

Verify capacitors provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

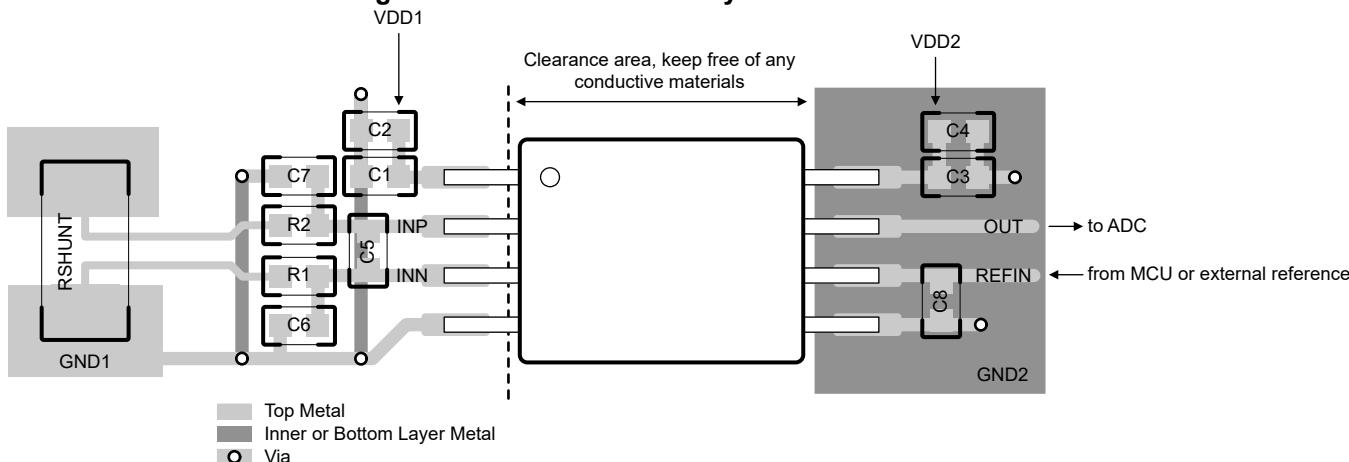
## 8.5 Layout

### 8.5.1 Layout Guidelines

The [Layout Example](#) section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x02R supply pins). This example also depicts the placement of other components required by the device.

### 8.5.2 Layout Example

**Figure 8-7. Recommended Layout of the AMC0x02R**



## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary](#) application report
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity](#) application report
- Texas Instrument, [SN6501 Transformer Driver for Isolated Power Supplies](#) data sheet
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator](#) design tool

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| December 2025 | *        | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| AMC0302RDWVR          | Active        | Production           | null (null)    | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | C0302R              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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