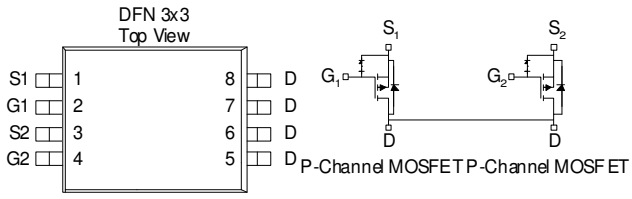
Dual P-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

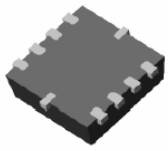
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN 3x3 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.028 @ V_{GS} = -4.5 V	6
	0.045 @ V_{GS} = -2.5V	4.8
	0.078 @ V_{GS} = -1.8V	3.6

Pb-free
RoHS COMPLIANT
HALOGEN FREE



ESD Protected
2000V



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	6	A
	T_A=70°C		4.9	
Pulsed Drain Current[b]		I_{DM}	±40	
Continuous Source Current (Diode Conduction)[a]		I_S	1.5	A
Power Dissipation[a]	T_A=25°C	P_D	1.5	W
	T_A=70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typ**	**Max**	
Maximum Junction-to-Ambient[a]	t <= 10 sec	R_{thJA}	72	83	°C/W
	Steady State		100	120	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

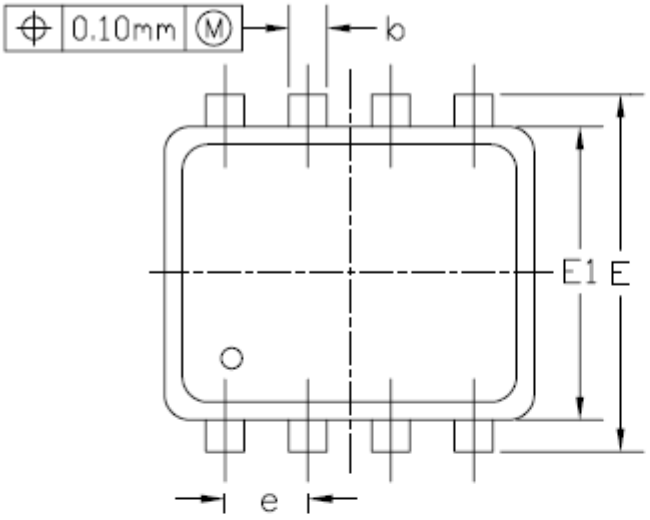
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	-0.3			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			-1	μA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			-10	μA
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	5			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1 A			0.028	Ω
		V_{GS} = 2.5 V, I_D = 1 A			0.045	
		V_{GS} = 1.8 V, I_D = 1 A			0.078	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 10 V, I_D = 1 A		25		S
Diode Forward Voltage[A]	V_{SD}	I_S = 1 A, V_{GS} = 0 V		0.8		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS}=10V, V_{GS}=4.5V, I_D=1A		11		nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			2.9		
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=10V, V_{GS}=4.5V, I_D=1A , R_{GEN}=10Ω		10		nS
Rise Time	t_r			70		
Turn-Off Delay Time	$t_{d(off)}$			100		
Fall-Time	t_f			80		

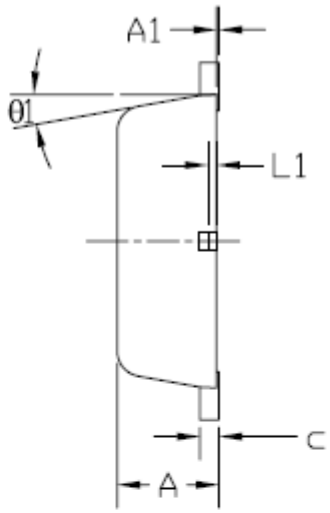
Notes

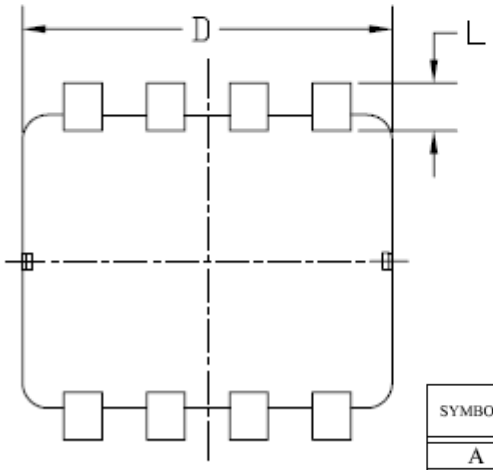
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information







BOTTOM VIEW

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	—	0.05	0.000	—	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.15	0.25	0.003	0.006	0.010
D		2.90 BSC			0.114 BSC	
E		2.80 BSC			0.110 BSC	
E1		2.30 BSC			0.091 BSC	
e		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.45	0.008	0.015	0.018
L1	0.05	—	—	0.002	—	—
θ1	0°	10°	12°	0°	10°	12°