

Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN 3x3 saves board space
- Fast switching speed
- High performance trench technology

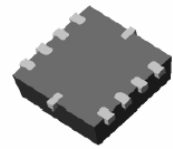
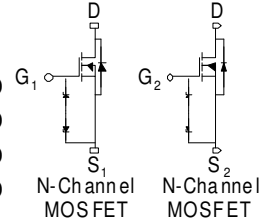
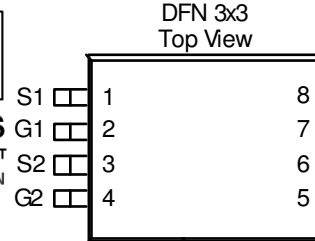
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (OHM)	$I_D$ (A)
20	0.015 @ $V_{GS} = 4.5$ V	8.2
	0.018 @ $V_{GS} = 2.5$ V	7.5



RoHS COMPLIANT HALOGEN FREE



ESD Protected  
2000V



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A=25^\circ\text{C}$	8.2
		$T_A=70^\circ\text{C}$	6.7
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	$\pm 40$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.5	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A=25^\circ\text{C}$	1.5
		$T_A=70^\circ\text{C}$	1.0
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typ	Max	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	72	83
		Steady State	100	120
				$^\circ\text{C/W}$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

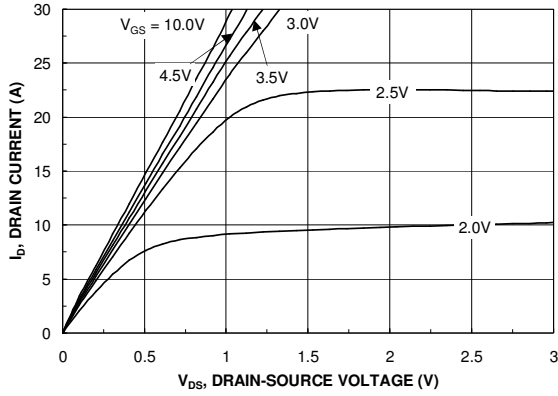
SPECIFICATIONS (T <sub>A</sub> = 25° C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions				Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 uA	0.4			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			10	uA
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	30			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2 A			0.015	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2 A			0.018	
Forward Transconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2 A		25		S
Diode Forward Voltage <sup>A</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2 A, V <sub>GS</sub> = 0 V		0.89		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A		13.4		nC
Gate-Source Charge	Q <sub>gs</sub>			0.9		
Gate-Drain Charge	Q <sub>gd</sub>			2.0		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A , R <sub>GEN</sub> =10Ω		18		nS
Rise Time	t <sub>r</sub>			25		
Turn-Off Delay Time	t <sub>d(off)</sub>			50		
Fall-Time	t <sub>f</sub>			25		

Notes

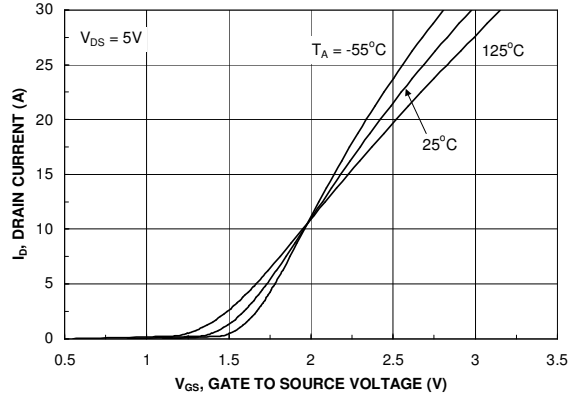
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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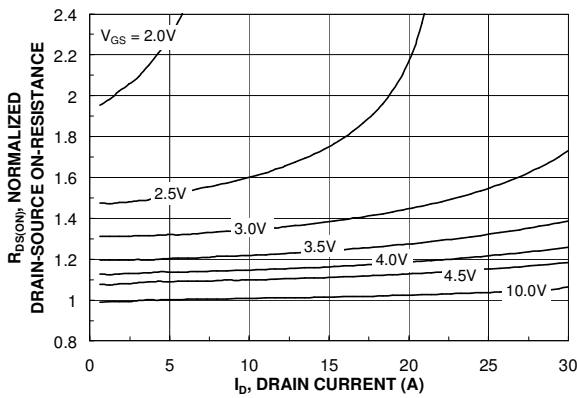
Typical Electrical Characteristics (N-Channel)



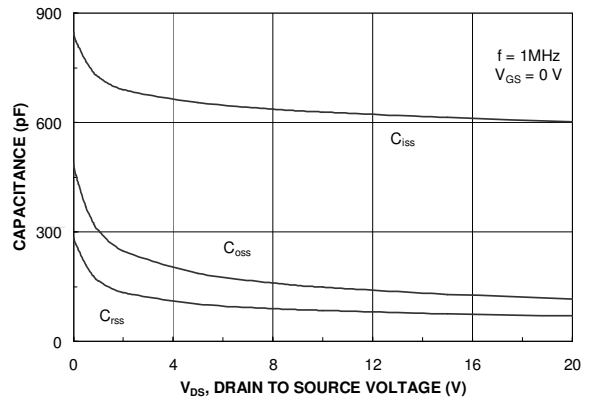
Output Characteristics



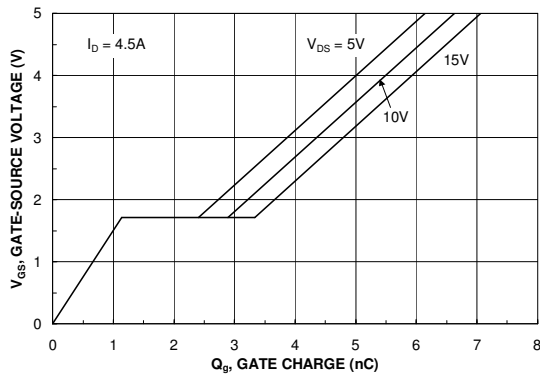
Transfer Characteristics



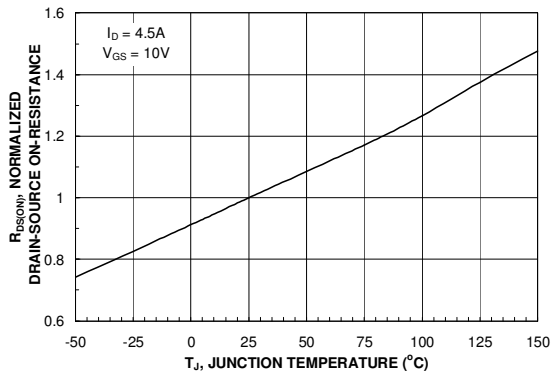
On-Resistance vs. Drain Current



Capacitance

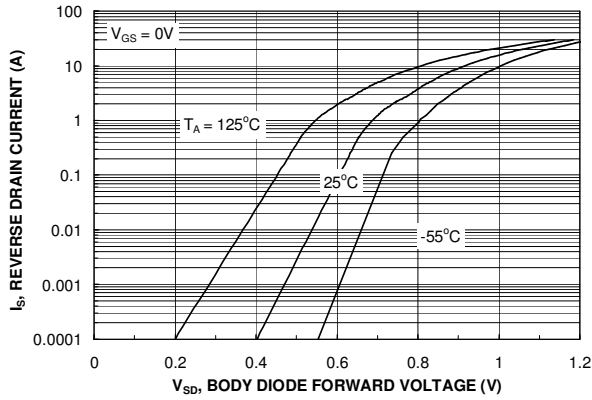


Gate Charge

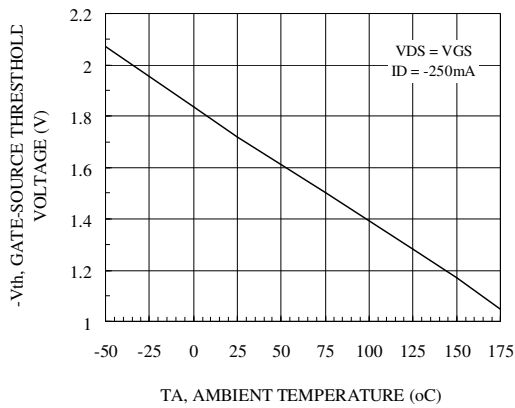


On-Resistance vs. Junction Temperature

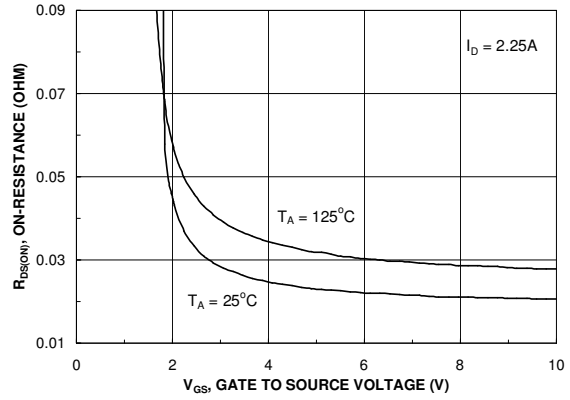
Typical Electrical Characteristics (N-Channel)



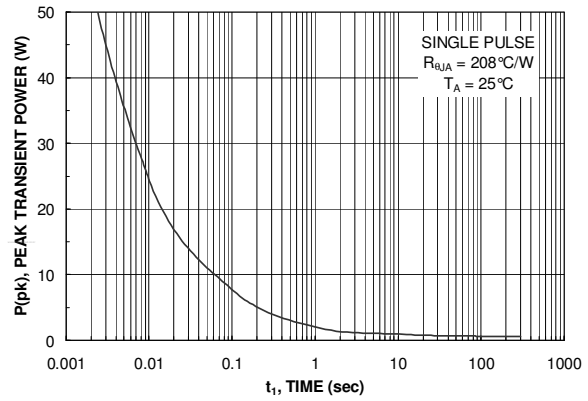
Source-Drain Diode Forward Voltage



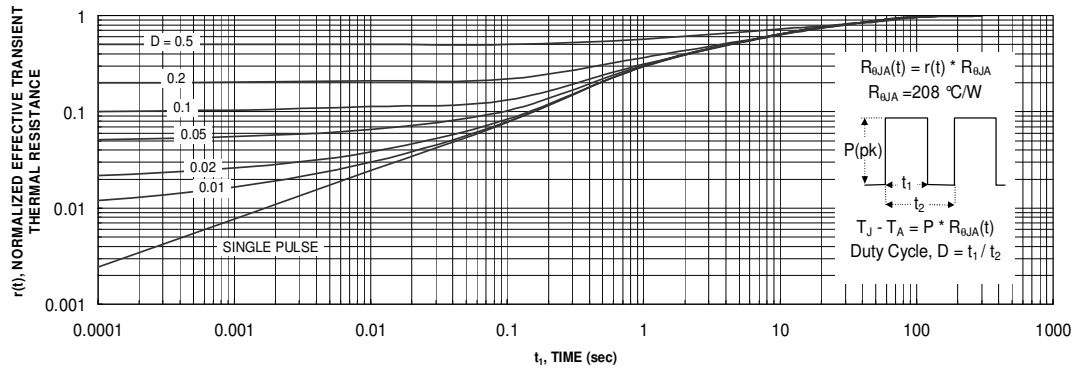
Vth Gate to Source Voltage Vs Temperature



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Junction to Ambient

# Package Information

