Preliminary Information

AMD

AMD-761™ System Controller

Software/BIOS Design Guide

Publication # **24081** Rev: **D**
Issue Date: **February 2002**

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Revision History

Date	Rev	Description
2/2002	D	Text added in the following locations explaining that the registers must be saved and restored when entering and exiting the S3 state: ■ Section 1.1.5 on page 7, 2nd paragraph added ■ Section 4 on page 185, first Note expanded ■ Section 4.4 on page 190, paragraph two added ■ Section 7 on page 211, paragraph added directly after last bullet in bulleted list The following additional changes were incorporated: ■ Table 34 on page 210, values for PSlewXfer and NSlewXfer changed from 01 and 00, respectively, to 11 and 11 ■ Updated "Revision History"
8/2001	C	Public release. Added bidirectional WSC# feature configuration register description.
4/2001	B	Modified descriptions for WSC# and WSC# feature additions. NDA version only.
3/2001	A	Initial public release.

1 Overview

The AMD Athlon™ processor powers the next generation in computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.

The AMD-761™ system controller provides standard Northbridge functionality for desktop personal computers using the AMD Athlon™ family of processors. This functionality includes the processor interface as well as PCI, AGP, and main memory interface implementing state of the art Double Data Rate (DDR) synchronous DRAM technology.

This document provides information typically required for development of the system BIOS and device drivers to properly program the AMD-761 system controller configuration registers. The document is organized as follows:

- Section 1 provides an overview of the general BIOS requirements for initializing the AMD-761 system controller configuration registers.
- Section 2 on page 9 contains a description of all AMD-761 system controller configuration registers.
- Section 3 on page 149 contains additional information on setup of the DDR SDRAM interface configuration registers.
- Section 4 on page 185 contains additional information on configuration of the power management features of the AMD-761 system controller.
- Section 5 on page 195 contains additional information on setup of the PCI bus interface configuration registers.
- Section 6 on page 205 contains additional information on setup of the AGP interface configuration registers.
- Section 7 on page 211 contains a list of recommended settings for many of the AMD-761 system controller configuration registers.

1.1 General BIOS Initialization Requirements

The following sections provide general requirements for BIOS when programming the AMD-761 system controller configuration registers. Note that the register descriptions also include some specific programming notes.

1.1.1 AMD-761™ Configuration Spaces

The AMD-761 system controller contains both I/O and memory-mapped configuration spaces as listed below.

- I/O Mapped Space
  - PCI configuration space address and data (CF8h, CFCh)
    - Host bridge registers mapped in PCI configuration space, device 0, function 0
    - DDR interface PDL and I/O controls mapped in PCI configuration space to device 0, function 1
    - PCI to PCI bridge/AGP registers mapped in PCI configuration space to device 1, function 0
- GART Memory-Mapped Registers
  - Mapped in memory space as defined by the programming of Base Address 1: GART Memory Mapped Register Base

1.1.2 Special Configuration Sequencing Requirements

This section outlines a few cases in the AMD-761 system controller configuration registers that require special handling for proper BIOS programming.

Configuration Cycles Enable

The AMD-761 system controller supports configuration address space as defined by the *PCI Local Bus Specification*, Revision 2.2, which defines a unique 256-byte space that is accessed through two 32-bit index registers mapped in I/O space.

As defined in the PCI specification, configuration cycles are generated on the PCI bus only when bit 31 of the Configuration Address register is set.

Function 1 Space

The configuration registers that control the memory interface's Programmable Delay Lines (PDLs) and I/O drive strengths are mapped to device 0: function 1 in the host bridge. This configuration space is disabled by default and requires a write to the PCI Control register's Func1_En (Dev 0:F0:0x4C, bit 0).

The intent of this separate configuration space is that it is configured at initial power-on, subsequently disabled, and essentially protected from further writes.

- Note that the AMD-761 system controller does not report as a multifunction device (bit 7 is not set in the Header_Type field in the PCI Latency Timer and Header Type register in Dev 0:F0:0x0C).
- Reads to the PCI header that normally occupies offsets 00h–3Fh return all 1s—that is, the normal PCI header registers are not implemented.

Memory-Mapped BARs

Five DWORD registers are accessed by the AMD-761 system controller AGP miniport driver as memory-mapped space. This space is defined by the Base Address 1: GART Memory-Mapped Register Base (Dev 0:F0:0x14), which provides address bits [31:12] of the memory-mapped space. Note that this space is defined as a 4-Kbyte region, hence the lower address bits [11:4] are 0s.

This register must be properly programmed by BIOS to allow the driver to access the memory-mapped space.

Memory Holes

Legacy memory holes are decoded in the normal region of main memory from 640 Kbyte to 1 Mbyte. The AMD-761 system controller does not allow PCI masters to access DRAM in this region unless the EV6_Mode bit is set in the PCI Arbitration Control Register. See "Bit Definitions PCI Arbitration Control (Dev0:F0:0x84)" on page 71.

AGP Override Bits for 4X Rate and Fast Writes

The AGP Status register (Dev 0:F0:0xA4) reports the AMD-761 system controller's capability to support AGP fast writes and the AGP-4X rate. The operating system normally reads these bits along with the same bits in the AGP card's status register, and uses this information to configure the AGP Command register (Dev 0:F0:0xA8) in the AMD-761 system controller and the AGP card.

The AMD-761 system controller provides BIOS the ability to override the reporting of fast write and 4X rate support. This override function is accomplished through a write to a separate register, which is required because the AGP Status register is specified as read-only in the AGP specification.

Refer to Section 6.2 on page 208 for details of this implementation.

Interrupt Pin Control R/W Attributes

The Int_Pin field in the AGP/PCI Interrupt and Bridge Control register (Dev 1:F0:0x3C) is read-only by default and initializes to all 0s. If the BIOS is required to initialize this field to another value, it must first change this field to R/W by setting the Int_Pin_Cntl bit in the Miscellaneous Device 1 Control register (Dev 1:F0:0x40).

The AMD-761 system controller does not use the Int_Pin field internally, the register is provided for software compatibility only.

Silicon Revisions

The reader is advised to read the *AMD-761™ System Controller Revision Guide*, order# 23613, for the most current information for the version of silicon being used. The silicon revision is available by reading the PCI revision ID and Class Code register in Dev 0:F0:0x08.

1.1.3 Power-On Reset Initialization

All of the AMD-761 system controller's configuration registers must be initialized by BIOS after initial power-on, paying especially close attention to the registers that are not initialized to a known value.

The AMD-761 system controller is reset when the Southbridge's PCIRST# pin is asserted, which occurs when transitioning from the Mechanical Off, S5, S4, or S3 sleep states.

To accommodate support of the Advanced Configuration and Power Interface (ACPI) S3 (suspend to RAM) power management state, the registers listed in Table 1 on page 5 are not initialized to a known state after reset (RESET# asserted), and they must be initialized by BIOS after initial power-on for proper operation. These registers retain the value programmed by BIOS after subsequent assertions of the RESET# pin when transitioning to and from the S3 sleep state.

Table 1. AMD-761™ System Controller Configuration Register Bits Unknown at RESET#

Register Name	Offset	Bit Name	Bit(s)
ECC Mode/Status	Dev 0:F0:0x48	SERR_Enable	[15:14]
		ECC_Diag	[12]
		ECC_Mode	[11:10]
DRAM Timing	Dev 0:F0:0x54	SBPWaitState	[31]
		Addr_Timing_A	[30]
		Addr_Timing_A	[29]
		RD_Wait_State	[28]
		Reg_DIMM_En	[27]
		t_{WTR}	[26]
		t_{WR}	[25:24]
		t_{RRD}	[23]
		Idle_Cyc_Limit	[18:16]
		PH_Limit	[15:14]
		t_{RC}	[11:9]
		t_{RP}	[8:7]
		t_{RAS}	[6:4]
		t_{CL}	[3:2]
		t_{RCD}	[1:0]
DRAM Mode/Status	Dev 0:F0:0x58	Burst_Ref_En	[20]
		Ref_Dis	[19]
		Reserved	[18]
		Cyc_Per_Ref	[17:16]
		CS7_X4Mode	[7]
		CS6_X4Mode	[6]
		CS5_X4Mode	[5]
		CS4_X4Mode	[4]
		CS3_X4Mode	[3]
		CS2_X4Mode	[2]
		CS1_X4Mode	[1]
		CS0_X4Mode	[0]
Status/Control	Dev 0:F0:0x70	Self_Ref_En	[18]
Memory Base Address 0–7	Dev 0:F0:0xC0 through Dev 0:F0:0xDC	CS_Base	[31:23]
		CS_Mask	[15:7]
		Addr_Mode	[2:1]
		CS_En	[0]

Table 1. AMD-761™ System Controller Configuration Register Bits Unknown at RESET# (Continued)

Register Name	Offset	Bit Name	Bit(s)
DDR PDL Calibration Control	Dev 0:F1:0x40	SW_Recal	[7]
		Use_Act_Dly	[6]
		Auto_Cal_En	[5]
		Act_Dly_Inh	[4]
		Auto_Cal_Period	[1:0]
DDR PDL Configuration 0–17	Dev 0:F1:0x44 through Dev 0:F1:0x88	Clk_Dly	[31:24]
		SW_Cal_Dly	[23:16]
		Cal_Dly	[15:8]
		Act_Dly	[7:0]
DDR DQS/MDAT Pad Configuration	Dev 0:F1:0x8C	PSlewMDAT	[29:27]
		NSlewMDAT	[26:24]
		PDrvMDAT	[19:18]
		NDrvMDAT	[17:16]
		PSlewDQS	[13:11]
		NSlewDQS	[10:8]
		PDrvDQS	[3:2]
		NDrvDQS	[1:0]
DDR CLK/CS Pad Configuration	Dev 0:F1:0x90	PSlewCLK	[29:27]
		NSlewCLK	[26:24]
		PDrvCLK	[19:18]
		NDrvCLK	[17:16]
		PSlewCS	[13:11]
		NSlewCS	[10:8]
		PDrvCS	[3:2]
		NDrvCS	[1:0]
DDR CMDB/CMDA Pad Configuration	Dev 0:F1:0x94	PSlewCMDB	[29:27]
		NSlewCMDB	[26:24]
		PDrvCMDB	[19:18]
		NDrvCMDB	[17:16]
		PSlewCMDA	[13:11]
		NSlewCMDA	[10:8]
		PDrvCMDA	[3:2]
		NDrvCMDA	[1:0]

Table 1. AMD-761™ System Controller Configuration Register Bits Unknown at RESET# (Continued)

Register Name	Offset	Bit Name	Bit(s)
DDR MAB/MAA Pad Configuration	Dev 0:F1:0x98	PSlewMAB	[29:27]
		NSlewMAB	[26:24]
		PDrvMAB	[19:18]
		NDrvMAB	[17:16]
		PSlewMAA	[13:11]
		NSlewMAA	[10:8]
		PDrvMAA	[3:2]
		NDrvMAA	[1:0]

Refer to Section 7 on page 211 for suggested values for these configuration registers.

1.1.4 Programming Reserved Bits

The AMD-761 system controller has many bits that are specified as reserved and which may be used in future silicon revisions. BIOS must always write a 0 to these bits and not depend on the value read back.

1.1.5 Power Management Considerations

There are several requirements for BIOS initialization of the AMD-761 system controller's configuration register when supporting power management. Refer to Section 4 on page 185 for further details of these requirements.

For any system enabling the S3 state, a number of core logic PCI configuration registers and processor MSRs must be saved or restored prior to suspending or restoring S3. Also, certain hidden bits must be unmasked. These requirements apply to all platforms regardless of segment and whether or not AMD PowerNow!™ is used.

1.2 Recommended AMD Athlon™ Processor SYS_CONFIG Settings

Table 2 provides recommendations for settings in the AMD Athlon processor System Configuration register in systems that utilize the AMD-761 system controller.

Table 2. Recommended Settings for AMD Athlon™ Processor SYSCFG Register

Bit Field	Name	BIOS Setting	Comments
[22]	EvictEn	0	An Evict command, when set, is sent as part of an INVD instruction. The Evict command has no function in the AMD-761™ system controller.
[17]	SysUcLockEn	0	A LockToggle command, when set, is sent as part of a LOCK instruction prefix and certain other instructions. LockToggle has no function in the AMD-761 system controller.
[16]	ChxToDirtyDis	0	The AMD Athlon™ processor and the AMD-761 system controller support Change-To-Dirty commands.
[13]	SysFillValIsD1	0	
[11]	ClVicBlkEn	0	ClVicBlkEn, when set, causes all evicted clean blocks to cause the CleanVictimBlk system interface command. This setting has no function with the AMD-761 system controller.
[10:8]	SetDirtyEnE	0	There are three set-to-dirty enables: SetDirtyEnE, SetDirtyEnO, and SetDirtyEnS. If a given enable is set and a cache block must make a transition from E-to-M, O-to-M, or S-to-M, then the AMD Athlon processor performs the action indicated by the setting of the ChxToDirtyDis field. However, if a given enable is cleared, the processor takes no externally visible action when the desired transition is performed. Change to dirty commands are not needed by the AMD-761 system controller.
	SetDirtyEnO	0	
	SetDirtyEnS	0	

2 AMD-761™ System Controller Programmer's Interface

2.1 Overview

The AMD-760™ chipset supports both x86 and Alpha™ processors that conform to the Socket2000 bus specification. Both processors share a compatible view of system memory and peripherals. Legacy x86 (IBM PC-AT) memory mappings are implemented by x86 processors (AMD Athlon™ processor) as shown in Figure 1.

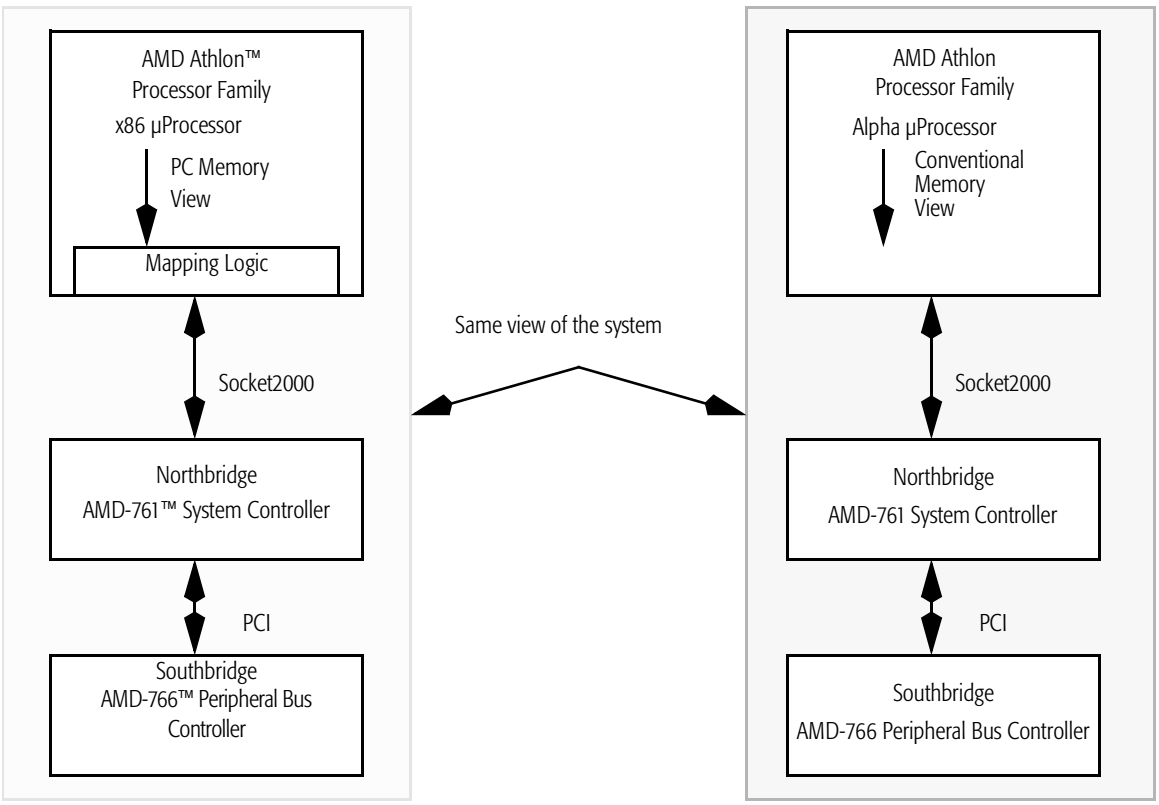

Figure 1. AMD Athlon™ Processor Family Address Mapping

2.2 Address Map

Table 3 shows the address map implemented by the AMD-761™ system controller.

Table 3. AMD-761™ System Controller Socket2000 Memory Map

Address Space Start	Address Space End	Name/Command	Description
SysAddOut MSB=0 & 1 FF000 0000	SysAddOut MSB =0 & 3 FFFF FFFF	Reserved (Masked)	May be used by the Northbridge for other purposes (used for EV6 Northbridges).
SysAddOut MSB=0 & 1 FE00 0000	SysAddOut MSB =0 & 1 FEFF FFFF	PCI Configuration Space (Masked)	This space is used to create PCI configuration cycles using WrBytes, WrLWs, RdBytes, and RdLWs commands only. See Section 2.2.3 on page 15.
SysAddOut MSB=0 & 1 FC00 0000	SysAddOut MSB =0 & 1 FDFF FFFF	PCI I/O Space (Masked)	This space is used to create PCI I/O cycles using only WrBytesWrLWs, RdBytes and RdLWs commands.
SysAddOut MSB=0 & 1 F800 0000	SysAddOut MSB =0 & 1 FBFF FFFF	PCI IACK/Special Cycle Generation (Masked)	WrLWs commands to this space are used to create PCI special cycles. The lower 16 bits of the data is passed on to the PCI bus as both the address and data with the special cycle PCI command. See Section 2.2.1 on page 12 for all special cycles generated by the AMD Athlon™ processor. RdBytes commands to this space are used to create PCI IACK. The lower 16 bits of these addresses are passed on unmodified to the PCI with the IACK PCI command. See Section 2.2.2 on page 15.
SysAddOut MSB=0 & 1 0000 0000	SysAddOut MSB =0 & 1 F7FF FFFF	Reserved (Masked)	May be used by the Northbridge for other purposes (used for EV6 Northbridges).
SysAddOut MSB=0 & 0 0000 0000	SysAddOut MSB =0 & 0 FFFF FFFF	PCI Memory Space (Masked)	The lower 32 bits of these addresses are forwarded unmodified to the PCI. Accessed only with Wr/RdBytes, Wr/RdLWs, Wr/RdQWs. The AMD-761™ system controller generates low-order address bit as required from the AMD Athlon processor system bus MASK field.
SysAddOut MSB=1 & 0 0000 0000	SysAddOut MSB =1 & 3 FFFF FFFF	Normal Memory (Masked Writes)	DRAM, accessed only with masked write commands WrBytes, WrLWs, WrQWs.
SysAddOut MSB=1 & 0 0000 0000	SysAddOut MSB =1 & 3 FFFF FFFF	Reserved (Masked Reads)	The AMD-761 system controller does not support masked reads to this address space.
SysAddOut MSB=1 & 0 FF000 0000	SysAddOut MSB =1 & 3 FFFF FFFF	Reserved (Blocks)	May be used by the Northbridge for other purposes (used for EV6 Northbridges).
SysAddOut MSB=0 & 0 0000 0000	SysAddOut MSB = 0 & 3 FFFF FFFF	Normal Memory (Blocks)	DRAM, accessed with read and write block commands. Note that the AMD-761 system controller only uses 32 address bits internally and the address space wraps. Address 1 0000 0000 is treated the same as 0 0000 0000.

For reference, the x86 view of memory from the perspective of the AMD Athlon processor and the mapping to the Socket2000 memory map is shown in Figure 2.

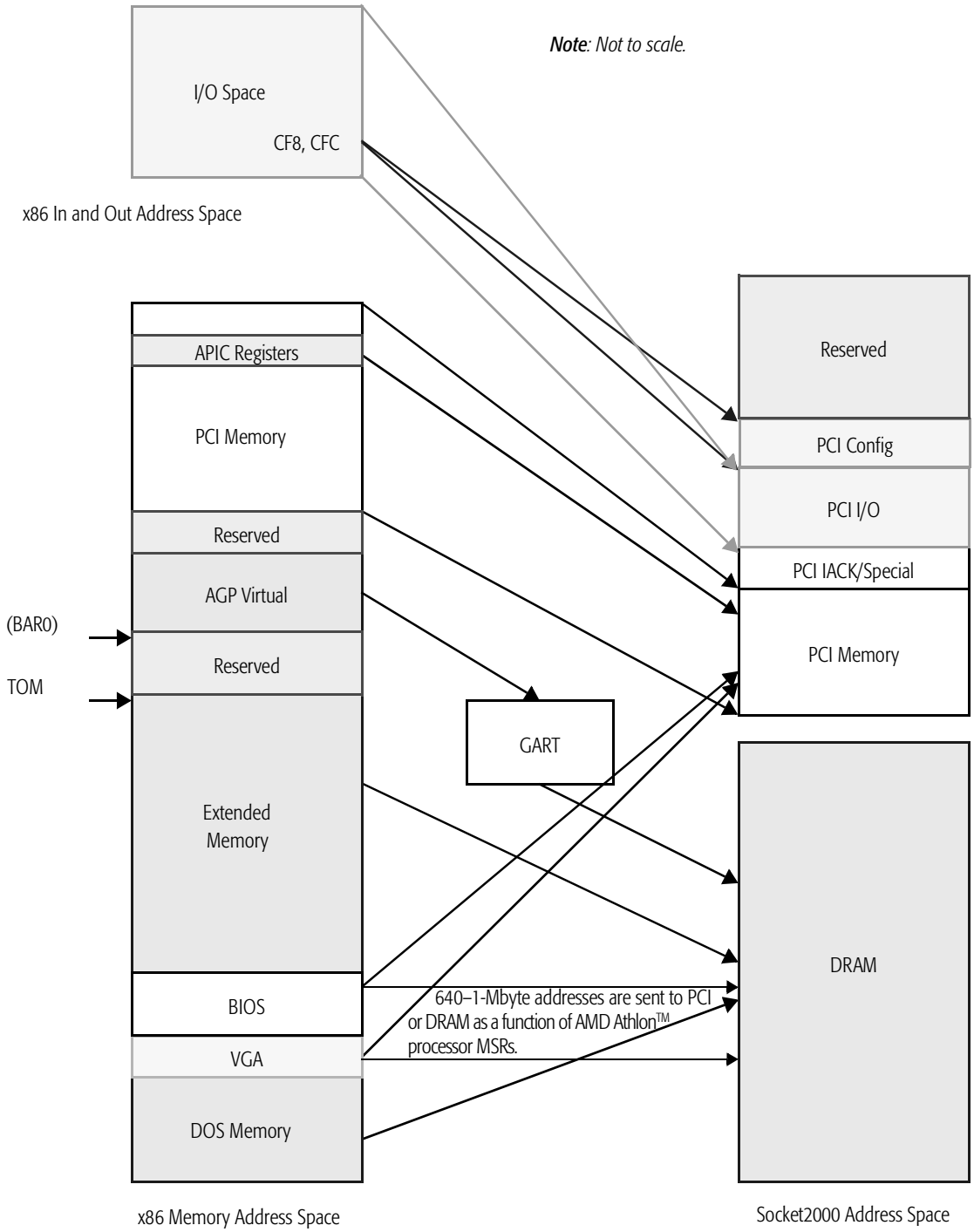

Figure 2. AMD Athlon™ Processor Family x86 Processor Address Mapping

2.2.1 Special Cycles

Special cycles generated by the AMD Athlon processor are forwarded down to the PCI bus with specific values in the address and data fields of the PCI special cycle command. Table 4 defines these values. The AMD Athlon processor generates AMD Athlon processor system bus WrLWs commands to a single address (1 F8000 0000) with the data field specifying the desired special cycle. The AMD-761 system controller maps the AMD Athlon processor system bus data value onto the PCI for both address and data phases of the Special Cycle Transaction.

Table 4. AMD Athlon™ Processor Special Cycle Encodings

Special Cycle	PCI Address and Data Field Contents	Processor Description	Northbridge and Southbridge Description
SHUTDOWN	0000 0000	The AMD Athlon™ processor generates in response to a shutdown condition. AMD Athlon processor system bus WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0000 0000	The AMD-761™ system controller forwards onto the PCI bus the PCI special cycle command: AD[31:0] = 0000 0000 (address and data). AMD-766™ peripheral bus controllers asserts INIT to processor.
HALT	0000 0001	The AMD Athlon processor generates in response to executing a HALT instruction: WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0000 0001	The AMD-761 system controller waits for all queues to memory to be empty (assumes the PCI grant enable register is clear, "Dev0:F0:0x84" on page 70). AMD-761 system controller optionally (via "Dev0:F0:0x60" on page 61) initiates an AMD Athlon system bus disconnect to this specific CPU. The AMD-761 system controller forwards onto the PCI bus (after the optional AMD Athlon system bus disconnect). PCI special cycle command: AD[31:0] = 0000 0001 (address and data) AMD-766 peripheral bus controllers ignores.
WB INVALIDATE	0001 0002	The AMD Athlon processor generates in response to executing a WBINV instruction WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0001 0002	The AMD-761 system controller forwards onto the PCI bus, PCI special cycle command: AD[31:0] = 0001 0002 (address and data). AMD-766 peripheral bus controllers ignores.

Table 4. AMD Athlon™ Processor Special Cycle Encodings (Continued)

Special Cycle	PCI Address and Data Field Contents	Processor Description	Northbridge and Southbridge Description
INVALIDATE	0002 0002	The AMD Athlon™ processor generates in response to executing an INVD instruction WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0002 0002	The AMD-761™ system controller forwards onto the PCI bus the PCI special cycle command: AD[31:0] = 0002 0002 (address and data). AMD-766™ peripheral bus controllers ignores.
FLUSHACK	0003 0002	The AMD Athlon processor generates in response to assertion of the FLUSH pin after all caches have been flushed to memory. WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0003 0002	The AMD-761 system controller forwards onto the PCI bus, PCI special cycle command: AD[31:0] = 0003 0002 (address and data). AMD-766 peripheral bus controllers ignores.
CONNECT	0004 0002	The AMD Athlon processor generates CONNECT as the first cycle after STOP/GRANT or HALT AMD Athlon system bus special cycle regardless of whether or not a disconnect is achieved (or even attempted). WrLWs command: SysAddOut: MSB= 0 & [33: 0] = 1 F8000 0000 SysDatOut: [31: 0] = 0004 0002	The AMD-761 system controller forwards onto the PCI bus, PCI special cycle command: AD[31: 0] = 0004 0002 (address and data) AMD-766 peripheral bus controllers ignores.
SMM ACK (ENTER)	0005 0002	The AMD Athlon processor generates an SMM ACK (ENTER) when entering a system management interrupt. WrLWs command: SysAddOut: MSB= 0 & [33: 0] = 1 F8000 0000 SysDatOut: [31: 0] = 0005 0002	The AMD-761 system controller forward onto the PCI bus, special cycle command: AD[31: 0] = 0005 0002.
SMM ACK (EXIT)	0006 0002	The AMD Athlon processor generates SMM ACK (EXIT) when exiting from a system management interrupt. WrLWs command: SysAddOut: MSB= 0 & [33: 0] = 1 F8000 0000 SysDatOut: [31: 0] = 0006 0002	The AMD-761 system controller forwards to the PCI bus. Command: AD[31: 0] = 0006 0002.

Table 4. AMD Athlon™ Processor Special Cycle Encodings (Continued)

Special Cycle	PCI Address and Data Field Contents	Processor Description	Northbridge and Southbridge Description
STOP/GRANT	0012 0002	AMD Athlon™ processor generates in response to assertion of the STPCLK. WrLWs command: SysAddOut: MSB=0 & [33:0] = 1 F8000 0000 SysDatOut: [31:0] = 0012 0002	The AMD-761™ system controller waits for all queues to memory to be empty (assumes the PCI grant enable register is clear, "Dev0:F0:0x84" on page 70). The AMD-761 system controller system controller optionally (via "Dev0:F0:0x60" on page 61) initiates an AMD Athlon processor system bus disconnect to this specific processor. The AMD-761 system controller forwards onto the PCI bus (after the optional system bus disconnect) PCI special cycle command: AD[31:0] = 0012 0002 (address and data). The AMD-766™ peripheral bus controllers receives and enters the appropriate power state. The AMD-766 peripheral bus controllers may then assert DCSTOP# to the Northbridge to signal that it should deassert CKE to DDR SDRAMs and stop its internal clocks.

2.2.2 IACK

In x86 compatible Socket2000 systems, APIC is used as the interrupt controller. To fetch the appropriate vector during IACK cycles, x86 processors are required to assert their APIC ID (CPU ID) on bits [15:12] of the address field when reading the IACK generation space. IACK return data flushes all PCI and AGP/PCI write buffers to memory.

2.2.3 PCI Configuration Accesses

In legacy x86 PC systems, PCI configuration cycles are generated via an indirect method. A configuration address register is defined at I/O address 0CF8 that allows software to load a value that is asserted on the PCI address wires during the next configuration read/write cycle. A configuration data register is defined at I/O address 0CFC that allows software to generate configuration read and write cycles on the PCI using IN and OUT instructions. Data sent during OUT instructions to the Configuration Data register is asserted on the PCI data wires during the generated configuration write transaction. Data received in response to a generated configuration read transaction is returned to satisfy the IN from the Configuration Data register.

In Socket2000 systems, PCI configuration cycles are generated in one of two ways:

- In EV6 Compatible mode, the x86 processor must detect IN and OUT instructions that reference 0CF8 and 0CFC and generate the appropriate, explicit RdBytes/Rd/LWs and WrBytes/WrLWs Socket2000 commands to a 16-Mbyte region as follows:
  - When an OUT instruction is detected to 0CF8, the write data is saved into a register and the instruction retired.
  - When an IN/OUT instruction is detected to 0CFC, an appropriate AMD Athlon system bus Rd/Wr transaction is launched with the SysAdd Field[23:0] taken from the register that saved the most recent write to 0CF8 (above).
- In traditional mode, which the AMD-761 system controller implements, IN and OUT instructions that reference 0CF8 and 0CFC are passed normally on to the AMD Athlon processor system bus where the Northbridge generates the appropriate PCI configuration access.

2.3 Address Decoding

A consistent view of memory and PCI devices is enforced by decoding logic in the AMD-761 system controller in the AMD Athlon processor system bus and PCI interfaces.

2.3.1 Socket2000 Address Decoding

The AMD-761 system controller must consider both the AMD Athlon processor system bus SysAddOut field and the command field when deciding what to do with a given command. This AMD Athlon processor system bus decoding is summarized as follows:

- SysAddOut MSB = 0 and command is a block command, DRAM is accessed:
  - If SysAddOut [31:0] falls between Dev0:BAR0 and Dev0:BAR0+Len, address is to AGP virtual address space and needs to passed through the GART before presentation to DRAM.
- SysAddOut MSB = 1 and command is a masked write command (WrQWs, WrLWs, WrBytes), DRAM is accessed:
  - If SysAddOut [31:0] falls between Dev0:BAR0 and Dev0:BAR0+Len, address is to AGP virtual address space and needs to passed through the GART before presentation to DRAM.
- SysAddOut MSB = 0 and SysAddOut [35:32] = 0 and command is a masked command, PCI memory-mapped I/O is accessed:
  - Using Dev0:F0:0x14, BAR1, send to the AMD-761 system controller memory-mapped GART control registers (see Section 2.5 on page 138).
  - Memory range address decoding, send to either PCI or AGP/PCI using address bits [31:0] based on the following:
    - Dev1:0x20, 0x24 (see “AGP/PCI Memory Limit and Base (Dev1:0x20)” on page 131 and “AGP/PCI Prefetchable Memory Limit and Base (Dev1:0x24)” on page 133).
    - Dev 0:F0:0x84 AGP VGA BIOS bits, see “Bit Definitions PCI Arbitration Control (Dev0:F0:0x84)” on page 71).

- SysAddOut MSB = 0 and SysAddOut [35:24] = 1F8 and command is RdBytes, an IACK special cycle is generated on the primary PCI. SysAddOut[15:0] are asserted on PCI AD[15:0] during this cycle. The data returned on the PCI is returned to the processor.
- SysAddOut MSB = 0 and SysAddOut [35:24] = 1F8 and command is WrBytes, a PCI special cycle is generated on the primary PCI. SysAddOut[15:0] are asserted on PCI AD[15:0] during this cycle (address = data).
- SysAddOut MSB = 0 and SysAddOut [35:24] = 1FC/1FD and command is RdBytes or WrBytes, a PCI I/O command is generated. SysAddOut[23:0] are asserted on PCI AD[23:0] with the PCI I/O read or write command.
  - Using Dev1:0x1C, I/O range address decoding, send to either PCI or AGP/PCI.

Note: *Low-order AMD Athlon processor system bus address bits, per the AMD Athlon processor system bus specification, SysAddOut only goes down to PA[3]. For mask operations, the Mask[7:0] bits are encoded to logically create PA[2:0] in the above.*

2.3.2 PCI/AGP Master Address Decoding

The PCI controllers in the AMD-761 system controller must consider the received PCI/AGP address in conjunction with the BAR registers and the memory configuration registers to route the transaction. The AMD-761 system controller does not allow PCI masters to access I/O regions or main memory from 640 Kbyte to 1 Mbyte (unless the EV6_Mode bit is set as described in "Bit Definitions PCI Arbitration Control (Dev0:F0:0x84)" on page 71). This decoding is summarized as follows:

1. AD[31:0] is less than the physical top of memory (from the memory controller), DRAM is accessed.
2. AD[31:0] is above the physical top of memory and it falls between Dev0:BAR0 and Dev0:BAR0+Len, address is to AGP virtual address space and needs to be passed through the GART before presentation to DRAM.

3. Memory range address decoding, send to AGP/PCI using address bits [31:0] based on the following (for writes only from the primary PCI):
    - Dev1:0x20, 0x24 (see "AGP/PCI Memory Limit and Base (Dev1:0x20)" on page 131 and "AGP/PCI Prefetchable Memory Limit and Base (Dev1:0x24)" on page 133).
    - Dev 0:F0:0x84 AGP VGA BIOS bits (see "Bit Definitions PCI Arbitration Control (Dev0:F0:0x84)" on page 71).
4. Else, the primary PCI is accessed (for writes only from the AGP/PCI).

Note: *GART Control register access. The AMD-761 system controller does not allow access to the memory-mapped GART control registers from either PCI or AGP/PCI masters.*

2.4 Configuration Registers

All functional registers in the AMD-761 system controller are implemented as PCI configuration registers. The AMD-761 system controller implements a standard PCI hierarchy that allows BIOS software to enumerate devices on the primary PCI, the AGP port, and future interfaces. See the logical bus hierarchy in Figure 3 on page 19.

Note that the AMD-761 system controller only responds to function 0 and 1, device 0 and function 0, device 1. All other configuration accesses return Fs. Function 1, device 0 accesses are ignored unless enabled by the appropriate bit in the PCI Control register (see "Dev0:F0:0x4C" on page 47).

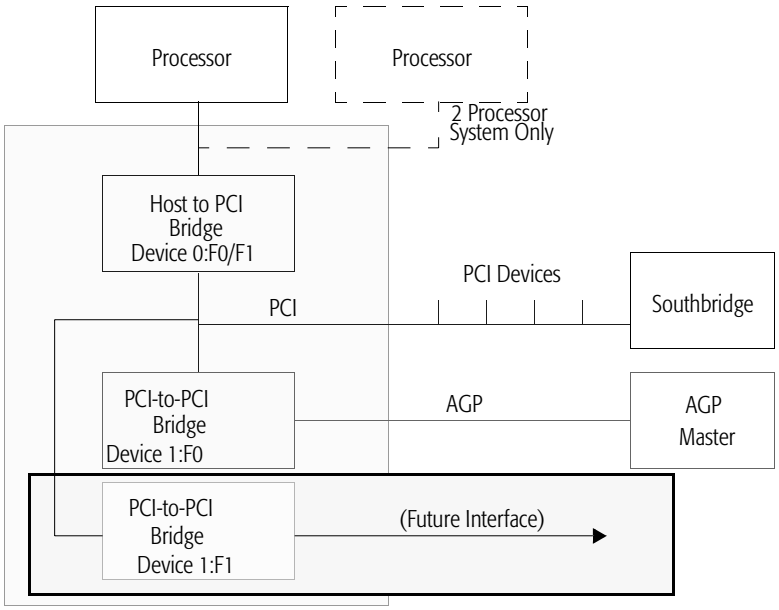

Figure 3. AMD-761™ System Controller Logical Bus Hierarchy

2.4.1 I/O Register Map

The AMD-761 system controller implements some I/O registers (accessed by processor I/O instructions). These registers, as presented in Table 5, are the Configuration Address and Configuration Data registers as specified in *PCI Local Bus Specification*, Revision 2.2.

Table 5. I/O Register Map

Register	AMD Athlon™ Processor System Bus Address	Reference
Configuration Address	SysAddOut MSB =0 & 1 FC000 0CF8	"I/O:0CF8" on page 21 and "I/O:0CF8" on page 23
Configuration Data	SysAddOut MSB =0 & 1 FC000 0CFC	"I/O:0CFC" on page 25

Configuration Address Register Type 0 I/O:0CF8

	31	30	29	28	27	26	25	24
Bit	Config_En	Reserved						
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R						

	23	22	21	20	19	18	17	16
Bit	PCI_Bus_Num							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Dev_Num					Func_Num		
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Reg_Num						Reserved	
Reset	0	0	0	0	0	0	0	0
R/W	R/W						R	

Register Description

When writes to the configuration address register have [23:16] == 0h00, a Type 0 configuration access is specified.

Bit Definitions **Configuration Address Register Type 0 (I/O:0CF8)**

Bit	Name	Function
31	Config_En	**Configuration Enable** 0 = PCI configuration cycles are not generated. 1 = Accesses to the Configuration Data and Address registers are converted to configuration cycles on the PCI.
30–24	Reserved	**Reserved**
23–16	PCI_Bus_Num	**PCI Bus Number** This bit field defines which PCI bus in the system is referenced with this address. The AMD-761™ system controller logically implements two PCI buses. The main PCI bus normally enumerates as bus 0 and the AGP bus enumerates as bus 1.
15–11	Dev_Num	**Device Number** This bit field defines which device is accessed in the system. Devices are assigned numbers in a system by tying the device IDSEL wire to a specific PCI AD wire. The AMD-761 system controller decodes this field and asserts the appropriate AD wire during the address phase to select the defined device. In the AMD-761 system controller there are two "hard-wired" device numbers for the host to PCI bridge (0b00000) and P2P bridge (0b00001).
10–8	Func_Num	**Function Number** This bit field defines which function is accessed in a given device. The AMD-761 system controller responds to function 0 only (0b000) by default. Function 1 (DDR PDL registers) can be enabled via writing to the PCI Control register (Dev 0:F0:0x4C) as described on page 47.
7–2	Reg_Num	**Register Number** This bit field defines which specific PCI register is accessed in the device and function specified above. The register numbers for the AMD-761 system controller device 0 are listed in Table 6, "Device 0, Function 0 Configuration Register Map," on page 27. The register numbers for the AMD-761 device 1 are listed in Table 15, "Device 1 Configuration Register Map," on page 117.
1–0	Reserved	**Reserved**

Programming Notes

Configuration Address Register Type 1 I/O:0CF8

	31	30	29	28	27	26	25	24
Bit	Config_En	Reserved						
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R						

	23	22	21	20	19	18	17	16
Bit	PCI_Bus_Num							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Dev_Num					Func_Num		
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Reg_Num						Reserved	
Reset	0	0	0	0	0	0	0	0
R/W	R/W						R	

Register Description

When writes to the configuration address register have [23:16] ~= 0h00, a type 1 configuration access is specified.

Bit Definitions **Configuration Address Register Type 1 (I/O:0CF8)**

Bit	Name	Function
31	Config_En	**Configuration Enable** 0 = PCI configuration cycles are not generated. 1 = Accesses to the Configuration Data and Address registers are converted to configuration cycles on the PCI.
30–24	Reserved	**Reserved**
23–16	PCI_Bus_Num	**PCI Bus Number** This bit field defines which PCI bus in the system is referenced with this address. The AMD-761™ system controller logically implements two PCI buses. The main PCI bus normally enumerates as bus 0 and the AGP bus enumerates as bus 1.
15–11	Dev_Num	**Device Number** This bit field defines which device is accessed in the system on the target PCI bus. This field is passed on directly to the AD wires undecoded.
10–8	Func_Num	**Function Number** This bit field defines which function is accessed in a given device. This field is passed on directly to the AD wires undecoded.
7–2	Reg_Num	**Register Number** This bit field defines which specific PCI register is accessed in the device and function specified above.
1–0	Reserved	**Reserved**

Programming Notes

Configuration Data I/O:0CFC

	31	30	29	28	27	26	25	24
Bit	Config_Data							
Reset	x	x	x	x	x	x	x	x
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	Config_Data							
Reset	x	x	x	x	x	x	x	x
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Config_Data							
Reset	x	x	x	x	x	x	x	x
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Config_Data							
Reset	x	x	x	x	x	x	x	x
R/W	R/W							

Register Description

Bit Definitions — Configuration Data (I/O:0CFC)

Bit	Name	Function
31—0	Config_Data	**Configuration Data** This bit field is used to access the PCI configuration register specified in the Configuration Address register above.

Programming Notes

2.4.2 Configuration Register Access

The AMD-761 system controller implements most registers as PCI configuration registers. The x86 software executes IN and OUT instructions to I/O addresses of 0CF8 and 0CFC to access all configuration registers. These are translated by the AMD Athlon™ processor into AMD Athlon processor system bus RdBytes and WrBytes commands with the lower 24 bits of the address field containing the logical contents of the ConfigAddr register (I/O address 0CF8). The format of this register is shown in "I/O:0CF8" on page 21 and "I/O:0CF8" on page 23.

Configuration accesses in the AMD-761 system controller conform to the following rules:

- The AMD-761 system controller is defined to be function 0 and 1, device 0; and function 0, device 1. The IDSEL pin of all external PCI devices must be wired to 1 of AD[31:13] as logically [12:11] are assigned to device 0, 1 (AMD-761 system controller).
- Function 1, device 0 configuration space contains only the DDR Programmable Delay Line (PDL) registers. This space is enabled only when the appropriate bit is set in the PCI Control register (see "Dev0:F0:0x4C" on page 47). Accesses to the normal reserved PCI space of function 1 yields all 1s. Accesses to function 1 are ignored when function 1 is not enabled.
- Device 0 accesses correspond to the host to PCI bridge registers defined in Section 2.4.3 on page 27.
- Device 1 accesses correspond to the PCI-to-PCI bridge registers defined in Section 2.4.5 on page 117.
- Access can be byte, word or DWord in length and must be naturally aligned.

Northbridges are required to create type 0 and type 1 accesses as follows:

- If SysAdd[23:16] = 0 (Bus# = 2'h00), a type 0 config cycle is generated and PCI AD[1:0] = 2'b00. Device#, SysAdd[15:11] is decoded and asserted on PCI AD[31:11] for IDSEL.
- If SysAdd[23:16] != 0 (Bus# != 2'h00), a type 1 config cycle is generated and PCI AD[1:0] = 2'b01. Bus# and Device# fields are passed onto the PCI directly with no decoding. PCI AD[31:24] = 2'h00.

2.4.3 Device 0: PCI Configuration Registers

In Table 6, the column entitled Offset consists of the register number specified in the Configuration Address register bits [7:2] concatenated with 0b00 to form a simple 1-byte offset. Reserved configuration registers return 0 when read.

Table 6. Device 0, Function 0 Configuration Register Map

Host to PCI Bridge (Device 0, Function 0)				Offset	Reference
Device ID		Vendor ID		0x00–0x03	"Dev0:F0:0x00" on page 30
Status		Command		0x04–0x07	"Dev0:F0:0x04" on page 32
Class Code = 0x060000			Revision ID	0x08–0x0B	"Dev0:F0:0x08" on page 35
Reserved	Header Type	Latency Timer	Reserved	0x0C–0x0F	"Dev0:F0:0x0C" on page 36
BAR0 - AGP Virtual Address Space				0x10–0x13	"Dev0:F0:0x10" on page 37
BAR1 - GART Memory-Mapped Control Registers Pointer				0x14–0x17	"Dev0:F0:0x14" on page 39
Reserved				0x18–0x1B	
Reserved				0x1C–0x33	
Reserved			Capabilities Pointer: A0	0x34–0x37	"Dev0:F0:0x34" on page 41
Reserved				0x38–0x43	
Extended BIU Control				0x44–0x53	"Dev0:F0:0x44" on page 42
ECC Mode/Status				0x48–0x4B	"Dev0:F0:0x48" on page 44
PCI Control				0x4C–0x4F	"Dev0:F0:0x4C" on page 47
AMD Athlon™ Processor System Bus Dynamic Compensation				0x50–0x53	"Dev0:F0:0x50" on page 49
DRAM Timing				0x54–0x57	"Dev0:F0:0x54" on page 51
DRAM Mode/Status				0x58–0x5B	"Dev0:F0:0x58" on page 56
Reserved				0x5C–0x5F	
BIU0 Status/Control				0x60–0x63	"Dev0:F0:0x60" on page 61
BIU0 SIP				0x64–0x67	"Dev0:F0:0x64" on page 64

Table 6. Device 0, Function 0 Configuration Register Map (Continued)

Host to PCI Bridge (Device 0, Function 0)			Offset	Reference
Reserved			0x68–0x6B	
Reserved			0x6C–0x6F	
Memory Status/Control			0x70–0x73	"Dev0:F0:0x70" on page 66
Reserved			0x74–0x77	
Reserved			0x78–0x7B	
Reserved			0x7C–0x7F	
Reserved	Boot Proc	WHAMI	0x80–0x83	"Dev0:F0:0x80" on page 68
PCI Arbitration Control			0x84–0x87	"Dev0:F0:0x84" on page 70
Configuration Status			0x88–0x8B	"Dev0:F0:0x88" on page 74
Reserved			0x8C–0x8F	
Reserved			0x90–0x93	
Reserved			0x94–0x97	
Reserved			0x98–0x9B	
PCI Top of Memory	Reserved		0x9C–0x9F	"Dev0:F0:0x9C" on page 77
AGP Capability Identifier			0xA0–0xA3	"Dev0:F0:0xA0" on page 79
AGP Status			0xA4–0xA7	"Dev0:F0:0xA4" on page 80
AGP Command			0xA8–0xAB	"Dev0:F0:0xA8" on page 82
AGP Virtual Address Space Size			0xAC–0xAF	"Dev0:F0:0xAC" on page 84
GART/AGP Mode Control			0xB0–0xB3	"Dev0:F0:0xB0" on page 86
AGP 4X Dynamic Compensation			0xB4–0xB7	"Dev0:F0:0xB4" on page 88
AGP Compensation Bypass			0xB8–0xBF	"Dev0:F0:0xB8" on page 91
Memory Base Address 0			0xC0–0xC3	"Dev0:F0:0xC0" on page 95
Memory Base Address 1			0xC4–0xC7	"Dev0:F0:0xC4" on page 95

Table 6. Device 0, Function 0 Configuration Register Map (Continued)

Host to PCI Bridge (Device 0, Function 0)	Offset	Reference
Memory Base Address 2	0xC8–0xCB	"Dev0:F0:0xC8" on page 95
Memory Base Address 3	0xCC–0xCF	"Dev0:F0:0xCC" on page 95
Memory Base Address 4	0xD0–0xD3	"Dev0:F0:0xD0" on page 95
Memory Base Address 5	0xD4–0xD7	"Dev0:F0:0xD4" on page 95
Memory Base Address 6	0xD8–0xDB	"Dev0:F0:0xD8" on page 95
Memory Base Address 7	0xDC–0xDF	"Dev0:F0:0xDC" on page 95
Reserved	0xE0–0xFF	

PCI ID — Dev0:F0:0x00

	31	30	29	28	27	26	25	24
Bit	Dev_ID							
Reset	0	1	1	1	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Dev_ID							
Reset	0	0	0	0	1	1	1	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Vend_ID							
Reset	0	0	0	1	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Vend_ID							
Reset	0	0	1	0	0	0	1	0
R/W	R							

Register Description

Bit Definitions **PCI ID (Dev0:F0:0x00)**

Bit	Name	Function
31—16	Dev_ID	**Device Identifier** This 16-bit field is assigned by the device manufacturer and identifies the type of device. The current Northbridge device ID assignments are: AMD-761™ system controller — AMD Athlon™ processor, 1P DDR 133 MHz 0x700E host to PCI bridge 0x700F PCI-to-PCI bridge (4-X AGP) AMD-762™ system controller — AMD Athlon processor, 2P DDR 133 MHz 0x700C host to PCI bridge 0x700D PCI-to-PCI bridge (4-X AGP) AMD-751™ system controller — AMD Athlon processor, 1P SDRAM-100 0x7006 host to PCI bridge 0x7007 PCI-to-PCI bridge (1X/2X AGP)
15—0	Vend_ID	**Vendor Identifier** This 16-bit field identifies the manufacturer of the device.

Programming Notes

PCI Command and Status — Dev0:F0:0x04

	31	30	29	28	27	26	25	24
Bit	PERR_Rcv	SERR_Sent	Mas_ABRT	Trgt_ABRT	Trgt_ABRT _ Signaled	DEVSEL_Timing		Data_PERR
Reset	0	0	0	0	0	0	1	0
R/W	R	R/W1C	R/W1C	R/W1C	R	R		R

	23	22	21	20	19	18	17	16
Bit	Fast_B2B	UDF	66M	Cap_Lst	Reserved			
Reset	0	0	0	1	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved						FBACK	SERR
Reset	0	0	0	0	0	0	0	0
R/W	R							R/W

	7	6	5	4	3	2	1	0
Bit	STEP	PERR	VGA	MWINV	SCYC	MSTR	MEM	I/O
Reset	0	0	0	0	0	1	0	0
R/W	R						R/W	R

Register Description

Bit Definitions **PCI Command and Status (Dev0:F0:0x04)**

Bit	Name	Function
31	PERR_Rcv	**Detected Parity Error** This bit is always 0 because the AMD-761™ system controller does not support data parity checking.
30	SERR_Sent	**Signaled System Error** This bit is set whenever the AMD-761 system controller generates a system error and asserts the SERR# line (ECC, GART error). This bit is cleared by writing a 1. Refer to Table 7 on page 34 for details about SERR# assertion and status.
29	Mas_ ABRT	**Received Master Abort** This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a master abort. This bit is cleared by writing a 1.
28	Trgt_ABRT	**Received Target Abort** This bit is set whenever a CPU to PCI transaction (except for a special cycle) is terminated due to a target abort. This bit is cleared by writing a 1.
27	Trgt_ABRT_ Signaled	**Signaled Target Abort** This bit is always 0 because the AMD-761 system controller does not terminate transactions with target aborts.
26–25	DEVSEL_Timing	**DEVSEL# Timing** This bit field defines the timing of DEVSEL# on the AMD-761 system controller. The AMD-761 system controller supports medium DEVSEL# timing.
24	Data_PERR	**Data Parity Error** This bit is always 0 because the AMD-761 system controller does not report parity errors.
23	Fast B2B	**Fast Back-to-Back Capable** This bit is always 0, indicating that the AMD-761 system controller as a target is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
22	UDF	**User-Definable Features** This bit is always 0, indicating that UDF is not supported on the AMD-761 system controller.
21	66M	**66-MHz Capable** This bit is always 0, indicating that the AMD-761 system controller is not 66-MHz capable.
20	Cap_Lst	**Capabilities List** This bit is set to indicate that this device's configuration space supports a capabilities list.
19–10	Reserved	**Reserved**
9	FBACK	**Fast Back-to-Back to Different Devices Enable** This bit is always 0, because the AMD-761 system controller does not allow generation of fast back-to-back transactions to different agents.
8	SERR	**System Error Enable** 0 = SERR# driver disabled 1 = SERR# driver enabled Refer to Table 7 for details about SERR# assertion and status.

Bit Definitions (Continued) **PCI Command and Status (Dev0:F0:0x04)**

Bit	Name	Function
7	STEP	**Address Stepping** This bit is always 0 because the AMD-761™ system controller does not perform address stepping.
6	PERR	**Parity Error Response** This bit is always 0 because the AMD-761 system controller does not report data parity errors.
5	VGA	**VGA Palette Snoop Enable** This bit is always 0, indicating that the AMD-761 system controller does not snoop the VGA palette address range.
4	MWINV	**Memory Write and Invalidate Enable** This bit is always 0 because the AMD-761 system controller does not generate memory write and invalidate commands.
3	SCYC	**Special Cycle** This bit is always 0 because the AMD-761 system controller ignores PCI special cycles.
2	MSTR	**Bus Master Enable** This bit is always set, indicating that the AMD-761 system controller is allowed to act as a bus master on the PCI bus.
1	MEM	**Memory Access Enable** 0 = PCI memory accesses ignored 1 = PCI memory accesses responded to
0	I/O	**I/O Access Enable** This bit is always 0 because the AMD-761 system controller does not respond to I/O cycles on the PCI bus.

Programming Notes

Table 7 lists the controls required to enable the assertion of the AMD-761 SERR# pin and the various status bits that can be read to determine when the SERR# and A_SERR# pins have been asserted.

Table 7. AMD-761™ System Controller SERR# Assertion Control and Status Bits

SERR# Source	SERR# Pin Assertion Control	Signalled System Error Status Bit
GART or ECC error	Enabled by bit 8, Dev 0:F0:0x04, PCI Status/Command register.	Read bit 30, Dev 0:F0:0x04, PCI Status/Command register.
A_SERR# assertion on AGP interface forwarded to SERR# pin	Enabled by bit 8, Dev 1:F0:0x04, PCI Status/Command register, and bit 17, Dev 1:F0:0x3C, AGP/PCI Interrupt and Bridge Control.	Read bit 30, Dev 1:F0:0x1C, AGP/PCI Status, I/O and Base Limit, and bit 30, Dev 1:F0:0x04, AGP/PCI Command/Status.

PCI Revision ID and Class Code — Dev0:F0:0x08

	31	30	29	28	27	26	25	24
Bit	Class_Code							
Reset	0	0	0	0	0	1	1	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Sub-Class_Code							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Prog_I/F							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Rev_ID(See Programming Notes below.)							
Reset	0	0	0	1	0	0	0	0
R/W	R							

Register Description

Bit Definitions — **PCI Revision ID and Class Code (Dev0:F0:0x08)**

Bit	Name	Function
31–24	Class_Code	**Class Code** Indicates a bridge device.
23–16	Sub-Class_Code	**Sub-Class Code** Indicates a Host/PCI bridge.
15–8	Prog_I/F	**Program Interface** Indicates a Host/PCI bridge.
7–0	Rev_ID	**Revision Identification** Identifies revision number of the device.

Programming Notes

Refer to the *AMD-761™ System Controller Revision Guide*, order# 23613, for details of the Rev_ID field for each silicon revision.

PCI Latency Timer and Header Type — Dev0:F0:0x0C

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Header_Type							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Lat_Timer							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

Bit Definitions — PCI Latency Timer and Header type (Dev0:F0:0x0C)

Bit	Name	Function
31–24	Reserved	**Reserved**
23–16	Header_Type	**Header Type** Bit 23 is always 0, indicating that the AMD-761™ system controller is a single function device. Bits [22:16] are 0, indicating that Type 00 configuration space header format is supported.
15–8	Lat_Timer	**Latency Timer** This bit field defines the minimum amount of time in PCI clock cycles that the bus master can retain ownership of the bus. This action is mandatory for masters that are capable of performing a burst consisting of more than two data phases.
7–0	Reserved	**Reserved**

Programming Notes

Base Address 0: AGP Virtual Address Space — Dev0:F0:0x10

	31	30	29	28	27	26	25	24
Bit	Base_Addr_High							Base-Addr_Low
Reset	0	0	0	0	0	0	0	0
R/W	R/W							R

	23	22	21	20	19	18	17	16
Bit	Base_Addr_Low							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Base_Addr_Low							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Base_Addr_Low				Prefetchable	Type		Memory
Reset	0	0	0	0	1	0	0	0
R/W	R							

Register Description

This register is used by system BIOS memory mapping software to allocate virtual address space for AGP.

Bit Definitions **Base Address 0: AGP Virtual Address Space (Dev0:F0:0x10)**

Bit	Name	Function
31–25	Base_Addr_High	**Base Address High** This bit field forms the upper part of BAR0. This field is loaded by BIOS software. Note that when the GART enable bit in the AGP Virtual Address Space Size register is 0 (see "Dev0:F0:0xAC" on page 84), these bits always return 0s to indicate no address space should be allocated to AGP. Note that a write to this register must occur before a read returns 0s with the GART enable bit cleared. This bit field corresponds to bits [3:1] of the AGP Virtual Address Space Size register. When bits [3:1] of that register are set, the R/W attributes in bits [30:25] in this register are automatically set. BIOS software writes all 1s to this BAR register and then reads back the register to determine how much memory is required for AGP as follows:
24–4	Base_Addr_Low	**Base Address Low** This bit field is hardwired to return 0s to indicate that the minimum allocated memory size is 32 Mbytes.
3	Prefetchable	**Prefetchable** This bit is hardwired to 1 to indicate that this range is prefetchable.
2–1	Type	**Type** This bit field is hardwired to indicate that this base register is 32 bits wide and mapping can be performed anywhere in the 32-bit address space.
0	Memory	**Memory** This bit is hardwired to 0 to indicate that this base address register maps into memory space.

31	30	29	28	27	26	25	Memory
RW	RW	RW	RW	RW	RW	RW	32 Mbytes
RW	RW	RW	RW	RW	RW	R	64 Mbytes
RW	RW	RW	RW	RW	R	R	128 Mbytes
RW	RW	RW	RW	R	R	R	256 Mbytes
RW	RW	RW	R	R	R	R	512 Mbytes
RW	RW	R	R	R	R	R	1 Gbyte
RW	R	R	R	R	R	R	2 Gbytes

Programming Notes

Base Address 1: GART Memory-Mapped Register Base — Dev0:F0:0x14

	31	30	29	28	27	26	25	24
Bit	Base_Addr_High							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	Base_Addr_High							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Base_Addr_High				Base_Addr_Low			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

	7	6	5	4	3	2	1	0
Bit	Base_Addr_Low				Prefetchable	Type		Memory
Reset	0	0	0	0	1	0	0	0
R/W	R							

Register Description

This register provides the base address for the GART memory-mapped configuration register space (see "Memory-Mapped Register Map" on page 140 for details).

Bit Definitions **Base Address 1: GART Memory-Mapped Register Base (Dev0:F0:0x14)**

Bit	Name	Function
31–12	Base_Addr_High	**Base Address High** This bit field forms the upper part of BAR1. This field is loaded by BIOS software.
11–4	Base_Addr_Low	**Base Address Low** This bit field is hardwired to return 0s to indicate that 4 Kbytes are allocated to GART memory-mapped control registers and that the registers always reside in a 4-Kbyte boundary per *PCI Local Bus Specification*, Revision 2.2.
3	Prefetchable	**Prefetchable** This bit is hardwired to 1 to indicate that this range is prefetchable
2–1	Type	**Type** This bit field is hardwired to indicate that this base register is 32 bits wide and mapping can be performed anywhere in the 32-bit address space.
0	Memory	**Memory** This bit is hardwired to 0 to indicate that this base address register maps into memory space.

Programming Notes

AGP/PCI Capabilities Pointer — Dev0:F0:0x34

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	CAP_PTR							
Reset	1	0	1	0	0	0	0	0
R/W	R							

Register Description

Bit Definitions — AGP/PCI Capabilities Pointer (Dev0:0x34)

Bit	Name	Function
31–8	Reserved	**Reserved**
7–0	CAP_PTR	**Capabilities Pointer** This field contains a byte offset into a device's configuration space containing the first item in the capabilities list. The first item in the capabilities list is the AGP function. Note that when the AGP valid bit in the PCI-to-PCI bridge virtual address space register is set to invalid, this capabilities pointer is set by the chipset to point to the next item in the linked list. If no next item exists, then it is set to null.

Programming Notes

Extended BIU Control — Dev0:F0:0x44

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved		Reserved			P0_WrDataDly		
Reset	0	0	0			SIP Stream		
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved	Reserved	Reserved	Reserved	P0_2BitPF			
Reset	0	0	0	0	0	0	0	0
R/W	R	R		R	R/W	R		

Register Description

This register provides controls for the processor interface, in addition to the BIU Control register at Dev 0:F0:0x60 for Processor 0.

Bit Definitions **Extended BIU Control (Dev0:F0:0x44)**

Bit	Name	Function
31–11	Reserved	**Reserved**
15–14	Reserved	**Reserved**
10–8	P0_WrDataDly	**Write Data Delay** P0_WrDataDly is the time in SYSCLK periods from the launch of a SysDC WriteData command until the launch of the first data object by the processor. This value is a calculated part of the SIP stream. This value is not provided in the BIU SIP register and is thus provided here.
7-4	Reserved	**Reserved**
3	P0_2BitPF	**Two Bit Times Per Frame Enable** This bit enables the use of the two bit time commands on the AMD Athlon™ processor system bus. This bit must be set when connected to an AMD Athlon processor and disabled when connected to an Alpha processor. For proper operation, BIOS must not clear this bit once it has been set. 0 = Two-bit time commands disabled 1 = Two-bit time commands enabled (AMD Athlon processor only)
2–0	Reserved	**Reserved** These bits must be written with 0 (cleared) for normal operation.

Programming Notes

ECC Mode/Status — Dev0:F0:0x48

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	SERR_Enable		Reserved	ECC_Diag	ECC_Mode		ECC_Status	
Reset	X	X	0	X	X	X	0	0
R/W	R/W		R	R/W	R/W		R/W1C	

	7	6	5	4	3	2	1	0
Bit	ECC_CS_MED				ECC_CS_SED			
Reset	0	0	0	0	0	0	0	0
R/W	R				R			

Register Description

This register provides ECC mode control and status reporting for the DRAM system.

Note that some bits of this register are not initialized at reset time, and all bits must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **ECC Mode/Status (Dev0:F0:0x48)**

Bit	Name	Function
31–16	Reserved	**Reserved**
15-14	SERR_Enable	**System Error Enable** These bits control the AMD-761™ system controller's reporting of ECC errors to the system via the SERR# pin on the PCI bus. Note that SERR# assertion is still subject to the normal PCI SERR# enable (bit 8 in Dev 0:F0:0x04). Refer to Table 7 on page 34 for details about SERR# assertion and status. 00 = SERR# assertion is disabled. X1 = Multiple bit errors force SERR# assertion. 1X = Single bit errors force SERR# assertion.
13	Reserved	**Reserved**
12	ECC_Diag	**Error Correcting Code Diagnostic Mode Enable** 0 = ECC diagnostic mode disabled 1 = ECC diagnostic mode enabled When the ECC diagnostic mode is enabled, the AMD-761 system controller always writes 0x00 to the ECC byte to aid testing of the ECC logic. During partial writes, the RMW sequence still occurs, but the ECC bits are always written to 0x00. For reads, the ECC circuitry is unaffected by the ECC_Diag bit. The ECC code returned from memory is checked, and errors are reported in the ECC_Status bits as usual. Correction is not performed in this mode.
11–10	ECC_Mode	**Error Correcting Code Mode** 00 = ECC disabled, no error detection or correction is performed. 01 = EC_HiPerf mode enabled. Error checking and status reporting is enabled. Data destined for the PCI/AGP and memory (RMR) is **not** corrected. 10 = ECC_HiPerf mode enabled. Error checking and status reporting is enabled. Data destined for the PCI/AGP and memory (RMR) is corrected. 11 = ECC_Scrub mode enabled. Error checking and status reporting is enabled. Data destined for the PCI/AGP and memory (RMR) is corrected. The memory contents are corrected (scrubbed) after all reads with errors.
9–8	ECC_Status	**Error Correcting Code Status** This bit field indicates the status of the ECC detect logic as follows: 00 = No error X1 = MED: multi-bit error detect 1X = SED: single-bit error detect The ECC status bits and corresponding failing chip-select indicators are set by the first error detected of each type (SED or MED). The AMD-761 system controller does not log any new errors of each type or assert SERR# until software clears the associated ECC_Status bit by writing a 1.

Bit Definitions (Continued) **ECC Mode/Status (Dev0:F0:0x48)**

Bit	Name	Function
7–4	ECC_CS_MED	**Multiple Bit Error Chip Select** These bits provide the binary encoded chip select for the first multiple-bit error detected by the AMD-761™ system controller.
3–0	ECC_CS_SED	**Single Bit Error Chip Select** These bits provide the binary encoded chip select for the first single-bit error detected by the AMD-761 system controller.

Programming Notes

System software is responsible for decoding the binary encoded, failing chip-select information and identifying a corresponding physical DIMM location.

Some bits in this register are not initialized at reset. BIOS must initialize all bits in this register prior to attempting DRAM access.

PCI Control — Dev0:F0:0x4C

Bit	31	30	29	28	27	26	25	24
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	23	22	21	20	19	18	17	16
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	15	14	13	12	11	10	9	8
	Reserved					Reserved	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0
R/W	R					R	R	R

Bit	7	6	5	4	3	2	1	0
	Reserved		Reserved	Reserved	WSC_DIR (See Note.)	PCI_DT_En	PCI_OR_En	Func1_En
Reset	0	0	0	0	0	0	0	0
R/W	R			R	R/W	R/W	R/W	R/W

Register Description

This register controls various functions in the primary PCI and AGP interfaces.

Note: *The WSC_DIR configuration bit is implemented only in Revision B4 silicon and above. This bit is reserved and must be cleared in all previous silicon revisions.*

Bit Definitions **PCI Control (Dev0:F0:0x4C)**

Bit	Name	Function
31—4	Reserved	**Reserved**
3	WSC_DIR	**Write Snoop Complete Direction Control** This bit controls the direction and function of the Write Snoop Complete (WSC#) pin. Refer to the *AMD-761™ System Controller Datasheet*, order# 24088, for a full description of the WSC# pin. 0 = Bidirectional mode for use with Southbridges that drive WSC# as an output *and* sample WSC# as an input (such as the AMD-766™ peripheral bus controller). In this mode, the WSC# pin of the AMD-761 system controller defaults as an input and is driven by the Northbridge only after the pin is first asserted by the Southbridge. 1 = Unidirectional mode for use with Southbridges that only sample WSC# as an input. In this mode, the WSC# pin is always driven by the AMD-761 system controller. ***Note:*** *This bit is implemented only in silicon revision B4 and above. It is reserved in all previous silicon revisions and must be cleared.*
2	PCI_DT_En	**Delayed Transactions Enable (PCI)** 0 = Delayed transactions disabled on the PCI interface 1 = Delayed transactions enabled on the PCI interface
1	PCI_OR_En	**Ordering Rules Compliance Enable (PCI)** This bit controls how the AMD-761 system controller PCI bus interface orders transactions. 0 = PCI ordering rules compliance disabled 1 = PCI ordering rules compliance enabled
0	Func1_En	**Function 1 Enable** This bit controls access to device 0, function 1 configuration space (DDR PDL registers). Refer to "Device 0, Function 1: DDR PDL Configuration Registers" on page 97 for more information on the function 1 registers. 0 = Device 0, function 1 disabled 1 = Device 0, function 1 enabled

Programming Notes

If the target latency bit is set (bit 23 of Dev 0:F0:0x84), then the delayed transactions enable (bit 2) must be set when the front-side bus is clocked at 66 MHz.

When enabling PCI ordering rules compliance, it is recommended that delayed transactions be enabled simultaneously for optimal performance.

Refer to See Chapter 5, "PCI Bus Interface" on page 195 for more information on the transaction options in the AMD-761 system controller. Refer to See Chapter 7, "Recommended BIOS Settings" on page 211 for the recommended bit settings for these bits.

Note that the WSC_DIR pin is implemented only in silicon revisions B4 and above and must be treated as Reserved (write a 0) in all other silicon revisions.

AMD Athlon™ Processor System Bus Dynamic Compensation Dev0:F0:0x50

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	PVal				NVal			
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	BYP_P				BYP_N			
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	SlewCntl			BYP	Reserved			
Reset	0	1	1	0	0	0	0	0
R/W	R/W			R/W	R			

Register Description

Note that the default value of the BYP, BYP_P, and BYP_N fields of this register can be optionally controlled by SIP bits when loading the SIP stream from external ROM.

Bit Definitions **AMD Athlon™ System Bus Dynamic Compensation (Dev0:F0:0x50)**

Bit	Name	Function
31–24	Reserved	**Reserved**
23–20	Pval	**P Transistor Strength Value** This field reflects the P transistor strength value that was automatically written to the AMD Athlon™ processor system bus I/O pads by the auto-compensation circuit. In bypass mode (bit 4=1) this field returns the values in the BYP_P field (bits [15:12]). The P values are active Low.
19–16	NVal	**N Transistor Strength Value** This field reflects the N transistor strength value that was automatically written to the AMD Athlon processor system bus I/O pads by the auto-compensation circuit. In bypass mode (bit 4=1) this field returns the values in the BYP_N field (bits [11:8]). The N values are active High.
15–12	BYP_P	**Bypass Values P Driver** Bypass strength values for the P driver. The P values are active Low. A value of 0 on bit 3 for instance signifies that (2^3 + 1) or 9 legs of the P driver are active.
11–8	BYP_N	**Bypass Values N Driver** Bypass strength values for the N driver. The N values are active High. A value of 1 on bit 3, for instance signifies that (2^3 + 1) or 9 legs of the N driver are active.
7–5	SlewCntl	**Slew Rate Control** Slew rate control for AMD Athlon processor system bus. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 (default) 100 = Slew rate 4 101= Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
4	BYP	**Bypass** Setting the bypass bit allows an external drive strength setting to be provided in the BYP_P and BYP_N fields. Clearing this bit causes the drive strength to be provided by the compensation circuit.
3-0	Reserved	**Reserved**

Programming Notes

DRAM Timing — Dev0:F0:0x54

	31	30	29	28	27	26	25	24
Bit	SBPWaitState	AddrTiming_A	AddrTiming_B	RD_Wait_State	Reg_DIMM_En	t_{WTR}	t_{WR}	
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	t_{RRD}	Reserved				Idle_Cyc_Limit		
Reset	X	0	0	0	0	X	X	X
R/W	R/W	R				R/W		

	15	14	13	12	11	10	9	8
Bit	PH_Limit		Reserved		t_{RC}			t_{RP}
Reset	X	X	0	0	X	X	X	X
R/W	R/W		R		R/W			

	7	6	5	4	3	2	1	0
Bit	t_{RP}	t_{RAS}			t_{CL}		t_{RCD}	
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

Register Description

This register defines the DRAM timing parameters for all banks. BIOS software must set appropriate values in this register before setting the SDRAM_Init bit (See "Bit Definitions DRAM Mode/Status (Dev0:F0:0x58)" on page 57) or attempting any DRAM accesses.

Note that this register is not initialized at reset time, and all bits must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **DRAM Timing (Dev0:F0:0x54)**

Bit	Name	Function
31	SBP_Wait_State	**Super Bypass Wait State** This bit forces a wait state on all super bypass reads. This bit should be set when the bus speed is 133 MHz (refer to Table 8 on page 55). 0 = No additional wait state on super bypass reads 1 = Add wait state on super bypass reads
30	AddrTiming_A	**Address Timing for Copy-A** This bit determines whether an extra delay is added to the address and command buses (MAA[14:0], RASA#, CASA#; WEA#, CKEA, CS[5:4, 1:0]#). This bit should be programmed depending on the loading presented to these pins. 0 = No extra delay 1 = XX ps delay
29	AddrTiming_B	**Address Timing for Copy-B** This bit determines whether an extra delay is added to the address and command buses (MAB[14:0], RASB#, CASB#; WEB#, CKEB, CS[7:6, 3:2]#). This bit should be programmed depending on the loading presented to these pins. 0 = No extra delay 1 = XX ps delay
28	RD_Wait_State	**Read Wait State** This bit determines whether a wait state must be added before returning the read data from the memory to the requester. This bit should be programmed depending on the overall round-trip timing. Note that this bit must be set for 100-MHz and 133-MHz operation, but it must **not** be set for 66-MHz operation (refer to Table 8). 0 = No wait states 1 = One wait state
27	Reg_DIMM_En	**Registered DIMM Enable** This bit enables the use of registered DIMMs on the motherboard. AMD-761™ system controller 0 = Unbuffered DIMMs 1 = Registered DIMMs
26	t_{WTR}	**Write Data In to Read Command Delay** This bit controls the number of clock cycles that must occur between the last valid write operation and the next read command. 0 = t_{WTR} duration is 1 clock cycle. 1 = t_{WTR} duration is 2 clock cycles.

Bit Definitions (Continued) **DRAM Timing (Dev0:F0:0x54)**

Bit	Name	Function
25-24	t_{WR}	**Write Recovery Time** This bit field controls the number of clock cycles that must occur from the last valid write operation to the earliest time a new precharge command can be asserted to the same bank. 00 = t_{WR} duration is 1 clock cycle. 01 = Reserved 10 = t_{WR} duration is 2 clock cycles. 11 = t_{WR} duration is 3 clock cycles.
23	t_{RRD}	**Activate Bank A to Activate Bank B Command Delay** This bit controls the number of clock cycles between successive activate commands to different banks. 0 = t_{RRD} duration is 2 clock cycles. 1 = t_{RRD} duration is 3 clock cycles.
22-19	Reserved	**Reserved**
18–16	Idle_Cyc_Limit	**Idle Cycle Limit** This bit field controls the number of idle cycles to wait before precharging an idle bank. Idle cycles are defined as cycles in which no valid requests are asserted. 111 = Disable idle precharge 110 = 48 cycles 101 = 32 cycles 100 = 24 cycles 011 = 16 cycles 010 = 12 cycles 001 = 8 cycles (recommended “safe” configuration) 000 = 0 cycles
15–14	PH_Limit	**Page Hit Limit** This bit field controls the number of consecutive page hit requests to allow before choosing a non-PH request. 00 = 1 cycle 01 = 4 cycle 10 = 8 cycles (recommended “safe” configuration) 11 = 16 cycles
13–12	Reserved	**Reserved**

Bit Definitions (Continued) **DRAM Timing (Dev0:F0:0x54)**

Bit	Name	Function
11–9	t_{RC}	**t_{RC}** This bit field indicates the t_{RC} timing value (bank cycle time: minimum time from activate to activate of same bank). 111 = 10 cycles 110 = 9 cycles 101 = 8 cycles (recommended "safe" configuration) 100 = 7 cycles 011 = 6 cycles 010 = 5 cycles 001 = 4 cycles 000 = 3 cycles
8–7	t_{RP}	**t_{RP}** This bit field indicates the t_{RP} timing value (precharge time: time from precharge to activate on the same bank). 00 = 3 cycles (recommended "safe" configuration) 01 = 2 cycles 10 = 1 cycles 11 = 4 cycles
6–4	t_{RAS}	**t_{RAS}** This bit field indicates the t_{RAS} timing value (minimum bank active time: time from activate to precharge of same bank). 111 = 9 cycles 110 = 8 cycles 101 = 7 cycles (recommended "safe" configuration) 100 = 6 cycles 011 = 5 cycles 010 = 4 cycles 001 = 3 cycles 000 = 2 cycles
3–2	t_{CL}	**CAS Latency of SDRAM** 11 = Reserved 10 = 2.5 cycles 01 = 2 cycles (recommended "safe" configuration) 00 = 3 cycles

Bit Definitions (Continued) **DRAM Timing (Dev0:F0:0x54)**

Bit	Name	Function
1–0	t_{RCD}	**t_{RCD}** This bit field (t_{RCD}) is the timing value (RAS to CAS latency, delay from activate to RD/WR command). 11 = 4 cycles 10 = 3 cycles (recommended "safe" configuration) 01 = 2 cycles 00 = 1 cycle

Programming Notes

This register is not initialized at reset. BIOS must initialize all bits in this register prior to setting the SDRAM_Init bit (See "Bit Definitions DRAM Mode/Status (Dev0:F0:0x58)" on page 57) or attempting DRAM access for correct operation.

The required settings for the wait state bits for SBP_Wait_State and Rd_Wait_State are listed in Table 8.

Table 8. Wait State Settings for DRAM Timing Register

DDR Interface Frequency	SBP_Wait_State [Bit 31]	Rd_Wait_State [Bit 28]
66 MHz	0	0
100 MHz	0	1
133 MHz	1	1

DRAM Mode/Status — Dev0:F0:0x58

	31	30	29	28	27	26	25	24
Bit	Clk_Dis5	Clk_Dis4	Clk_Dis3	Clk_Dis2	Clk_Dis1	Clk_Dis0	SDRAM_Init	Reserved
Reset	0	0	0	0	0	0	0	0
R/W	R/W						R/W1S	R

	23	22	21	20	19	18	17	16
Bit	Mode_Reg _ Status	STR_Control		Burst_Ref_En	Ref_Dis		Cyc_Per_Ref	
Reset	0	0	0	X	X	X	X	X
R/W	R/W1S	R/W						

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	CS7_X4Mode	CS6_X4Mode	CS5_X4Mode	CS4_X4Mode	CS3_X4Mode	CS2_X4Mode	CS1_X4Mode	CS0_X4Mode
Reset	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Description

This register provides general mode control and status reporting of the DRAM system.

Note that some bits of this register are not initialized at reset time, and all bits must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **DRAM Mode/Status (Dev0:F0:0x58)**

Bit	Name	Function
31	Clk_Dis5	**Clock Disable** This bit controls the DDR CLKOUT5/CLKOUT5# differential clock pair: 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*
30	Clk_Dis4	**Clock Disable** This bit controls the DDR CLKOUT4/CLKOUT4# differential clock pair. 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*
29	Clk_Dis3	**Clock Disable** This bit controls the DDR CLKOUT3/CLKOUT3# differential clock pair. 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*
28	Clk_Dis2	**Clock Disable** This bit controls the DDR CLKOUT2/CLKOUT2# differential clock pair. 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*
27	Clk_Dis1	**Clock Disable** This bit controls the DDR CLKOUT1/CLKOUT1# differential clock pair. 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*
26	Clk_Dis0	**Clock Disable** This bit controls the DDR CLKOUT0/CLKOUT0# differential clock pair. 0 = Clock pair enabled 1 = Clock pair disabled (three-stated) ***Note:*** *This bit is meant to disable the clock pair when it is not connected to anything. This bit should not be used for memory sizing or power management uses.*

Bit Definitions (Continued) **DRAM Mode/Status (Dev0:F0:0x58)**

Bit	Name	Function
25	SDRAM_Init	**SDRAM Initialization** This bit is used by the BIOS to tell the SDRAM controller to start the SDRAM initialization sequence. Once set, this bit cannot be reset. The BIOS should first program the SDRAM timing registers and set the output buffer drive strength. After that, it should set this bit.
24	Reserved	**Reserved**
23	Mode_Reg_Status	**Mode Register Status** 0 = Off/done 1 = Set When clear, the Mode register write is disabled and/or Mode register write done. When set, the Mode register write is enabled. Configuration bits t_{CL} must be set before this bit is asserted. BIOS software sets this bit for write to the SDRAM Mode register. The memory controller clears this bit when it has issued the Mode register write to the SDRAM.
22–21	STR_Control	**Suspend to RAM Control** These bits are used to allow the BIOS to communicate the power-up sequence to the AMD-761™ system controller memory controller and power management logic, as follows: 00 = Default. These bits are cleared to this state any time the RESET# pin is asserted. The AMD-761 memory controller always drives the CKE pins inactive (Low) while these bits are Low. 01 = BIOS sets this pattern after the system resumes from S4 (suspend to disk), S5 (soft off), or mechanical off states. This action causes the AMD-761 memory controller to assert the CKE pins and follow the normal sequence for DDR DRAM initialization after power-on. 1X = BIOS sets this pattern when the system is resuming from the S3 (suspend to RAM) state. This action causes the AMD-761 memory controller to exit self-refresh while preserving all memory data.
20	Burst_Ref_En	**Burst Refresh Enable** 0 = AMD-761 system controller does not burst refreshes. 1 = AMD-761 system controller queues up to four refreshes before issuing. Refreshes are only queued during long sequences of operations to the same memory device.
19	Ref_Dis	**Refresh Disable** This bit is provided for system debug, and should be cleared for normal operation. 0 = Refresh enabled (normal operation) 1 = Refresh disabled (debug only)
18		**Reserved**

Bit Definitions (Continued) **DRAM Mode/Status (Dev0:F0:0x58)**

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>17–16</td><td>Cyc_Per_Ref</td><td>Cycles Per Refresh
Refresh counter defines period of refresh requests.
The following table shows the relationship between the values in this field and the resultant refresh period for the different system clock frequencies:
<table><tr><th>Value</th><th>66 MHz</th><th>100 MHz</th><th>133 MHz</th></tr><tr><td>00</td><td>30.72 µs</td><td>20.48 µs</td><td>15.36 µs</td></tr><tr><td>01</td><td>23.04 µs</td><td>15.36 µs</td><td>11.52 µs</td></tr><tr><td>10</td><td>15.36 µs</td><td>10.24 µs</td><td>7.68 µs</td></tr><tr><td>11</td><td>7.68 µs</td><td>7.68 µs</td><td>3.84 µs</td></tr></table></td></tr>
<tr><td>15–8</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>7</td><td>CS7_X4Mode</td><td>Chip-Select 7 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>6</td><td>CS6_X4Mode</td><td>Chip-Select 6 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>5</td><td>CS5_X4Mode</td><td>Chip-Select 5 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>4</td><td>CS4_X4Mode</td><td>Chip-Select 4 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>3</td><td>CS3_X4Mode</td><td>Chip-Select 3 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>2</td><td>CS2_X4Mode</td><td>Chip-Select 2 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>1</td><td>CS1_X4Mode</td><td>Chip-Select 1 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
<tr><td>0</td><td>CS0_X4Mode</td><td>Chip-Select 0 X4Mode Enable
0 = This chip select consists of non-x4 devices (disabled).
1 = This chip select consists of x4 devices (enabled).</td></tr>
</table>

Programming Notes

Note that some bits of this register are not initialized at reset time, and all bits must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

The Clk_Dis bits are cleared by RESET#, and therefore all DDR DRAM interface clock pairs are enabled when exiting the Advanced Configuration and Power Interface (ACPI) S3 sleep state (suspend to RAM). BIOS should disable any clock pairs that are connected to unpopulated DIMM slots upon exit of S3.

When a chip select is programmed to operate in x4 DIMM mode, the DM[8:0] pins become DQS pins for that chip select. The pad configuration for the DM[8:0] pins is automatically controlled by the DQS_Drive field (Dev 0:F0:0x40) instead of the MDAT_Drive field, when **any** chip select is configured for x4 DIMM mode.

BIU0 Status/Control — Dev0:F0:0x60

Bit	31	30	29	28	27	26	25	24
	Prb_En	Reserved	Reserved	Reserved	Xca_Prb_Cnt			Xca_RD_Cnt
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	23	22	21	20	19	18	17	16
	Xca_RD_Cnt		Xca_WR_Cnt			Halt_Discon_En	Stp_Grant_Discon_En	Prb_Limit
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	15	14	13	12	11	10	9	8
	Prb_Limit		Ack_Limit				Bypass_En	SysDC_Out_Dly
Reset	0	0	0	0	1	1	0	Pinstrapping
R/W	R/W		R				R/W	R

Bit	7	6	5	4	3	2	1	0
	SysDC_Out_Dly	SysDC_In_Dly				WR2_RD	RD2_WR	
Reset	Pinstrapping							
R/W	R							

Register Description

This register provides general status and control for the AMD Athlon™ processor system bus interface.

Bit Definitions **BIU0 Status/Control (Dev0:F0:0x60)**

Bit	Name	Function
31	Prb_En	**Probe Enable** 0 = Probes are not sent to this processor. 1 = Probes are sent to this processor.
30	Reserved	This bit must be programmed to zero for normal operation.
29	Reserved	This bit must be programmed to zero for normal operation.
28	Reserved	This bit must be programmed to zero for normal operation.
27–25	Xca_Prb_Cnt	**Xca Probe Count** This bit field represents the maximum number of consecutive AMD Athlon™ processor system bus grants for probe data movement types that are allowed before letting another type have the bus.BIOS must program this field to a non-zero value for proper operation. The recommended value to be loaded in this field by BIOS software is 0x2.
24–22	Xca_RD_Cnt	**Xca Read Count** This bit field represents the maximum number of consecutive AMD Athlon processor system bus grants for read data movement types that are allowed before letting another type have the bus.BIOS must program this field to a non-zero value for proper operation. The recommended value to be loaded in this field by BIOS software is 0x6.
21–19	Xca_WR_Cnt	**Xca Write Count** This bit field represents the maximum number of consecutive AMD Athlon processor system bus grants for write data movement types that are allowed before letting another type have the bus.BIOS must program this field to a non-zero value for proper operation. The recommended value to be loaded in this field by BIOS software is 0x6.
18	Halt_Discon_En	**Halt Disconnect Enable** 0 = No AMD Athlon system bus disconnect is performed following HALT. 1 = AMD Athlon system bus disconnects after receiving a HALT special cycle.
17	Stp_Grant_ Discon_En	**Stop Grant Disconnect Enable** 0 = No AMD Athlon processor system bus disconnect is performed following STOP/GRANT. 1 = AMD Athlon processor system bus disconnects after receiving a STOP/GRANT special cycle.
16–14	Prb_Limit	**Probe Limit** BIOS software initializes this field with the maximum number of outstanding probes that the given CPU can handle. The default is a single probe. Encoding is as follows: 0b000 = 1 probe 0b001 = 2 probes ..... 0b111 = 8 probes
13–10	Ack_Limit	**Ack Limit** BIOS software reads this field to determine how many outstanding unacknowledged AMD Athlon processor system bus commands can be sent to the AMD-761™ system controller. The AMD-761 system controller allows a maximum of four unacknowledged commands. Encoding is as follows: 0b0000 = 1 unacknowledged command 0b0001 = 2 unacknowledged commands ..... 0b1111 = 16 unacknowledged commands

Bit Definitions (Continued) **BIU0 Status/Control (Dev0:F0:0x60)**

Bit	Name	Function
9	Bypass_En	**Bypass Enable** When set, the AMD-761™ system controller internally bypasses certain memory pipe stages for optimal performance. This bit may be set only if both of the following are true: 1. System is single processor or it is two processors and only CPU0 is present, and 2. CPU clock multiplier is 4 or greater. See "Config Status" on page 74 to determine the clock multiplier (FID).
8–7	SysDC_Out_Dly	**SysDC Out Delay** This bit field specifies the number of SysClk cycles from a return of read data type SysDC command and the start of the corresponding data. 0b00 = Reserved 0b01 = 1 clock 0b10 = 2 clocks 0b11 = 3 clocks This field is initialized by pinstrapping during reset.
6–3	SysDC_In_Dly	**SysDC In Delay** This bit field specifies the number of SysClk cycles from a write data type SysDC command and the start of the corresponding data. 0b0000 = 1 clock 0b0001 = 2 clocks ..... 0b1111 = 16 clocks This field is initialized by pinstrapping during reset.
2	WR2_RD	**WR2 Read** This field defines the number of SysClk cycles that are inserted between write data and read data cycles to allow the AMD Athlon™ processor system bus data wires to turn around. This field is initialized by pinstrapping during reset.
1–0	RD2_WR	**RD2 Write** This field defines the number of SysClk cycles that are inserted between read data and write data cycles to allow the AMD Athlon processor system bus data wires to turn around. This field is initialized by pinstrapping during reset.

Programming Notes

BIU0 SIP — Dev0:F0:0x64

	31	30	29	28	27	26	25	24
Bit	Clk_Fwd_Offset	Data_Init_Cnt		Addr_Init_Cnt		Sys_Data_Even_Clk_Dly		
Reset	0	Pinstrapping						
R/W	R/W	R						

	23	22	21	20	19	18	17	16
Bit	Sys_Data_Odd_Clk_Dly			Sys_Data_Even_Dly		Sys_Data_Odd_Dly		Sys_Addr_Dly
Reset	Pinstrapping							
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Sys_Addr_Dly	SysDC_Dly				Sys_Addr_Clk_Dly		
Reset	Pinstrapping							
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Sys_Rst_Clk_Offset		Sys_Data_Rec_Mux_PreLd			Sys_Addr_Rec_Mux_PreLd		
Reset	0	0	Pinstrapping					
R/W	R							

Register Description

This register provides visibility to the serial initialization packet delivered to the AMD Athlon™ processor during the AMD Athlon processor system bus connect protocol.

Bit Definitions **BIU0 SIP (Dev0:F0:0x64)**

Bit	Name	Function
31	Clk_Fwd_Offset	**Clock Forward Offset** 0 = The AMD-761™ system controller delays driving of the data and clock for AMD Athlon™ processor system bus SysData bits [31:16] and [63:48] by ~1000 ps. 1 = All AMD Athlon system bus ClkFWD groups drive the same nominally SysClk edge.
30–29	Data_Init_Cnt	**Data Initialization Count** This value specifies the number of SysClks from the launch of data by the processor until it can be read from the AMD-761 system controller receive FIFO.
28–27	Addr_Init_Cnt	**Address Initialization Count** This value specifies the number of SysClks from the launch of a command by the processor until it can be read from the AMD-761 system controller receive FIFO.
26–24	Sys_Data_Even _Clk_Dly	**System Data Even Clock Delay --** AMD Athlon processor SIP[33:31] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the even clocks.
23–21	Sys_Data_Odd _Clk_Dly	**System Data Odd Clock Delay --** AMD Athlon processor SIP[30:28] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the odd clocks.
20–19	Sys_Data_Even _Dly	**System Data Even Delay --** AMD Athlon processor SIP[27:26] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the even data (SysData bits [31:16] and [63:48]).
18–17	Sys_Data_Odd _Dly	**System Data Odd Delay --** AMD Athlon processor SIP[25:24] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the odd data (SData bits [15:00] and [47:32]).
16–15	Sys_Addr_Dly	**System Address Delay --** AMD Athlon processor SIP[23:22] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the address (SysAddOut).
14–11	SysDC_Dly	**SysDC Delay --** AMD Athlon processor SIP[19:16] This value is an internal processor parameter that is used to cause SYSDC commands and their associated data to arrive in the processor core at the correct relative times.
10–8	Sys_Addr_Clk _Dly	**System Addr Clock Delay --** AMD Athlon processor SIP[13:11] This value specifies the number of processor XICLK phases between the nominal start of bit time and the launch of the SADDOUTCLK.
7–6	Sys_Rst_Clk _Offset	**System Reset Clock Offset --** AMD Athlon processor SIP[10:9] This value is an internal processor parameter that is used to properly time AMD Athlon system bus data transfer.
5–3	Sys_Data_Rec _Mux_PreLd	**System Data Rec Mux PreLd --** AMD Athlon processor SIP[8:6] This value specifies the number of SysClk phases from the launch of data by the AMD-761 system controller until it can be read from the AMD Athlon receive FIFO.
2–0	Sys_Addr_Rec _Mux_PreLd	**System Address Rec Mux PreLd --** AMD Athlon processor SIP[5:3] This value specifies the number of SysClk phases from the launch of address/command by the AMD-761 system controller until it can be read from the AMD Athlon receive FIFO.

Programming Notes

Memory Status/Control — Dev0:F0:0x70

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved					Self_Ref_En		
Reset	0	0	0	0	0	X	0	0
R/W	R					R/W		

	15	14	13	12	11	10	9	8
Bit				Reserved		PCI_Pipe_En	PCI_Blk_WR_En	Reserved
Reset	0	0	0	0	0	0	0	0
R/W	R/W			R		R/W		R

	7	6	5	4	3	2	1	0
Bit	Reserved			Reserved	Reserved	Reserved	Reserved	Reserved
Reset	0	0	0	0	0	0	0	0
R/W	R			R				R

Register Description

This register provides general status and control for the memory controller.

Note that the Self_Ref_En bit in this register is not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **Memory Status/Control (Dev0:F0:0x70)**

Bit	Name	Function
31–19	Reserved	**Reserved**
18	Self_Ref_En	**Self-Refresh Enable** This bit enables self-refresh when entering certain power management states. This bit should normally be set, but the option to disable this function is provided to accommodate specific DIMMs that do not correctly support the self-refresh feature. Note that if this bit is not set, then DCSTOP# assertion (ACPI sleep states) must be inhibited. 0 = Self-refresh disabled 1 = Self-refresh enabled
17–14		**Reserved**
13		**Reserved**
12–11	Reserved	**Reserved**
10	PCI_Pipe_En	**PCI Pipe Enable** 0 = All PCI transactions, from either the PCI or AGP interfaces, force the memory controller to check for outstanding read probes with a matching block address and stall until these probes are complete. 1 = Memory controller pipelines PCI transactions. Setting this bit generally increases PCI throughput. This bit must be clear when the processor is allowed to issue CleanVictimBlock commands.
9	PCI_Blk_WR_En	**PCI Block Write Enable** 0 = PCI full-block writes do RID/INV probes, forcing the memory controller to wait for probe data movement. 1 = PCI full-block writes do NOP/INV probes. This bit must be clear when the AMD Athlon™ processor is allowed to issue CleanVictimBlock commands.
8–1	Reserved	**Reserved**
0	Reserved	**Reserved**

Programming Notes

Note that the Self_Ref_En bit in this register is not initialized at reset time but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

DCSTOP# assertion (ACPI S1/S3) must not be enabled if the Self_Ref_En bit is cleared.

Who Am I (WHAMI) Dev0:F0:0x80

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved				Reserved	Reserved	Reserved	BIU0_Present
Reset	0	0	0	0	0	0	0	From CPU
R/W	R							

	15	14	13	12	11	10	9	8
Bit	FirstBusID							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	WHAMI							
Reset	CPUID							
R/W	R							

Register Description

Bit Definitions **Who Am I (WHAMI) (Dev0:F0:0x80)**

Bit	Name	Function
31-17	Reserved	**Reserved**
16	BIU0_Present	**BIU0 Present** This bit, when set, indicates that a processor is installed on the specified AMD Athlon™ processor system bus port on the AMD-761™ system controller and it has requested a connect sequence (ProcRdy assertion).
15–8	FirstBusID	**First BusID** This field contains the AMD Athlon processor system bus ID of the first processor to read this register: 00h if CPU0 was the first to read WHAMI after reset, 01h if CPU1 was the first to read WHAMI after reset.
7–0	WHAMI	**Who Am I** This field returns the AMD Athlon processor system bus ID (below) of the processor that accesses it: 00h for CPU0, 01h for CPU1.

Programming Notes

PCI Arbitration Control — Dev0:F0:0x84

	31	30	29	28	27	26	25	24
Bit	AGP_VGA_BIOS							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	Tgt_Latency	Reserved				Reserved	AGP_Chain_En	PCI_Chain_En
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R				R	R/W	R/W

	15	14	13	12	11	10	9	8
Bit	MDA_Debug	PCI_WR_Post_Rtry	AGP_WR_Post_Rtry	RD_Data_Err_Dis	AGP_Erly_Prb_Dis	PCI_Erly_Prb_Dis	AGP_Arb_Pipe_Dis	SB_Lock_Dis
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	PM_Reg_En	15M_Hole	14M_Hole	EV6_Mode	Tgt_Lat_Tim_Dis	AGP_Pref_En	PCI_Pref_En	Park_PCI
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Register Description

This register provides general PCI arbiter mode control.

Bit Definitions **PCI Arbitration Control (Dev0:F0:0x84)**

Bit	Name	Function
31–24	AGP_VGA_BIOS	**AGP VGA BIOS** These bits when set indicate that the corresponding (16-KByte) segment should be mapped to the AGP PCI bus. Bit 24 corresponds to the addresses 0xC0000–0xC3FFF and bit 31 maps addresses 0xDC000–0xDFFFF to the AGP PCI interface. Set one or more of these bits if the AGP graphics card has a ROM BIOS.
23	Tgt_Latency	**Target Latency** This bit is designed to ensure that the AMD-761™ system controller is compliant to the PCI maximum target latency rule. Note that this compliance applies only to the PCI bus and not the AGP bus. 0 = AMD-751™ system controller-compatible, the AMD-761 system controller does not disconnect a master when it cannot service a read request within 32 PCI clock periods (initial latency) or 8 clocks (subsequent data cycles). 1 = If the AMD-761 system controller cannot respond to a memory read within 32 clocks for the initial access, or 8 clocks for each subsequent access, it forces a retry. ***Note:*** *To prevent potential deadlocks, set this bit and clear bit 3 (Tgt_Lat_Tim_Dis) if the system has PCI to AGP traffic.*
22–18	Reserved	**Reserved**
17	AGP_Chain_En	**Enable AGP Chaining** When set, CPU writes to the AGP bus are chained together.
16	PCI_Chain_En	**Enable PCI Chaining** When set, CPU writes to PCI are chained together.
15	MDA_Debug	**MDA Debug** This bit allows monochrome display adapters (MDA) to be used simultaneously with AGP cards for debug of AGP device drivers. The behavior of the AMD-761 system controller display adapters is a function of this bit and the VGA Enable in (D1:0x3C[19]) as follows: MDA address ranges: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh VGA = 0, MDA = 0: all MDA and VGA references go to PCI VGA = 0, MDA = 1: operation undefined VGA = 1, MDA = 0: all VGA references go to AGP, MDA only (I/O 3BFh) goes to PCI VGA = 1, MDA = 1: all VGA references go to AGP, all MDA (including memory) go to PCI
14	PCI_WR_Post _Rtry	**PCI Write Post Retry** When set, this bit enables retries on PCI if there are pending posted writes.
13	AGP_WR_Post _Rtry	**AGP Write Post Retry** When set, this bit enables retries on the AGP bus if there are pending posted writes.

Bit Definitions (Continued) **PCI Arbitration Control (Dev0:F0:0x84)**

Bit	Name	Function
12	RD_Data_Err_ Dis	**Read Data Error Disable** Whenever a cycle from a processor to the PCI or AGP buses results in a master abort (except special cycles), the AMD-761™ system controller returns a read data error indicator to the processor. When set, this bit causes data value of all 1s to be returned. When clear, an AMD Athlon™ processor system bus read data error response is returned. The CPU response to read data error is determined by the settings of the Machine Check Architecture registers in the processor.
11	AGP_Erly_Prb_ Dis	**AGP Early Probe Disable** As soon as the AMD-761 system controller detects a PCI write cycle to memory from an external AGP master, it sends a "probe only" request to the processor that is used to flush data from the processor cache. After one or more data phases, a write request is sent to the memory, which also results in a probe. When set, this bit disables the early probe from an AGP master running a PCI write cycle to memory.
10	PCI_Erly_Prb_ Dis	**PCI Early Probe Disable** This bit is similar AGP_Erly_Prb_Dis and can disable early probe requests for write cycles from an external master on the standard PCI bus.
9	AGP_Arb_Pipe_ Dis	**AGP Arbiter Pipe Disable** When set, this bit disables the AGP arbiter from pipelining grants onto the bus.
8	SB_Lock_Dis	**Southbridge Lock Disable** When the Southbridge makes a request for the PCI bus, the AMD-761 system controller makes sure that all the previous posted requests from the processors and PCI are completed by the memory before granting the bus to the Southbridge. When set, this bit disables this flushing of previous requests.
7	PM_Reg_En	**Power Management Register Enable** This bit, when set, enables reading from and writing to the power management register (at BAR2).
6	15M_Hole	**15M Memory Hole** When set, this bit creates a hole in memory from 15 Mbytes to 16 Mbytes. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range.
5	14M_Hole	**14M Memory Hole** When set, this bit creates a hole in memory from 14 Mbytes to 15 Mbytes. This register is used by the PCI decode logic to know when to accept a cycle from an external PCI master. When set, the PCI decode logic does not assert a match for addresses falling in this range.
4	EV6_Mode	**EV6 Mode** When set, this bit indicates that the PCI interfaces have to decode memory hits in the EV6 mode. There are no memory holes and DMA can be done to any address that lies within the SDRAM map.

Bit Definitions (Continued) **PCI Arbitration Control (Dev0:F0:0x84)**

Bit	Name	Function
3	Tgt_Lat_Tim_ Dis	**Target Latency Timer Disable** When the AMD-761™ system controller acts as a PCI target, it has a latency timer that retries the (write) cycle if it cannot respond within 8 bus clocks (16 clocks for the first transfer). When set, this bit disables the AMD-761 system controller's target latency timer on both the standard PCI and AGP PCI interfaces. ***Note:*** *To prevent potential deadlocks caused by PCI to AGP traffic on the system, this bit should be cleared and bit 23 (Tgt_Latency) must be set. Note also that setting this bit disables the Tgt_Latency function controlled by bit 23.*
2	AGP_Pref_En	**AGP Prefetch Enable** When set, this bit enables the AMD-761 system controller to prefetch data from the SDRAM when a PCI master on the standard AGP bus reads from the main memory.
1	PCI_Pref_En	**PCI Prefetch Enable** When set, this bit enables the AMD-761 system controller to prefetch data from the SDRAM when a PCI master on the PCI bus reads from the main memory.
0	Park_PCI	**Park PCI** When set, this bit enables parking on an external PCI master. When clear, the PCI arbiter only parks on processor accesses to PCI.

Programming Notes

To avoid potential deadlocks for systems that use traffic from the PCI bus to the PCI bus of the AGP, clear the write target latency timer disable bit (bit 3, Tgt_Lat_Tim_Dis), and set the read target latency timer bit (bit 23, Tgt_Latency). Refer to the programming notes for the PCI Control register (Dev 0:F0:0x4C) for details on the recommended setting of the Tgt_Latency bit.

Config Status — Dev0:F0:0x88

	31	30	29	28	27	26	25	24
Bit	AGP_Clk_Mux			Sys_Clk_Mux			Type_Det	S2K_Thresh
Reset	x (from PCI AD[14:12])			x (from PCI AD[7:5])			x (from PCI AD[20])	x (from PCI AD[4])
R/W	R							

	23	22	21	20	19	18	17	16
Bit	K7_PP_En	IG_PP_En	Clk_Speed		Reserved		S2K0_Bus_Len	
Reset	x (from PCI C/BE[3]#)	x (from PCI C/BE[2]#)	x (from PCI AD[31:30])		x (from PCI AD[27:26])		x (from PCI AD[11:10])	
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Tristate_En	NAND_En	Bypass_PLLs	Dis_Divider	Reserved			
Reset	x (from PCI AD[25])	x (from PCI AD[23])	x (from PCI AD[9])	x (from PCI AD[29])	x (from PCI AD[19:16])			
R/W	R							

	7	6	5	4	3	2	1	0
Bit	SIP_ROM_En	GP_Strap	In_Clk_En	Out_Clk_En	CPU0_Divider			
Reset	x(from PCI C/BE[0]#)	x (from PCI AD[15])	x (from PCI AD[24])	x (from PCI AD[8])	x (from PCI AD[3:0])			
R/W	R							

Register Description

This register allows BIOS software to determine what system initialization states have been programmed by resistor pinstrappings on the motherboard.

Bit Definitions **Config Status (Dev0:F0:0x88)**

Bit	Name	Function
31–29	AGP_Clk_Mux	**AGP Clock Mux** For internal test only.
28–26	Sys_Clk_Mux	**System Clock Mux** For internal test only.
25	Type_Det	**Type Detect** 0 = This installed card in the AGP slot uses 1.5-V signalling. 1 = This installed card in the AGP slot uses 3.3-V signalling.
24	S2K_Thresh	**AMD Athlon™ Processor System Bus Threshold** AMD Athlon™ processor system bus threshold range select for AMD Athlon™ system bus I/O cells. When Low, these AMD Athlon processor system bus inputs sense input thresholds between 1.35 V and 1.9 V. When High, the inputs sense thresholds between 2.0 V and 2.2 V.
23	K7_PP_En	**AMD Athlon Processor Push-Pull Driver Enable** When set, this bit indicates that the AMD Athlon processor push-pull drivers are enabled.
22	IG_PP_En	**AMD-761™ System Controller Push-Pull Driver Enable** When set, this bit indicates that the AMD-761 system controller push-pull drivers are enabled.
21–20	Clk_Speed	**Clock Speed** This bit field defines the speed of the system clock received by the AMD-761 system controller: 00 = 100 MHz 01 = 66 MHz 10 = Reserved 11 = 133 MHz
19–18	Reserved	**Reserved**
17–16	S2K0_Bus_Len	**AMD Athlon Processor System Bus Length** This bit field indicates the relative length of the AMD Athlon processor system bus trace routing on the motherboard. 00 = Short 01..... 10..... 1 = Long
15	Tristate_En	**Tristate Enable** For internal test only.
14	NAND_En	**NAND Enable** For internal test only.

Bit Definitions (Continued) **Config Status (Dev0:F0:0x88)**

Bit	Name	Function
13	Bypass_PLLs	**Bypass PLLs** This bit is set for test and debug of the AMD-761™ system controller with the internal PLLs disabled. 0 = AMD-761 system controller PLLs enabled 1 = AMD-761 system controller PLLs bypassed; clocks driven from SYSCLK and AGPCLK pins directly to internal clock trees
12	Dis_Divider	**Disable Divider** For internal test only.
11–8	Reserved	**Reserved**
7	SIP_ROM_En	**SIP ROM Enabled** This bit indicates that the external SIP ROM is enabled and is read to create the SIP stream to the AMD Athlon processor, instead of the internally generated SIP table.
6	GP_Strap	**General-Purpose Strap** This bit may be used as a general-purpose strap for communicating motherboard- specific information to BIOS. The AMD-761 system controller does not use this strap internally.
5	In_Clk_En	**INCLK Enable** This bit indicates that the AMD-761 system controller delays the INCLK to the AMD Athlon processor. When reset, the motherboard is expected to provide delay in the etch to center the INCLK with the data.
4	Out_Clk_En	**OUTCLK Enable** This bit indicates that the AMD Athlon processor delays the OUTCLK to the AMD-761 system controller. When reset, the motherboard is expected to provide delay in the etch to center the OUTCLK with the data.
3–0	CPU0_Divider	**CPU Divider** This bit field contains the CPU clock multiplier field supplied by the processor. Together with the Clk_Speed field and the S2K0_Bus_Len field, these fields allow the AMD-761 system controller to properly program the AMD Athlon™ processor system bus initialization logic using the SIP protocol. The clock multiplier field is also known as the Frequency Identification (FID) bits and the values are shown below.

FID Value	Multiplier	FID Value	Multiplier	FID Value	Multiplier	FID Value	Multiplier
0000	11.0	0100	5.0	1000	7.0	1100	9.0
0001	11.5	0101	5.5	1001	7.5	1101	9.5
0010	12.0	0110	6.0	1010	8.0	1110	10.0
0011	12.5	0111	6.5	1011	8.5	1111	10.5

Programming Notes

PCI Top of Memory — Dev0:F0:0x9C

	31	30	29	28	27	26	25	24
Bit	PCI_Mem_Top							
Reset	1	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

This register is used to define the top of main system memory. It is used to compare the memory addresses of an external PCI master to determine if it is in the range of the AMD-761™ system controller DRAM. If the address compares, then the AMD-761 system controller responds to the bus master access with DEVSEL# assertion.

Bit Definitions **PCI Top of Memory (Dev0:F0:0x9C)**

Bit	Name	Function
31–24	PCI_Mem_Top	**PCI Memory Top** This 8-bit field is compared to the incoming PCI bus master address to determine if a memory cycle falls within the AMD-761™ system controller DRAM region, as follows: 31 30 29 28 27 26 25 24 PCIMemTop Field 31 30 29 28 27 26 25 24 PCI Address BIOS should write to this field following completion of the memory sizing algorithm, after it has determined the total size of the installed memory.
23–0	Reserved	**Reserved**

Programming Notes

AGP Capability Identifier — Dev0:F0:0xA0

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Major_Rev				Minor_Rev			
Reset	0	0	1	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Next_Pointer							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Cap_ID							
Reset	0	0	0	0	0	0	1	0
R/W	R							

Register Description

Bit Definitions — AGP Capability Identifier (Dev0:F0:0xA0)

Bit	Name	Function
31–24	Reserved	**Reserved**
23–20	Major_Rev	**Major Revision** Major revision of the AGP interface specification conformed to by this device.
19–16	Minor_Rev	**Minor Revision** Minor revision of the AGP interface specification conformed to by this device.
15–8	Next_Pointer	**Next Pointer** Pointer to the next item in the capabilities list. Must be null for the final item on the list.
7–0	Cap_ID	**CapID** This value indicates that this list item pertains to AGP registers.

Programming Notes

AGP Status — Dev0:F0:0xA4

	31	30	29	28	27	26	25	24
Bit	Max_ReqQ_Depth							
Reset	0	0	0	0	1	1	1	1
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved						SBA	Reserved
Reset	0	0	0	0	0	0	1	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved		R4G	FW	Reserved	Rates		
Reset	0	0	0	0	0	1	1	1
R/W	R							

Register Description

Bit Definitions **AGP Status (Dev0:F0:0xA4)**

Bit	Name	Function
31–24	Max_ReqQ_ Depth	**Maximum Command Requests** This field contains the maximum number of AGP command requests that this node can manage.
23–10	Reserved	**Reserved**
9	SBA	**Sideband Addressing** This field is always 1, indicating that the AMD-761™ system controller supports sideband addressing.
8–6	Reserved	**Reserved**
5	R4G	**Address Limit** This bit is always 0, indicating that the AMD-761 system controller does not support addresses greater than 4 Gbytes.
4	FW	**Fast Write Transfer** This bit indicates supports of fast write transfers. 0 = Fast writes not supported 1 = Fast writes supported
3	Reserved	**Reserved**
2–0	Rates	**Rate Transfers** This field indicates that the AMD-761 system controller supports 1x (bit[0]), 2x (bit[1]), and 4X (bit[2]) transfers.

Programming Notes

Fast writes are disabled by default and are indicated in the status bit that reports this capability. Setting the FW_Enable bit in the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4, bit 7) sets the FW bit in this register to indicate support of this feature. Fast writes are enabled when both the FW_Enable bit (in the AGP 4X Dynamic Compensation register) and the Fast_Writes bit in the AGP Command register are set.

AGP 4X transfers are supported and the 4X status bit is set by default in this register. This bit can be overridden by setting the 4X_Override bit in the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4, bit 6).

AGP Command — Dev0:F0:0xA8

Bit	31	30	29	28	27	26	25	24
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	23	22	21	20	19	18	17	16
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	15	14	13	12	11	10	9	8
	Reserved						SBA_En	AGP_En
Reset	0	0	0	0	0	0	0	0
R/W	R						R/W	

Bit	7	6	5	4	3	2	1	0
	Reserved		R4G_En	Fast_Writes	Reserved	Data_Transfer_Mode		
Reset	0	0	0	0	0	0	0	0
R/W	R			R/W	R	R/W		

Register Description

Bit Definitions **AGP Command (Dev0:F0:0xA8)**

Bit	Name	Function
31–10	Reserved	**Reserved**
9	SBA_En	**Sideband Addressing Enable** When this bit is set, sideband addressing is enabled.
8	AGP_En	**AGP Operations Enable** When this bit is set, the AMD-761™ system controller accepts AGP operations. When this bit is clear, the AMD-761 system controller ignores AGP operations.
7–6	Reserved	**Reserved**
5	R4G_En	**4GB Address Indicator** This bit indicates that the AMD-761 system controller does not support addresses greater than 4 Gbytes. The AMD-761 system controller supports only 32-bit addresses.
4	Fast_Writes	**Fast Writes** 0 = Fast writes disabled 1 = Fast writes enabled when the FW_Enable bit is also set in the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4, bit 7)
3	Reserved	**Reserved**
2–0	Data_Transfer _Mode	**Data Transfer Mode** Only one bit must be set in this field to indicate the desired AGP data transfer rate. 001 = 1X AGP rate 010 = 2X AGP rate 100 = 4X AGP rate

Programming Notes

AGP Virtual Address Space Size — Dev0:F0:0xAC

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							Vga_IA_En
Reset	0	0	0	0	0	0	0	0
R/W	R							R/W

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved				VA_Size			GART_En
Reset	0	0	0	0	0	0	0	0
R/W	R				R/W			

Register Description

Bit Definitions **AGP Virtual Address Space Size (Dev0:F0:0xAC)**

Bit	Name	Function
31–17	Reserved	**Reserved**
16	Vga_IA_En	**ISA Address Aliasing Enable** When set, this bit forces the AMD-761™ system controller to alias ISA addresses, which means that address bits [15:10] are not used in decoding. When clear, no ISA aliasing is performed and address bits [15:10] are used for decoding.
15–4	Reserved	**Reserved**
3–1	VA_Size	**Virtual Address Size** This field defines the virtual address space size to be allocated to GART by the system BIOS. Prior to the execution of the system BIOS memory mapping software, system BIOS gets the amount of GART virtual address space required by the graphics controller. It sets these bits to the required value. Changing these bits automatically changes bits [30:25] in the host-PCI bridge (device 0) AGP Virtual Address Space register, offset 0x10 (see "Dev0:F0:0x10" on page 37). The size of GART virtual address space is always greater than or equal to the amount of physical system memory allocated to AGP in non-contiguous 4-Kbyte blocks. The amount of physical memory allocated to AGP is determined by operating system software. [3] [2] [1] VA_Size 0 0 0 32 Mbytes 0 0 1 64 Mbytes 0 1 0 128 Mbytes 0 1 1 256 Mbytes 1 0 0 512 Mbytes 1 0 1 1 Gbytes 1 1 0 2 Gbytes
0	GART_En	**GART Enable** When clear, GART is not valid in this system. System BIOS does not allocate virtual address space for GART because the host-PCI bridge (device 0) AGP virtual address space, offset 0x10 (see "Dev0:F0:0x10" on page 37) is set to 0. The PCI-PCI bridge (device 1) capabilities pointer is set to point to the next item in the linked list or null if there is no other item. This bit is set by BIOS PCI enumeration routines. When set, GART is valid in this system. System BIOS allocates virtual address space for GART based upon the value in bits [3:1] above.

Programming Notes

GART/AGP Mode Control — Dev0:F0:0xB0

Bit	31	30	29	28	27	26	25	24
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	23	22	21	20	19	18	17	16
	Reserved				NonGART _Snoop		PDC_En	Lv1_Index
Reset	0	0	0	0	0	0	0	0
R/W	R			R/W				

Bit	15	14	13	12	11	10	9	8
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	7	6	5	4	3	2	1	0
	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

This register provides bits to control specific features of the AMD-761™ system controller AGP implementation.

Bit Definitions **GART/AGP Mode Control (Dev0:F0:0xB0)**

Bit	Name	Function
31–21	Reserved	**Reserved**
20		**Reserved**
19	NonGART_Snoop	**NonGART Snoop** When set, this bit forces AGP accesses that are not in the GART range to cause AMD Athlon™ processor system bus probes to the processor(s). When clear, AGP addresses that fall outside of the GART range do not cause probes.
18		**Reserved**
17	PDC_En	**Gart Page Directory Cache Enable** This bit is used only in the two-level GART mode. It has no effect in the one-level GART mode. The GART directory is enabled only when both this bit and the AGP Features Control register (offset 02h of the memory-mapped Features and Capabilities register—see "Bar1 + 0x00" on page 141) bit 2, "GART Cache Enable", are 1s.
16	Lv1_Index	**Level 1 Index (GART Index Scheme Control)** When set to 1, this bit enables the one-level GART mode. When cleared to 0, two-level GART mode is enabled.
15–0	Reserved	**Reserved**

Programming Notes

AGP 4X Dynamic Compensation — Dev0:F0:0xB4

Bit	31	30	29	28	27	26	25	24
	PVal				NVal			
Reset	X	X	X	X	X	X	X	X
R/W	R							

Bit	23	22	21	20	19	18	17	16
	Reserved	DisStrb	Quantum_Cnt					
Reset	0	0	0	0	0	0	0	1
R/W	R	R/W	R/W					

Bit	15	14	13	12	11	10	9	8
	Reserved				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R							

Bit	7	6	5	4	3	2	1	0
	FW_Enable	4X_Override	Comp3.3	Reserved		PCI	Always_ Compensate	Do_ Compensate
Reset	0	0	0	0	0	0	0	0
R/W	R/W			R		R/W		

Register Description

Bit Definitions **AGP 4X Dynamic Compensation (Dev0:F0:0xB4)**

Bit	Name	Function
31–28	PVal	**P Transistor Strength Value** This field reflects the P transistor strength value that was written to the non-strobed AGP I/O pads according to Table 9 on page 90.
27–24	NVal	**N Transistor Strength Value** This field reflects the N transistor strength value that was written to the non-strobed AGP I/O pads according to Table 9 on page 90.
23	Reserved	**Reserved**
22	DisStrb	**Disable Strobe** This bit allows the complimentary strobes ADSTB[1:0]# to be disabled when the AGP interface is operating in 2X mode. Setting this bit causes these pins to be driven High.
21–16	Quantum_Cnt	**Quantum Count** This field is used to determine the number of 100-ms intervals that elapse before a dynamic compensation event is performed when the AlwaysCompensate bit is set. The value allows for dynamic compensation time quantums to range from 100 ms to 6.4 s.
15–8	Reserved	**Reserved**
7	FW_Enable	**Fast Writes Override** 0 = Fast writes disabled 1 = Fast writes enabled (see below) AGP fast writes are enabled by a combination of this bit and the Fast_Writes enable bit in the AGP Command register (Dev 0:F0:0xA8, bit 4). The Fast_Writes status bit in the AGP Status register (Dev 0:F0:0xA4, bit 4) is 0 by default, indicating that the AMD-761™ system controller does not support this feature. Setting this bit forces the status bit to a 1 to indicate support of fast writes. The fast writes feature is enabled only when this bit and the Fast_Writes bit in the AGP Command register (Dev 0:F0:0xA8, bit 4) are set.
6	4X_Override	**AGP 4X Override** This bit can be set to override the value in the read-only AGP Status register (Dev 0:FD0:0xA4). By default the rates field of the AGP Status register report 4X capability, but setting this bit forces the 4X-capable bit to be 0, indicating a maximum of 2X support.
5	Comp3.3	**Compensate for 3.3-V Signalling** This bit overrides the TYPEDET# value to force an AGP auto-compensation in a 3.3-V signalling environment. This bit may be set in conjunction with the Do_Compensate bit to enable BIOS to determine which drive strength values the auto-compensation circuit selected for this motherboard. ***Note:*** *This bit must be set only while the AGP interface is **disabled**. Setting this bit while the AGP interface is enabled results in unpredictable behavior.*
4-3	Reserved	**Reserved**
2	PCI	**PCI** As shown in Table 9 on page 90, this bit, along with BYP and AGP2X bits, controls the drive strength of the output buffer and whether the input buffers are single-ended or differential.

Bit Definitions (Continued) **AGP 4X Dynamic Compensation (Dev0:F0:0xB4)**

Bit	Name	Function
1	Always_ Compensate	**Always Compensate** When set, dynamic compensation is performed by AGP on an ongoing basis at regular intervals.
0	Do_Compensate	**Do Compensate** This bit is used to initiate a dynamic compensation command on AGP. This bit is cleared by the AMD-761™ system controller when the compensation cycle is complete. See the programming note below on recommendation for exiting bypass mode.

Programming Notes

When transitioning from bypass enabled to disabled via the AGP Compensation Bypass register (Dev 0:F0:0xB8), the Do_Compensate bit should be set. AGP should not be subsequently enabled until the Do_Compensate bit is read back as a 0, indicating that the compensation cycle is complete.

Refer to the AGP Compensation Bypass register (Dev 0:F0:0xB8) for details of bypass mode.

Table 9. I/O Pad Drive Strength and Input Type

BYPASS	TYPEDET#	PCI	AGP Mode	Output Drive Strength
0	0	X	N/A	Compensated Strength
0	1	0	N/A	AGP-1X Strength
0	1	1	N/A	PCI Strength
1	X	X	N/A	Bypass, User Configurable
BYPASS	**TYPEDET#**	**PCI**	**AGP Mode**	**Input Type**
X	0	X	4X	Differential
X	0	X	1X/2X	Single-Ended
X	1	X	1X/2X	Single-Ended
X	1	X	1X/2X	Single-Ended

AGP Compensation Bypass — Dev0:F0:0xB8

Bit	31	30	29	28	27	26	25	24
	BYP_PDrvXfer				BYP_NDrvXfer			
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	23	22	21	20	19	18	17	16
	BYPXfer	Reserved			PSlewXfer		NSlewXfer	
Reset	1	0	0	0	0	0	0	0
R/W	R/W	R			R/W			

Bit	15	14	13	12	11	10	9	8
	BYP_PDrvStrb				BYP_NDrvStrb			
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	7	6	5	4	3	2	1	0
	BYPStrb	Reserved			PSlewStrb		NSlewStrb	
Reset	1	0	0	0	0	0	0	0
R/W	R/W	R			R/W			

Register Description

This register allows BIOS to bypass the AGP auto-compensation to directly control the AGP pad configuration.

Bit Definitions **AGP Compensation Bypass (Dev0:F0:0xB8)**

Bit	Name	Function
31–28	BYP_PDrvXfer	**P Drive Strength Control** This field is used to directly program the P transistor drive strength on all AGP pins except the data strobes. A value of 0000 is the weakest, 1111 is the strongest. This value is written to the I/O pads only when BYPXfer (bit 23) is set.
27–24	BYP_NDrvXfer	**N Drive Strength Control** This field is used to directly program the N transistor drive strength on all AGP signals except the data strobes. A value of 0000 is the weakest, 1111 is the strongest. This value is written to the I/O pads only when BYPXfer (bit 23) is set.
23	BYPXfer	**Bypass Enable** This bit must be set to bypass the auto-compensation circuit for direct control of all AGP pads except the strobe pins. When this bit is set, the values programmed in the drive strength fields are written directly to the pads.
22–20	Reserved	**Reserved**
19–18	PSlewXfer	**Slew Rate Control** This field is used to directly program the rise time in all AGP signals except the data strobes. This field is not affected by the BYPXfer bit. 00 = Slew rate 0 (slowest) 01 = Slew rate 1 10 = Slew rate 2 11 = Slew rate 3 (fastest)
17–16	NSlewXfer	**Slew Rate Control** This field is used to directly program the fall time in all AGP signals except the data strobes. This field is not affected by the BYPXfer bit. 00 = Slew rate 0 (slowest) 01 = Slew rate 1 10 = Slew rate 2 11 = Slew rate 3 (fastest)
15–12	BYP_PDrvStrb	**P Drive Strength Control** This field is used to directly program the P transistor drive strength on the AGP data strobes (AD_STB[1:0], AD_STB[1:0]#). A value of 0000 is the weakest, 1111 is the strongest. This value is written to the I/O pads only when BYPStrb (bit 7) is set.
11–8	BYP_NDrvStrb	**N Drive Strength Control** This field is used to directly program the N transistor drive strength on all AGP data strobes (AD_STB[1:0], AD_STB[1:0]#). A value of 0000 is the weakest, 1111 is the strongest. This value is written to the I/O pads only when BYPStrb (bit 7) is set.
7	BYPStrb	**Bypass Enable** This bit must be set to bypass the auto-compensation circuit for direct control of all AGP strobe pins (AD_STB[1:0], AD_STB[1:0]#). When this bit is set, the values programmed in the drive strength fields are written directly to the pads.
6–4	Reserved	**Reserved**

Bit Definitions (Continued) **AGP Compensation Bypass (Dev0:F0:0xB8)**

Bit	Name	Function
3–2	PSlewStrb	**Slew Rate Control** This field is used to directly program the rise time in all AGP data strobes (AD_STB[1:0], AD_STB[1:0]#). This field is not affected by the BYPStrb bit. 00 = Slew rate 0 (slowest) 01 = Slew rate 1 10 = Slew rate 2 11 = Slew rate 3 (fastest)
1–0	NSlewStrb	**Slew Rate Control** This field is used to directly program the fall time in all AGP data strobes (AD_STB[1:0], AD_STB[1:0]#). This field is not affected by the BYPStrb bit. 00 = Slew rate 0 (slowest) 01 = Slew rate 1 10 = Slew rate 2 11 = Slew rate 3 (fastest)

Programming Notes

There are three basic modes of bypass operation, as shown in the table below. Note that compensation applies to 1.5-V signalling operation only.

Auto Compensate	Bypass	Bypass Modes
Non-strobe	Strobes	Non-strobed signals auto-compensated while strobe signals programmed manually in bypass mode.
	All signals	All signals programmed manually in bypass mode.
All signals		All signals auto-compensated.

It is possible to configure the AGP I/O pads such that the non-strobed signals are auto-compensated while the strobes are in bypass mode, but not vice-versa, as shown in the table above.

Once the non-strobed signals are programmed in bypass mode, these programmed bypassed values are also written to the strobed signal I/O pads, until the strobed pads bypass values are also written.

Memory Base Address Registers (Dev0:F0:0xC0 to 0xDF)

The AMD-761 system controller DDR memory controller can access up to eight banks of DRAM (four DIMMs, one bank per side). These banks are controlled by eight chip selects. These registers define how an incoming address is parsed to select only one out of the eight chip selects. BIOS software is responsible for correctly loading these registers based on data returned from the serial presence detect ROM mechanism through the SMBus implemented in the Southbridge. BIOS software must adhere to the following rules when configuring these registers:

- The largest banks are configured first as the lowest addressed memory, increasing addresses with decreasing size of banks available.
- Logically, a given chip-select N, is asserted when:

  (Addr[31:23] & ~CSMaskN) == (CSBaseN & ~CSMaskN)
- The smallest bank supported is 32 Mbytes.

See Table 10 on page 95.

Table 10. DDR Memory Base Address Register Locations

Memory Base Address Register 0	**Dev0:F0:0xC0**
Memory Base Address Register 1	**Dev0:F0:0xC4**
Memory Base Address Register 2	**Dev0:F0:0xC8**
Memory Base Address Register 3	**Dev0:F0:0xCC**
Memory Base Address Register 4	**Dev0:F0:0xD0**
Memory Base Address Register 5	**Dev0:F0:0xD4**
Memory Base Address Register 6	**Dev0:F0:0xD8**
Memory Base Address Register 7	**Dev0:F0:0xDC**

	31	30	29	28	27	26	25	24
Bit	CS_Base							
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	CS_Base	Reserved						
Reset	X	0	0	0	0	0	0	0
R/W	R/W	R						

	15	14	13	12	11	10	9	8
Bit	CS_Mask							
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	CS_Mask	Reserved				Addr_Mode		CS_En
Reset	X	0	0	0	0	X	X	X
R/W	R/W	R				R/W		

Register Description

Note that these registers are not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **Memory Base Address Registers 0–7 (Dev0:F0:0xC0–0xDF)**

Bit	Name	Function
31–23	CS_Base	**Chip-Select Base** This bit field defines which 8-Mbyte boundary the given bank services. Incoming addresses are compared against field, subject to the mask field in bits [15:7].
22–16	Reserved	**Reserved**
15–7	CS_Mask	**Chip-Select Mask** This bit field defines what bits in the address are ignored when incoming addresses are compared to the CSBase in bits[31:23] above. If a given bit is set, the corresponding bit in the compare is ignored.
6–3	Reserved	**Reserved**
2–1	Addr_Mode	**Addressing Mode** This bit field determines the addressing mode for this CS, based on the type of DIMM installed, according to Table 11. This addressing applies to the physical addressing on the MAA and MAB address buses. *Note that modes 00 and 11 are reserved*.
0	CS_En	**Chip-Select Enable** When set, this bank is eligible for selection by incoming addresses. When clear, this bank's chip select is not asserted and the values in [31:23] and [15:7] are ignored.

Programming Notes

Note that these registers are not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access. Table 11 shows DRAM addressing modes.

Table 11. AMD-761™ DRAM Addressing Modes

Mode	Pins	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode 1 Addr_Mode = 01 64 Mbyte x4/8/16 128 Mbyte x4/8/16	**Row**	12	11		24	23	22	21	20	19	18	17	16	15	14	13
	Col	12	11		27	PC	26	25	10	9	8	7	6	5	4	3
		BK	BK													
Mode 2 Addr_Mode = 10 256 Mbyte x4/8/16 512 Mbyte x4/8/16	**Row**	12	11	25	24	23	22	21	20	19	18	17	16	15	14	13
	Col	12	11	29	28	PC	27	26	10	9	8	7	6	5	4	3
		BK	BK													

2.4.4 Device 0, Function 1: DDR PDL Configuration Registers

The registers defined in this section are required to implement Double Data Rate (DDR) DRAM in the AMD-761 system controller Northbridge. The function 1 registers control the 18 DDR programmable delay lines (PDL). In Table 12, the column entitled Offset consists of the register number specified in the Configuration Address register bits [7:2] concatenated with 0b00 to form a simple 1-byte offset.

Table 12. Device 0, Function 1 Configuration Register Map

DDR PDL Registers (Device 0, Function 1)	Offset	Reference
Reserved	0x00 to 0x3F	
DDR PDL Calibration Control	0x40 to 0x43	"Dev0:F1:0x40" on page 98
DDR PDL Configuration 0	0x44 to 0x47	"Dev0:F1:0x44" on page 101
DDR PDL Configuration 1	0x48 to 0x4B	
DDR PDL Configuration 2	0x4C to 0x4F	
DDR PDL Configuration 3	0x50 to 0x53	
DDR PDL Configuration 4	0x54 to 0x57	
DDR PDL Configuration 5	0x58 to 0x5B	
DDR PDL Configuration 6	0x5C to 0x5F	
DDR PDL Configuration 7	0x60 to 0x63	
DDR PDL Configuration 8	0x64 to 0x67	
DDR PDL Configuration 9	0x68 to 0x6B	
DDR PDL Configuration 10	0x6C to 0x6F	
DDR PDL Configuration 11	0x70 to 0x73	
DDR PDL Configuration 12	0x74 to 0x77	
DDR PDL Configuration 13	0x78 to 0x7B	
DDR PDL Configuration 14	0x7C to 0x7F	
DDR PDL Configuration 15	0x80 to 0x83	
DDR PDL Configuration 16	0x84 to 0x87	
DDR PDL Configuration 17	0x88 to 0x8B	
DDR MDAT/DQS Pad Configuration	0x8C to 0x8F	"Dev0:F1:0x8C" on page 104
DDR CLK/CS Pad Configuration	0x90 to 0x93	"Dev0:F1:0x90" on page 108
DDR CMDB/CMDA Pad Configuration	0x94 to 0x97	"Dev0:F1:0x94" on page 111
DDR MAB/MAA Pad Configuration	0x98 to 0x9B	"Dev0:F1:0x98" on page 114
Reserved	0x9C to 0xFF	

DDR PDL Calibration Control — Dev0:F1:0x40

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	SW_Recal	Use_Act_Dly	Auto_Cal_En	Act_Dly_Inh	Reserved		Auto_Cal_Period	
Reset	X	X	X	X	0	0	X	X
R/W	R/W	W	R/W	R/W	R		R/W	

Register Description

This register allows BIOS control of the calibration circuit for the AMD-761™ system controller's 18 programmable delay lines.

Note that this register is not initialized at reset time but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

Bit Definitions **DDR PDL Calibration Control (Dev0:F1:0x40)**

Bit	Name	Function
31–8	Reserved	**Reserved**
7	SW_Recal	**Software Recalibration** Software should write a 1 to this bit to cause recalibration of the PDLs. The hardware recomputes the Cal_Delay values for all PDLs, based on the values of their SW_Cal_Dly fields. Status of the recalibration that was initiated by writing a 1 to this bit is also indicated in this bit. After setting this bit, software should poll this bit until it becomes a 0 again. 0 = Calibration complete (default) 1 = Calibration not complete If Auto_Cal_En is set, writes to this bit are ignored. Also refer to Table 13, "PDL Calibration Modes," on page 100. ***Note:*** *This bit should not be set if the system clock frequency is 66 MHz.*
6	Use_Act_Dly	**Use Actual Delay** Software should set this bit to indicate to the hardware that it has written to the Act_Dly fields and wants to update the PDLs (all 18) with the newly written Act_Delay values. Software only needs to change the Act_Delay values that are not currently at their desired values (the other Act_Dly values are simply re-applied). This method should be used only when SW_Recal and Auto_Cal_En bits are not set. If Auto_Cal_En is set, writes to this bit are ignored. Also refer to Table 13, "PDL Calibration Modes," on page 100. This bit always returns a 0 when read.
5	Auto_Cal_En	**Auto Calibration Mode** 0 = Auto-calibration mode off (default) 1 = Auto-calibration mode on When this bit is set, all of the Cal_Dly values are recomputed periodically (according to the setting of the Auto_Cal_Period field) for all PDLs, based on the values of their SW_Cal_Dly fields. If the Act_Dly_Inh bit is not set, the Cal_Dly values are also applied to the Act_Dly. Also refer to Table 13, "PDL Calibration Modes," on page 100. ***Note:*** *Once Auto_Cal_En is set to 1, clearing it makes the bit a 0, but the Auto-Calibration logic may perform one more update, depending on when the Auto_Cal_En bit is cleared. Therefore, BIOS should at least wait for the amount of time specified by the Auto_Cal_Period field after clearing the Auto_Cal_En bit before attempting to change any of the PDL parameters.* ***Note:*** *This bit should not be set if the system clock frequency is 66 MHz.*

Bit Definitions (Continued) **DDR PDL Calibration Control (Dev0:F1:0x40)**

Bit	Name	Function
4	Act_Dly_Inh	**Actual Delay Update Inhibit** This bit configures the hardware to either update the actual PDLs (Act_Dly values) with new Cal_Delay values or not. The setting of this bit affects both auto-calibration and SWCalibration but not the Use_Act_Dly method. After an exit from power-on reset or self-refresh, the setting of this bit determines whether the Act_Dly value is updated or not. 0 = Update all the PDLs with new Cal_Dly values in hardware after recomputation is done (default). 1 = Do not update the Actual PDL delay values after recomputation of Cal_Dly is done. ***Note:*** *The internal logic tests this bit just prior to updating the Act_Dly, so the other bits in this register should be taken into consideration when writing to this bit.*
3–2	Reserved	**Reserved**
1–0	Auto_Cal_Period	**Auto-Calibration Period** This bit field defines how often auto-calibration is performed. 00 = 10000 system clocks 01 = 1000000 system clocks 10 = 10000000 system clocks 11 = Reserved BIOS should configure this field before setting the Auto_Cal_En bit, and while Auto_Cal_En is set, do not write to this field.

Programming Notes

Note that this register is not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access.

See Table 13 for PDL calibration modes.

Table 13. PDL Calibration Modes

Auto_Cal_En	Use_Act_Delay	SW_ReCal	Resultant Operation
0	0	0	No action.
0	0	1	SW_Cal_Dly values are applied.
0	1	0	Act_Dly values are applied.
0	1	1	Illegal combination (do not use).
1	X	X	SW_Cal_Dly values are applied according to the Auto_Cal_Period setting. Do not set the Act_Dly or SW_Recal bits.

Table 14. DDR PDL Configuration Register Locations

DDR PDL Configuration Register 0	Dev0:F1:0x44
DDR PDL Configuration Register 1	Dev0:F1:0x48
DDR PDL Configuration Register 2	Dev0:F1:0x4C
DDR PDL Configuration Register 3	Dev0:F1:0x50
DDR PDL Configuration Register 4	Dev0:F1:0x54
DDR PDL Configuration Register 5	Dev0:F1:0x58
DDR PDL Configuration Register 6	Dev0:F1:0x5C
DDR PDL Configuration Register 7	Dev0:F1:0x60
DDR PDL Configuration Register 8	Dev0:F1:0x64
DDR PDL Configuration Register 9	Dev0:F1:0x68
DDR PDL Configuration Register 10	Dev0:F1:0x6C
DDR PDL Configuration Register 11	Dev0:F1:0x70
DDR PDL Configuration Register 12	Dev0:F1:0x74
DDR PDL Configuration Register 13	Dev0:F1:0x78
DDR PDL Configuration Register 14	Dev0:F1:0x7C
DDR PDL Configuration Register 15	Dev0:F1:0x80
DDR PDL Configuration Register 16	Dev0:F1:0x84
DDR PDL Configuration Register 17	Dev0:F1:0x88

DDR PDL Configuration Registers

	31	30	29	28	27	26	25	24
Bit	Clk_Dly							
Reset	X	X	X	X	X	X	X	X
R/W	R							

	23	22	21	20	19	18	17	16
Bit	SW_Cal_Dly							
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Cal_Dly							
Reset	X	X	X	X	X	X	X	X
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Act_Dly							
Reset	X	X	X	X	X	X	X	X
R/W	R/W							

Register Description

These registers allow configuration of programmable delay lines 0–17. There are a total of 18 PDLs (one per DDR DQS pin in x4 mode). Note that these registers are not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access, and a software initiated calibration should be forced.

Bit Definitions **DDR PDL Configuration Registers 0–17 (Dev0:F1:0x44–0x8B)**

Bit	Name	Function
31–24	Clk_Dly	**Clock Delay** This field provides the number of buffers that amount to one half-period of the system clock. ***Note:*** *Upon exit from self-refresh, this bit field is updated with the number of buffers required to equal one half-period of the system clock. The value of this field depends on the operating PVT point. This field is also updated when a recalibration is done either due to Auto_Cal_En or SW_Recal.*
23–16	SW_Cal_Dly	**Software Calibration Delay** This bit field represents the amount of delay that is required for the corresponding DQS. The typical value is 0x69 for 100-MHz DDR operation, or 0x6B for 133 MHz. This field is used to calculate the Cal_Dly value during exit from self-refresh, auto-calibration, and software-initiated recalibration. This field must be configured before setting the SW_Recal bit or the Auto_Cal_En bit, and while these bits are set, this field must not be written. BIOS writes a desired value into this field if the default DQS delays are not the desired DQS delays for any reason. The value written in this field should be 256 times the required delay as a percentage of the half-period of the system clock, and then rounded off to the nearest integer. For example, if the desired DQS delay is 43.5 percent of the system clock's half-period, the value written into this field should be 0.434 x 256 = 111 (0x6F). ***Note:*** *This bit field should not be used if the system clock frequency is 66 MHz.*
15–8	Cal_Dly	**Calibration Delay** This bit field provides the last Cal_Dly value in number of buffers. ***Note:*** *Upon exit from self-refresh, this bit field is updated with the number of buffers required to equal the time specified by the SW_Cal_Dly field. The value of this field depends on the operating PVT point. This field is also updated when a recalibration is done either due to Auto_Cal_En or SW_Recal.*
7–0	Act_Dly	**Actual Delay** This bit field provides the current Act_Dly value (in number of buffers) that is in effect for the corresponding PDL. Software can read the current value of Act_Dly from this field. Software can write the desired number of buffer delays into this field. Software typically writes to this field only if auto-calibration is disabled. After writing to this field, software should also set the Use_Act_Dly bit in the PDL Calibration Control register. Upon writes to this field, the new value takes effect at the first available "safe" time after the Use_Act_Dly bit is set. ***Note:*** *Upon exit from self-refresh, this bit field is updated with the number of buffers required to equal the time specified by the SW_Cal_Dly field. The value of this field depends on the operating PVT point. This field is also updated when a recalibration is done either due to Auto_Cal_En or SW_Recal (unless the Act_Dly_Inh bit in the PDL Calibration register is set).* ***Note:*** *Values written directly by software to this field are not PVT-independent, so this field is primarily for lab and debug use.*

Programming Notes

Note that these registers are not initialized at reset time, but must be initialized by BIOS for proper operation. This action should be done prior to attempting DRAM access, and a software-initiated calibration should be forced.

DDR DQS/MDAT Pad Configuration — Dev0:F1:0x8C

	31	30	29	28	27	26	25	24
Bit	Reserved		PSlewMDAT			NSlewMDAT		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	23	22	21	20	19	18	17	16
Bit	Reserved				PDrvMDAT		NDrvMDAT	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

	15	14	13	12	11	10	9	8
Bit	Reserved		PSlewDQS			NSlewDQS		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	7	6	5	4	3	2	1	0
Bit	Reserved				PDrvDQS		NDrvDQS	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

Register Description

This register allows BIOS control of the DDR DQS and memory data pad drive strength and slew rate.

Bit Definitions **DDR DQS/MDAT Pad Configuration (Dev0:F1:0x8C)**

Bit	Name	Function
31–30	Reserved	**Reserved**
29–27	PSlewMDAT	**MDAT Rising Edge Slew Rate** These bits control the rising edge slew rate of the MDAT[63:0] and DM[8:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest) Note that the DM[8:0] pins are controlled by the PSlewDQS field when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register (Dev 0:F0:0x58).
26–24	NSlewMDAT	**MDAT Falling Edge Slew Rate** These bits control the falling edge slew rate of the MDAT[63:0] and DM[8:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest) Note that the DM[8:0] pins are controlled by the NSlewDQS field when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register (Dev 0:F0:0x58).
23–20	Reserved	**Reserved**
19–18	PDrvMDAT	**MDAT P Transistor Drive Strength** These bits control the P transistor drive strength of the MDAT[63:0] and DM[8:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest) Note that the DM[8:0] pins are controlled by the PDrvDQS field when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register (Dev 0:F0:0x58).

Bit Definitions (Continued) **DDR DQS/MDAT Pad Configuration (Dev0:F1:0x8C)**

Bit	Name	Function
17–16	NDrvMDAT	**MDAT N Transistor Drive Strength** These bits control the N transistor drive strength of the MDAT[63:0] and DM[8:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest) Note that the DM[8:0] pins are controlled by the NDrvDQS field when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register (Dev 0:F0:0x58).
15–14	Reserved	**Reserved**
13–11	PSlewDQS	**DQS Rising Edge Slew Rate** These bits control the rising edge slew rate of the DQS[8:0] pins (and DM[8:0] pins) when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register at Dev 0:F0:0x58). 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
10–8	NSlewDQS	**DQS Falling Edge Slew Rate** These bits control the falling edge slew rate of the DQS[8:0] pins (and DM[8:0] pins) when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register at Dev 0:F0:0x58). 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
7–4	Reserved	**Reserved**

Bit Definitions (Continued) **DDR DQS/MDAT Pad Configuration (Dev0:F1:0x8C)**

Bit	Name	Function
3–2	PDrvDQS	**DQS P Transistor Drive Strength** These bits control the P transistor drive strength of the DQS[8:0] pins (and DM[8:0] pins) when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register at Dev 0:F0:0x58). 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
1–0	NDrvDQS	**DQS N Transistor Drive Strength** These bits control the N transistor drive strength of the DQS[8:0] pins (and DM[8:0] pins) when any chip select is configured for x4 DIMMs in the DRAM Mode/Status register at Dev 0:F0:0x58). 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)

Programming Notes

DDR CLK/CS Pad Configuration — Dev0:F1:0x90

	31	30	29	28	27	26	25	24
Bit	Reserved		PSlewCLK			NSlewCLK		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	23	22	21	20	19	18	17	16
Bit	Reserved				PDrvCLK		NDrvCLK	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

	15	14	13	12	11	10	9	8
Bit	Reserved		PSlewCS			NSlewCS		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	7	6	5	4	3	2	1	0
Bit	Reserved				PDrvCS		NDrvCS	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

Register Description

This register allows BIOS control of the DDR clocks and chip-selects pad drive strength and slew rate.

Bit Definitions **DDR CLK/CS Pad Configuration (Dev0:F1:0x90)**

Bit	Name	Function
31–30	Reserved	**Reserved**
29–27	PSlewCLK	**Clocks Rising Edge Slew Rate** These bits control the rising edge slew rate of the CLKOUT[5:0] and CLKOUT[5:0]# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
26–24	NSlewCLK	**Clocks Falling Edge Slew Rate** These bits control the falling edge slew rate of the CLKOUT[5:0] and CLKOUT[5:0]# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
23–20	Reserved	**Reserved**
19–18	PDrvCLK	**Clocks P Transistor Drive Strength** These bits control the P transistor drive strength of the CLKOUT[5:0] and CLKOUT[5:0]# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
17–16	NDrvCLK	**Clocks N Transistor Drive Strength** These bits control the N transistor drive strength of the CLKOUT[5:0] and CLKOUT[5:0]# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
15–14	Reserved	**Reserved**

Bit Definitions (Continued) **DDR CLK/CS Pad Configuration (Dev0:F1:0x90)**

Bit	Name	Function
13–11	PSlewCS	**CS Rising Edge Slew Rate** These bits control the rising edge slew rate of the CS[7:0]# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
10–8	NSlewCS	**CS Falling Edge Slew Rate** These bits control the falling edge slew rate of the CS[7:0]# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
7–4	Reserved	**Reserved**
3–2	PDrvCS	**CS P Transistor Drive Strength** These bits control the P transistor drive strength of the CS[7:0]# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
1–0	NDrvCS	**CS N Transistor Drive Strength** These bits control the N transistor drive strength of the CS[7:0]# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)

Programming Notes

DDR CMDB/CMDA Pad Configuration — Dev0:F1:0x94

	31	30	29	28	27	26	25	24
Bit	Reserved		PSlewCMDB			NSlewCMDB		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	23	22	21	20	19	18	17	16
Bit	Reserved				PDrvCMDB		NDrvCMDB	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

	15	14	13	12	11	10	9	8
Bit	Reserved		PSlewCMDA			NSlewCMDA		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	7	6	5	4	3	2	1	0
Bit	Reserved				PDrvCMDA		NDrvCMDA	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

Register Description

This register allows BIOS control of the DDR RASA#, RASB#, CASA#, CASB#, WEA#, WEB#, CKEA#, and CKEB# pad drive strength and slew rate.

Bit Definitions **DDR CMDB/CMDA Pad Configuration (Dev0:F1:0x94)**

Bit	Name	Function
31–30	Reserved	**Reserved**
29–27	PSlewCMDB	**Command B Rising Edge Slew Rate** These bits control the rising edge slew rate of the RASB#, CASB#, WEB#, and CKEB# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
26–24	NSlewCMDB	**Command B Falling Edge Slew Rate** These bits control the falling edge slew rate of the RASB#, CASB#, WEB#, and CKEB# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
23–20	Reserved	**Reserved**
19–18	PDrvCMDB	**Command B P Transistor Drive Strength** These bits control the P transistor drive strength of the RASB#, CASB#, WEB#, and CKEB# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
17–16	NDrvCMDB	**Command B N Transistor Drive Strength** These bits control the N transistor drive strength of the RASB#, CASB#, WEB#, and CKEB# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
15–14	Reserved	**Reserved**

Bit Definitions (Continued) **DDR CMDB/CMDA Pad Configuration (Dev0:F1:0x94)**

Bit	Name	Function
13–11	PSlewCMDA	**Command A Rising Edge Slew Rate** These bits control the rising edge slew rate of the RASA#, CASA#, WEA#, and CKEA# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
10–8	NSlewCMDA	**Command A Falling Edge Slew Rate** These bits control the falling edge slew rate of the RASA#, CASA#, WEA#, and CKEA# pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
7–4	Reserved	**Reserved**
3–2	PDrvCMDA	**Command A P Transistor Drive Strength** These bits control the P transistor drive strength of the RASA#, CASA#, WEA#, and CKEA# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
1–0	NDrvCMDA	**Command A N Transistor Drive Strength** These bits control the N transistor drive strength of the RASA#, CASA#, WEA#, and CKEA# pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)

Programming Notes

DDR MAB/MAA Pad Configuration — Dev0:F1:0x98

	31	30	29	28	27	26	25	24
Bit	Reserved		PSlewMAB			NSlewMAB		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	23	22	21	20	19	18	17	16
Bit	Reserved				PDrvMAB		NDrvMAB	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

	15	14	13	12	11	10	9	8
Bit	Reserved		PSlewMAA			NSlewMAA		
Reset	0	0	X	X	X	X	X	X
R/W	R		R/W					

	7	6	5	4	3	2	1	0
Bit	Reserved				PDrvMAA		NDrvMAA	
Reset	0	0	0	0	X	X	X	X
R/W	R				R/W			

Register Description

This register allows BIOS control of the DDR MAA and MAB address bus pad drive strength and slew rate.

Bit Definitions **DDR MAB/MAA Pad Configuration (Dev0:F1:0x98)**

Bit	Name	Function
31–30	Reserved	**Reserved**
29–27	PSlewMAB	**MAB Rising Edge Slew Rate** These bits control the rising edge slew rate of the MAB[14:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
26–24	NSlewMAB	**MAB Falling Edge Slew Rate** These bits control the falling edge slew rate of the MAB[14:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
23–20	Reserved	**Reserved**
19–18	PDrvMAB	**MAB P Transistor Drive Strength** These bits control the P transistor drive strength of the MAB[14:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
17–16	NDrvMAB	**MAB N Transistor Drive Strength** These bits control the N transistor drive strength of the MAB[14:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
15–14	Reserved	**Reserved**

Bit Definitions (Continued) **DDR MAB/MAA Pad Configuration (Dev0:F1:0x98)**

Bit	Name	Function
13–11	PSlewMAA	**MAA Rising Edge Slew Rate** These bits control the rising edge slew rate of the MAA[14:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
10–8	NSlewMAA	**MAA Falling Edge Slew Rate** These bits control the falling edge slew rate of the MAA[14:0] pins. 000 = Slew rate 0 (slowest) 001 = Slew rate 1 010 = Slew rate 2 011 = Slew rate 3 100 = Slew rate 4 101 = Slew rate 5 110 = Slew rate 6 111 = Slew rate 7 (fastest)
7–4	Reserved	**Reserved**
3–2	PDrvMAA	**MAA P Transistor Drive Strength** These bits control the P transistor drive strength of the MAA[14:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)
1–0	NDrvMAA	**MAA N Transistor Drive Strength** These bits control the N transistor drive strength of the MAA[14:0] pins. 00 = Drive strength 0 (weakest) 01 = Drive strength 1 10 = Drive strength 2 11 = Drive strength 3 (strongest)

Programming Notes

2.4.5 Device 1: PCI-to-PCI Bridge Configuration Registers

The registers defined in this section are required to implement the PCI-to-PCI bridge function (device 1) in the AMD-761 system controller Northbridge. In Table 15, the column entitled Offset consists of the register number specified in the Configuration Address register bits [7:2] concatenated with 0b00 to form a simple 1-byte offset.

Table 15. Device 1 Configuration Register Map

PCI-to-PCI Bridge (Device 1)				Offset	Reference
Device ID		Vendor ID		0x00	"Dev1:0x00" on page 118
Status		Command		0x04	"Dev1:0x04" on page 120
Class Code0x0600			Revision ID	0x08	"Dev1:0x08" on page 123
Reserved	Header Type	Primary Latency Timer	Reserved	0x0C	"Dev1:0x0C" on page 124
Reserved				0x10 to 0x17	
SecLatency Time	Subordinate Bus Num	Secondary Bus Num	Primary Bus Num	0x18	"Dev1:0x18" on page 125
Secondary Status		I/O Limit	I/O Base	0x1C	"Dev1:0x1C" on page 127
Memory Limit		Memory Base		0x20	"Dev1:0x20" on page 130
Prefetchable Memory Limit		Prefetchable Memory Base		0x24	"Dev1:0x24" on page 132
Reserved				0x28 to 0x2F	
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		0x30	"Dev1:0x30" on page 134
Reserved			Reserved	0x34 to 0x3B	
Bridge Control		Interrupt Pin	Interrupt Line	0x3C	"Dev1:0x3C" on page 135
Miscellaneous Device 1 Control				0x40	"Dev1:0x40" on page 137
Reserved				0x44 to 0xFF	

AGP/PCI ID — Dev1:0x00

	31	30	29	28	27	26	25	24
Bit	Dev_ID							
Reset	0	1	1	1	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Dev_ID							
Reset	0	0	0	0	1	1	1	1
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Vend_ID							
Reset	0	0	0	1	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Vend_ID							
Reset	0	0	1	0	0	0	1	0
R/W	R							

Register Description

Bit Definitions **AGP/PCI ID (Dev1:0x00)**

Bit	Name	Function
31–16	Dev_ID	**Device Identifier** This 16-bit register is assigned by the device manufacturer and identifies the type of device. The current Northbridge device ID assignments are: AMD-761™ system controller — AMD Athlon™ processor, 1P DDR 133 MHz 0x700E host to PCI bridge 0x700F PCI-to-PCI bridge (4X AGP) AMD-762™ system controller — AMD Athlon processor, 2P DDR 133 MHz 0x700C host to PCI bridge 0x700D PCI-to-PCI bridge (4X AGP) AMD-751™ system controller — AMD Athlon processor, 1P SDRAM-100 0x7006 host to PCI bridge 0x7007 PCI-to-PCI bridge (1X/2X AGP)
15–0	Vend_ID	**Vendor Identifier** This 16-bit register identifies the manufacturer of the device.

Programming Notes

AGP/PCI Command and Status — Dev1:0x04

	31	30	29	28	27	26	25	24
Bit	PERR_Rcv	SERR_Rcv	Mas_ABRT	Trgt_ABRT	Trgt_ABRTS _Signaled	DEVSEL_Timing		Data_PERR
Reset	0	0	0	0	0	0	1	0
R/W	R	R/W1C	R					

	23	22	21	20	19	18	17	16
Bit	Fast_B2B	UDF	66M	Cap_Lst	Reserved			
Reset	0	0	1	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved						FBACK	SERR
Reset	0	0	0	0	0	0	0	0
R/W	R							R/W

	7	6	5	4	3	2	1	0
Bit	STEP	PERR	VGA	MWINV	SCYC	MSTR	MEM	I/O
Reset	0	0	0	0	0	0	0	0
R/W	R					R/W		

Register Description

The AGP/PCI Command and Status register provides coarse control over the PCI-PCI bridge function within the AMD-761™ system controller. This register controls the ability to generate and respond to PCI cycles on both the AGP bus and the PCI bus.

Bit Definitions **AGP/PCI Command and Status (Dev1:0x04)**

Bit	Name	Function
31	PERR_Rcv	**Detected Parity Error** This bit is always Low because the AMD-761™ system controller does not support parity checking.
30	SERR_Rcv	**Signaled System Error** This bit is set whenever the AMD-761 system controller received AGP SERR# and subsequently asserted PCI SERR#. This bit is cleared by writing a 1. Refer to Table 7 on page 34 for details about SERR# assertion and status.
29	Mas_ABRT	**Received Master Abort** This bit is always 0.
28	Trgt_ABRT	**Receive Target Abort** This bit is always 0.
27	Trgt_ABRTS _Signaled	**Signaled Target Abort** This bit is always 0.
26–25	DEVSEL_Timing	**DEVSEL# Timing** This field is always 0b01, indicating that the AMD-761 system controller supports medium DEVSEL# timing.
24	Data_PERR	**Data PERR#** This bit is always 0 because the AMD-761 system controller does not report data parity errors.
23	Fast_B2B	**Fast Back-to-Back Capable** This bit is always 0, indicating that the AMD-761 system controller as a target is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
22	UDF	**User-Definable Features** This bit is always 0, indicating that UDF is not supported on the AMD-761 system controller.
21	66M	**66-MHz Capable** This bit is always 1, indicating that the AMD-761 system controller supports 66 MHz on device 1.
20	Cap_Lst	**Capabilities List** This bit is always 0, indicating that the configuration space of this device does not support a capabilities list.
19–10	Reserved	**Reserved**
9	FBACK	**Fast Back-to-Back to Different Devices Enable** This bit is always 0, because the AMD-761 system controller does not allow generation of fast back-to-back transactions to different agents.

Bit Definitions (Continued) **AGP/PCI Command and Status (Dev1:0x04)**

Bit	Name	Function
8	SERR	**System Error Enable** When set, this bit enables the SERR# output. When clear, this bit disables the SERR# output. The AGP A_SERR# is an input to the AMD-761™ system controller. The AMD-761 system controller receives AGP A_SERR#, ORs it with the normal PCI SERR#, and asserts it to the AMD-766™ peripheral bus controller for possible error interrupt generation. Refer to Table 7 on page 34 for details about SERR# assertion and status.
7	STEP	**Address Stepping** This bit is always 0 because the AMD-761 system controller does not perform address stepping.
6	PERR	**Parity Error Response** This bit is always 0 because the AMD-761 system controller does not report data parity errors.
5	VGA	**VGA Palette Snoop Enable** This bit is always 0, indicating that the AMD-761 system controller does not snoop the VGA palette address range.
4	MWINV	**Memory Write and Invalidate Enable** This bit is always 0 because the AMD-761 system controller does not generate memory write and invalidate commands.
3	SCYC	**Special Cycle** This bit is always 0 because the AMD-761 system controller ignores PCI special cycles.
2	MSTR	**Bus Master Enable** When this bit is set, the AMD-761 system controller accepts DMA accesses from the AGP interface.
1	MEM	**Memory Access Enable** When set, the AMD-761 system controller forwards AMD Athlon™ processor system bus accesses that reference AGP memory space onto the AGP bus (see "Dev1:0x20" on page 130).
0	I/O	**I/O Access Enable** When set, the AMD-761 system controller forwards CPU accesses that reference AGP I/O space onto the AGP bus (see "Dev1:0x1C" on page 127).

Programming Notes

AGP/PCI Revision ID and Class Code — Dev1:0x08

	31	30	29	28	27	26	25	24
Bit	Class_Code							
Reset	0	0	0	0	0	1	1	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Sub-Class_Code							
Reset	0	0	0	0	0	1	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Prog_I/F							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Rev_ID							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

Bit Definitions — AGP/PCI Revision ID and Class Code (Dev1:0x08)

Bit	Name	Function
31–24	Class_Code	**Class Code** This field is always 06h, indicating that it is a bridge device.
23–16	Sub-Class_Code	**Sub-Class Code** This field is always 04h for sub-class code and 00h for Prog. I/F, indicating it is a PCI/PCI bridge.
15–8	Prog_I/F	**Program Interface** This field is always 00h, indicating that it is a PCI-to-PCI bridge.
7–0	Rev_ID	**Revision ID** This field contains an 8-bit value identifying the revision number of the device.

Programming Notes

AGP/PCI Header Type — Dev1:0x0C

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Header_Type							
Reset	0	0	0	0	0	0	0	1
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Pri_Lat_Timer							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

Bit Definitions — AGP/PCI Header Type (Dev1:0x0C)

Bit	Name	Function
31–24	Reserved	**Reserved**
23–16	Header_Type	**Header Type** Bit 23 is always 0, indicating that the AMD-761™ system controller is a single function device. Bits 22:16 are 0x01, indicating that type 01 configuration space header format is supported (PCI-to-PCI bridge).
15–8	Pri_Lat_Timer	**Primary Latency Timer** This latency timer is not used in the AMD-761 system controller because the primary bus of the PCI-to-PCI bridge is internal. This register is read/write to maintain compliance with the PCI specifications.
7–0	Reserved	**Reserved**

Programming Notes

AGP/PCI Sub Bus Number/Secondary Latency Timer — Dev1:0x18

Bit	31	30	29	28	27	26	25	24
	Secon_Lat_Timer							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	23	22	21	20	19	18	17	16
	Sub-Bus_Num							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	15	14	13	12	11	10	9	8
	Secon_Bus_Num							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Bit	7	6	5	4	3	2	1	0
	Pri_Bus_Num							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Register Description

Bit Definitions **AGP/PCI Sub Bus Number/Secondary Latency Timer (Dev1:0x18)**

Bit	Name	Function
31–24	Secon_Lat_Timer	**Secondary Latency Timer** Adheres to the definition of the latency timer in the *PCI Local Bus Specification*, Revision 2.2, but only applies to the secondary interface of a PCI-to-PCI bridge.
23–16	Sub-Bus_Num	**Sub-Bus Number** This bit field records the number of the highest numbered PCI bus that is behind (or subordinate to) a bridge. The bridge uses this number in conjunction with the Secondary Bus Number register to determine when to respond to type 1 configuration transactions on the primary interface and to pass them on to the secondary interface.
15–8	Secon_Bus_Num	**Secondary Bus Number** This bit field records the number of the PCI bus that the secondary interface of the bridge is connected to. The bridge uses this number to determine when to respond to type 1 configuration transactions on the primary interface and to convert them to type 0 transactions on the secondary interface.
7–0	Pri_Bus_Num	**Primary Bus Number** This bit field records the number of the PCI bus that the primary interface of the bridge is connected to. The bridge uses this number to decode type 1 configuration transactions on the secondary interface that should be converted to special cycle transactions on the primary interface.

Programming Notes

The AGP bus is logically a sub-bus of the PCI bus. The PCI bus normally enumerates as bus 0 and the AGP bus enumerates as bus 1.

AGP/PCI Status, I/O Base and Limit — Dev1:0x1C

	31	30	29	28	27	26	25	24
Bit	PERR_Rcv	SERR_Rcv	Mas_ABRT	Trgt_ABRT	Trgt_ABRTS _Signaled	DEVSEL_Timing		Data_PERR
Reset	0	0	0	0	0	0	1	0
R/W	R	R/W1C			R			

	23	22	21	20	19	18	17	16
Bit	Fast_B2B	UDF	66M	Cap_Lst	Reserved			
Reset	0	0	1	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	IO_Lim[15:12]				IO_Lim_R			
Reset	0	0	0	0	0	0	0	1
R/W	R/W				R			

	7	6	5	4	3	2	1	0
Bit	IO_Base[15:12]				IO_Base_R			
Reset	0	0	0	0	0	0	0	1
R/W	R/W				R			

Register Description

The Secondary Status register reflects the conditions of the secondary PCI-to-PCI bridge interface (the AGP bus). The I/O Base register defines the bottom (inclusive) of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other. The I/O Limit register defines the top (inclusive) of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other.

Bit Definitions **AGP/PCI Status, I/O Base and Limit (Dev1:0x1C)**

Bit	Name	Function
31	PERR_Rcv	**Detected Parity Error** This bit is always Low because the AMD-761™ system controller does not support parity checking.
30	SERR_Rcv	**Signaled System Error** This bit is set whenever the AMD-761 system controller received AGP SERR#. This bit is cleared by writing a 1. Refer to Table 7 on page 34 for details about SERR# assertion and status.
29	Mas_ABRT	**Received Master Abort** This bit is set by the AMD-761 system controller whenever a bus master transaction (except for a special cycle) is terminated due to a master abort. This bit is cleared by writing a 1.
28	Trgt_ABRT	**Receive Target Abort** This bit is set by the AMD-761 system controller whenever a bus master transaction (except for a special cycle) is terminated due to a target abort. This bit is cleared by writing a 1.
27	Trgt_ABRTS _Signaled	**Signaled Target Abort** This bit is always 0 because the AMD-761 system controller does not terminate transactions with target aborts.
26–25	DEVSEL_Timing	**DEVSEL# Timing** This field is always 0x1, indicating that the AMD-761 system controller supports medium DEVSEL# timing.
24	Data_PERR	**Data PERR#** This bit is always 0 because the AMD-761 system controller does not report data parity errors.
23	Fast_B2B	**Fast Back-to-Back Capable** This bit is always 0, indicating that the AMD-761 system controller as a target is not capable of accepting fast back-to-back transactions when the transactions are not to the same agent.
22	UDF	**User-Definable Features** This bit is always 0, indicating that UDF is not supported on the AMD-761 system controller.
21	66M	**66-MHz Capable** This bit is always 1, indicating that the AMD-761 system controller supports 66 MHz on device 1.
20	Cap_Lst	**Capabilities List** This bit is always 0, indicating that the configuration space of this device does not support a capabilities list.
19–16	Reserved	**Reserved**
15–12	IO_Lim[15:12]	**I/O Limit (Write)** This bit field indicates the upper writable 4 bits that define the top address of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other.
11–8	IO_Lim_R	**I/O Limit (Read)** The lower read-only 4 bits define the top address of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other. 0x1 indicates that 32-bit I/O address decoding is available.

Bit Definitions (Continued) **AGP/PCI Status, I/O Base and Limit (Dev1:0x1C)**

Bit	Name	Function
7–4	IO_Base[15:12]	**I/O Base (Write)** The upper writable 4 bits define the bottom address of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other.
3–0	IO_Base_R	**I/O Base (Read)** The lower read-only 4 bits define the bottom address of an address range that is used by the bridge to determine when to forward I/O transactions from one interface to the other. 0x1 indicates that 32-bit I/O address decoding is available.

Programming Notes

AGP/PCI Memory Limit and Base — Dev1:0x20

	31	30	29	28	27	26	25	24
Bit	MLim[31:20]							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	MLim[31:20]				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

	15	14	13	12	11	10	9	8
Bit	MBase[31:20]							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	MBase[31:20]				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

Register Description

Bit Definitions **AGP/PCI Memory Limit and Base (Dev1:0x20)**

Bit	Name	Function
31–20	MLim[31:20]	**Memory Limit Address** Memory limit address defines the top address of the non-prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. The lower 20 bits of address are assumed to be 0xFFFFF. The memory address range adheres to 1-Mbyte alignment and granularity.
19–16	Reserved	**Reserved**
15–4	MBase[31:20]	**Memory Base Address** Memory Base Address defines the base address of the non-prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 0. The memory address range adheres to 1-Mbyte alignment and granularity.
3–0	Reserved	**Reserved**

Programming Notes

AGP/PCI Prefetchable Memory Limit and Base — Dev1:0x24

	31	30	29	28	27	26	25	24
Bit	Prefet_Mem_Lim							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	Prefet_Mem_Lim				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

	15	14	13	12	11	10	9	8
Bit	Prefet_Mem_Base							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	7	6	5	4	3	2	1	0
Bit	Prefet_Mem_Base				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

Register Description

Bit Definitions

Bit Definitions **AGP/PCI Prefetchable Memory Limit and Base (Dev1:0x24)**

Bit	Name	Function
31–20	Prefet_Mem_Lim	**Prefetchable Memory Limit Address** Prefetchable memory limit address defines the top address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. The lower 20 bits of address are assumed to be 0xFFFFF. The memory address range adheres to 1-Mbyte alignment and granularity.
19–16	Reserved	**Reserved**
15–4	Prefet_Mem_Base	**Prefetchable Memory Base Address** Prefetchable memory base address defines the base address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 0. The memory address range adheres to 1-Mbyte alignment and granularity.
3–0	Reserved	**Reserved**

Programming Notes

AGP/PCI I/O Limit and Base Upper 16 Bits — Dev1:0x30

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	I/O_Lim[23:16]							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	I/O_Base[23:16]							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Register Description

This set of registers define the valid range of 32-bit I/O addresses that are allowed to be forwarded from the host to the AGP/PCI. Note that if this register is 0, 32-bit addressing mode is effectively disabled.

Bit Definitions — **AGP/PCI I/O Limit and Base Upper 16 Bits (Dev1:0x30)**

Bit	Name	Function
31–24	Reserved	**Reserved**
23–16	I/O_Lim[23:16]	**I/O Limit** This field defines the upper limit (inclusive) of 24-bit I/O addresses that are passed to the AGP/PCI bus.
15–8	Reserved	**Reserved**
7–0	I/O_Base[23:16]	**I/O Base** This field defines the base (inclusive) of 24-bit I/O addresses that are passed to the AGP/PCI bus.

Programming Notes

AGP/PCI Interrupt and Bridge Control — Dev1:0x3C

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Bridge_Fast_B2B_En	Secon_Bus_Reset	Mas_Abort_Mode	Reserved	VGA_En	ISA_En	SERR_En	Par_Resp_En
Reset	0	0	0	0	0	0	0	0
R/W	R				R/W			R

	15	14	13	12	11	10	9	8
Bit	Int_Pin							
Reset	0	0	0	0	0	0	0	0
R/W	R/W (See Note)							

	7	6	5	4	3	2	1	0
Bit	Int_Line							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

Register Description

Bit Definitions **AGP/PCI Interrupt and Bridge Control (Dev1:0x3C)**

Bit	Name	Function
31–24	Reserved	**Reserved**
23	Bridge_Fast_B2B_En	**Fast Back-to-Back Capable** This bit is always 0, indicating that the AMD-761™ system controller as a master is not capable of generating fast back-to-back transactions to different agents on the secondary bus.
22	Secon_Bus_Reset	**Secondary Bus Reset** This bit is always 0. Reset for the secondary interface is done with the PCIRST# output of the AMD-766™ peripheral bus controller.
21	Mas_Abort_Mode	**Master Abort Mode** This bit is always 0. The response to a master abort is determined by the RD_Data_Err_Dis bit, Dev0:F0:0x84 bit 12.

Bit Definitions (Continued) **AGP/PCI Interrupt and Bridge Control (Dev1:0x3C)**

Bit	Name	Function
20	Reserved	**Reserved**
19	VGA_En	**VGA Enable** Affects the response by the bridge to compatible VGA addresses. When it is set, the bridge decodes and forwards the following accesses on the primary interface to the secondary interface. Memory accesses in the range: 0xA0000 to 0xBFFFF I/O address where AD[9:0] are in the ranges: 0x3B0 to 0x3BB and 0x3C0 to 0x3DF (inclusive of ISA address aliases — AD[15:10] are not decoded)
18	ISA_En	**ISA Enable** Modifies the response by the bridge to ISA I/O addresses. This modification applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 Kbytes of PCI I/O address space (0000 0000h to 0000 FFFFh). When set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-Kbyte block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-Kbyte block. 0 = Forward all I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1 = Block forwarding of ISA I/O addresses in the address range defined by the I/O Base & I/O Limit registers that are in the first 64 Kbytes of PCI I/O address space (top 768 bytes of each 1-Kbyte block).
17	SERR_En	**SERR Enable** Forwards the secondary interface SERR# assertions to the primary interface. This bit must be set, along with the SERR enable bit (Dev 1:F0:0x04) to allow an AGP SERR# to be propagated to the AMD-761™ system controller PCI SERR# pin. Refer to Table 7 on page 34 for details about SERR# assertion and status.
16	Par_Resp_En	**Parity Response Enable** This bit is always 0. The AMD-761 system controller does not support parity.
15–8	Int_Pin	**Interrupt Pin** Indicates which interrupt pin the PCI-to-PCI bridge uses. ***Note:*** *This field is R/W depending on the value of the IntPinCntl bit (Bit 0 of Dev 1:0x40). Refer to "Dev1:0x40" on page 137 for details. The ability to write this field is supported to allow BIOS to program to the required value.* The AMD-761 system controller hardware does not use this field internally in any way.
7–0	Int_Line	**Interrupt Line** Communicates interrupt line routing information. This field is a simple R/W field to allow BIOS software to program to the required value.

Programming Notes

Miscellaneous Device 1 Control — Dev1:0x40

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved							Int_Pin_Cntl
Reset	0	0	0	0	0	0	0	0
R/W	R							R/W

Register Description

Bit Definitions — Miscellaneous Device 1 Control (Dev1:0x40)

Bit	Name	Function
31–1	Reserved	**Reserved**
0	Int_Pin_Cntl	**Interrupt Pin Control** This bit controls the IntPin field in AGP/PCI Interrupt and Bridge Control register (Dev1:0x3C). 0 = IntPin field is read-only. 1 = IntPin field is read-writable for BIOS initialization.

Programming Notes

2.5 Memory-Mapped Registers

The AMD-761 system controller implements a set of memory-mapped control registers as shown in Section 2.5.2 on page 140. The base for these registers is defined in BAR1 (see "Dev0:F0:0x14" on page 39). This address is determined and loaded by system BIOS. The registers in the space are used by the AMD-761 miniport driver to control the GART cache functionality during run time.

2.5.1 AMD-761™ System Controller GART Cache Overview

This section provides a brief overview for programmers. The Graphics Address Relocation Table (GART) is a structure in memory that contains mappings from a virtual address generated by an AGP master (or any other master in the system including PCI masters and the CPU) and the actual physical address of a given request. The default mode used by the AMD-761 GART cache is a two-level directory/table indexing scheme that is very similar to the standard x86 virtual memory architecture. By using two levels of indexing, the GART structure does not need to be physically contiguous. Figure 4 on page 139 illustrates the two-level indexing scheme.

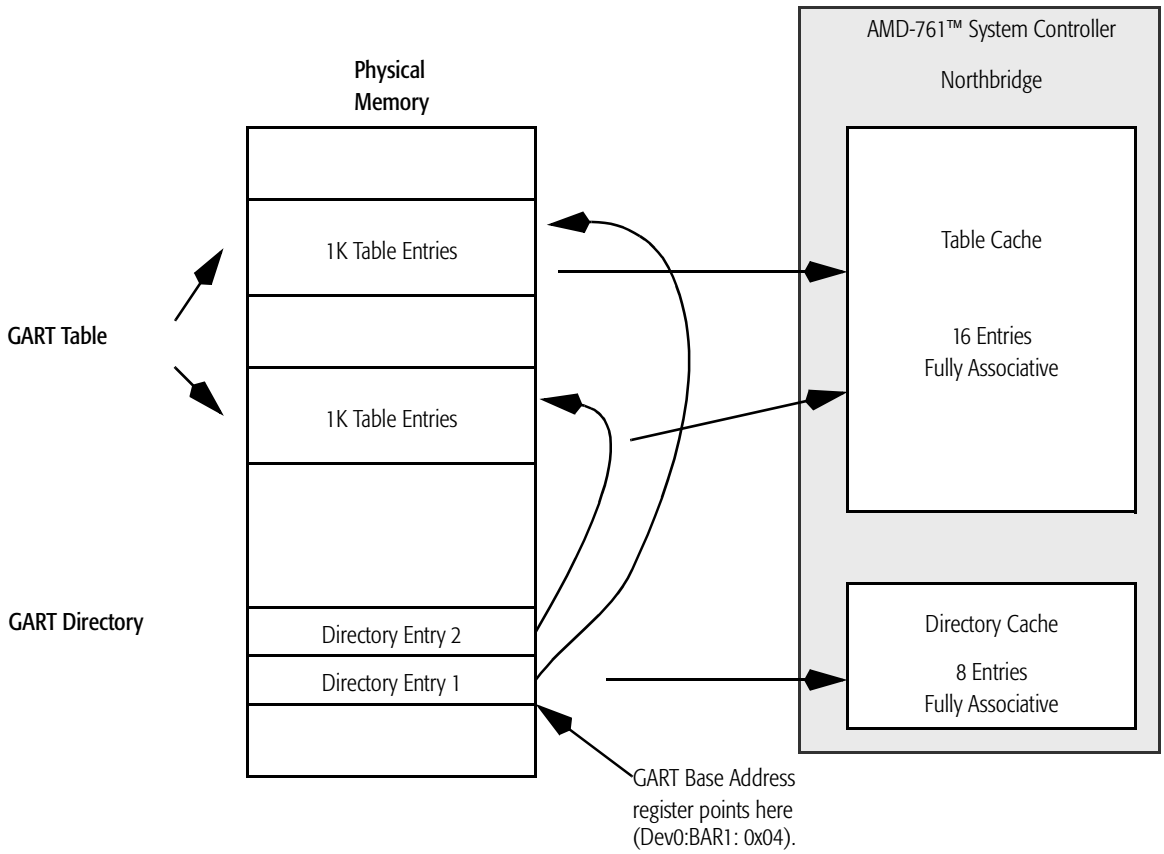

Figure 4. Two-Level GART Indexing

2.5.2 Memory-Mapped Register Map

For registers that are accessed by the AMD-761 system controller miniport driver during run time, the AMD-761 system controller implements a set of memory-mapped registers for quick access. These are defined in Table 16.

Table 16. AMD-761™ System Controller Memory-Mapped Registers

GART Memory-Mapped Control Registers				Offset from BAR1	Reference
Feature Status	Feature Control	Capabilities	Revision ID	0x00	"Bar1 + 0x00" on page 141
GART Base Address				0x04	"Bar1 + 0x04" on page 144
GART Cache Size				0x08	"Bar1 + 0x08" on page 145
GART Cache Control				0x0C	"Bar1 + 0x0C" on page 146
GART Cache Entry Control				0x10	"Bar1 + 0x10" on page 147

BAR1 Initialization

Note that BIOS must program the Base Address 1:GART Memory Mapped Register Base register (Dev 0:F0:0x14) prior to accessing the memory-mapped registers. Refer to "Dev0:F0:0x14" on page 39 for details of this register.

Features and Capabilities — Bar1 + 0x00

Bit	31	30	29	28	27	26	25	24
	Reserved		Valid_Bit_Err_ID		P2P_Status	GART_Cache_Status	Reserved	Valid_Err
Reset	0	0	0	0	0	0	0	0
R/W	R							R/W1C

Bit	23	22	21	20	19	18	17	16
	Reserved				P2P_En	TLB_En	SB_STB_Tog_Det	Gar_Valid_Err_En
Reset	0	0	0	0	0	0	0	0
R/W	R					R/W		

Bit	15	14	13	12	11	10	9	8
	Reserved				Hang_En	P2P_Cap	Link_Cap	Valid_Cap
Reset	0	0	0	0	0	0	0	1
R/W	R				R/W	R		

Bit	7	6	5	4	3	2	1	0
	Rev_ID							
Reset	0	0	0	0	0	0	0	1
R/W	R							

Register Description

Bit Definitions **Features and Capabilities (Bar1 + 0x00)**

Bit	Name	Function
31–30	Reserved	Reserved
29–28	Valid_Bit_Err_ID	**Valid Bit Error ID** These bits are used to determine the source of the valid bit error. The values are as follow: 00 = AGP 01 = CPU 10 = PCI/AGP's PCI 11 = Reserved
27	P2P_Status	**P2P Status** This bit is hardwired to 0 to indicate that the AMD-761™ system controller implements only those PCI-to-PCI bridge commands required to implement AGP (the AMD-761 system controller does not implement a complete PCI 2.1-compliant PCI-to-PCI bridge between PCI and AGP).
26	GART_Cache _Status	**GART Cache Status** 0 = GART cache disabled 1 = GART cache enabled by software
25	Reserved	**Reserved**
24	Valid_Err	**Valid Bit Error** When set, this bit indicates that a valid bit error has been detected and SERR# has been asserted. Refer to Table 7 on page 34 for details about SERR# assertion and status. This bit is cleared by writing a 1.
23–20	Reserved	**Reserved**
19	P2P_En	**P2P Enable** This bit is hardwired to 0 to indicate that the AMD-761 system controller only implements those PCI-to-PCI bridge commands required to implement AGP (the AMD-761 system controller does not implement a complete PCI 2.1-compliant PCI-to-PCI bridge between PCI and AGP).
18	TLB_En	**TLB Enable** When set, this bit enables the caching of GART TLB entries.
17	SB_STB_Tog _Det_Dis	**Sideband Strobe Toggle Detect Disable** When set, this bit disables the AGP sideband strobe toggle detect logic.
16	GAR_Valid_Err _En	**GART Valid Error Enable** When set, the AMD-761 system controller asserts SERR# when a graphics device attempts to access a page in AGP memory that is not valid (valid bit error). A valid bit error causes the GART table walk state machine to hang. The processor can still access memory after that if it does not use GART address space. Refer to Table 7 on page 34 for details about SERR# assertion and status.
15–12	Reserved	**Reserved**
11	Hang_En	**Hang Enable** When set, illegal GART entries fetched by the GTW logic forces the AMD-761 system controller to hang.

Bit Definitions (Continued) **Features and Capabilities (Bar1 + 0x00)**

Bit	Name	Function
10	P2P_Cap	**P2PCap** This bit is hardwired to 0 to indicate that the AMD-761™ system controller implements only those PCI-to-PCI bridge commands required to implement AGP (the AMD-761 system controller does not implement a complete PCI 2.1-compliant PCI-to-PCI bridge between PCI and AGP).
9	Link_Cap	**LinkCap** This bit is always Low, indicating that GART entry multiple pages are not supported.
8	Valid_Cap	**ValCap** This bit is set to indicate that the AMD-761 system controller supports the detection of valid bit errors.
7–0	Rev_ID	**Revision ID** This field contains the revision identification.

Programming Notes

GART Directory Base Address — Bar1 + 0x04

	31	30	29	28	27	26	25	24
Bit	GART_Dir_Base_Addr							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	GART_Dir_Base_Addr							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	GART_Dir_Base_Addr				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

	7	6	5	4	3	2	1	0
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

Register Description

Bit Definitions — GART Directory Base Address (Bar1 + 0x04)

Bit	Name	Function
31–12	GART_Dir_Base_Addr	**GART Directory Base Address** These bits define the base address of the GART directory that is located in physical system memory. These 20 bits correspond to the 20 most significant bits of the 32-bit GART directory base address that is aligned on a 4-Kbyte page boundary. Twenty bits provide 4-Kbyte resolution, which is the minimum allowable size of the GART. A value other than 0 defines a valid base address.
11–0	Reserved	**Reserved**

Programming Notes

GART Cache Size — Bar1 + 0x08

	31	30	29	28	27	26	25	24
Bit	GART_Cache_Size							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	GART_Cache_Size							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	GART_Cache_Size							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	GART_Cache_Size							
Reset	0	0	0	1	0	0	0	0
R/W	R							

Register Description

Bit Definitions — GART Cache Size (Bar1 + 0x08)

Bit	Name	Function
31–0	GART_Cache_Size	**GART Cache Size** The AMD-761™ system controller implements a GART table cache that contains 16 entries, organized as eight-way set associative.

Programming Notes

GART Cache Control — Bar1 + 0x0C

	31	30	29	28	27	26	25	24
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	23	22	21	20	19	18	17	16
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	15	14	13	12	11	10	9	8
Bit	Reserved							
Reset	0	0	0	0	0	0	0	0
R/W	R							

	7	6	5	4	3	2	1	0
Bit	Reserved							GART_Cache _Inval
Reset	0	0	0	1	0	0	0	0
R/W	R							R/W1S

Register Description

Bit Definitions — GART Cache Control (Bar1 + 0x0C)

Bit	Name	Function
31–1	Reserved	**Reserved**
0	GART_Cache _Inval	**GART Cache Invalidate** This bit is written by the AMD-761™ miniport driver. When set to 1, the AMD-761 system controller invalidates the entire GART directory and table cache. When the invalidate operation is completed, the AMD-761 system controller resets this bit to 0.

Programming Notes

GART Table Cache Entry Control — Bar1 + 0x10

	31	30	29	28	27	26	25	24
Bit	GART_Tbl_Entry_Addr							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	23	22	21	20	19	18	17	16
Bit	GART_Tbl_Entry_Addr							
Reset	0	0	0	0	0	0	0	0
R/W	R/W							

	15	14	13	12	11	10	9	8
Bit	GART_Tbl_Entry_Addr				Reserved			
Reset	0	0	0	0	0	0	0	0
R/W	R/W				R			

	7	6	5	4	3	2	1	0
Bit	Reserved						Tbl_Update	Tbl_Inval _Entry
Reset	0	0	0	0	0	0	0	0
R/W	R						R/W1S	

Register Description

This register must be written to with doubleword (32-bit or 4-byte) operands.

Bit Definitions **GART Table Cache Entry Control (Bar1 + 0x10)**

Bit	Name	Function
31–12	GART_Tbl_Entry _Addr	**GART Table Entry Address** These bits define the page address for the particular GART table entry to be invalidated or updated. When a page address is written to this register by the AMD-761™ miniport driver, the referenced GART table cache entry is invalidated or updated based on the value in bits [1:0] as long as it is within the virtual address space. If the page address is outside of the virtual address space, then the invalidate/update instructions do nothing.
11–2	Reserved	**Reserved**
1	Tbl_Update	**Table Update** When set, this bit forces the AMD-761 system controller to update the GART table cache entry specified in bits [31:12] with the current entry in the GART table in system memory. The update function is performed immediately following the write to this register. When the update operation is completed, this bit is reset to 0.
0	Tbl_Inval_Entry	**Table Invalidate Entry** When set, this bit forces the AMD-761 system controller to invalidate the GART table cache entry specified in bits [31:12] if it is present in the GART cache. The invalidate function is performed immediately following the write to this register. When the invalidate operation is completed, this bit is reset to 0. Note that this bit does not affect the GART directory cache.

Programming Notes

3 DDR SDRAM Interface

This chapter details BIOS configuration as it pertains to the AMD-761™ system controller DDR SDRAM controller. The topics discussed in this chapter are entitled as follows:

3.1 Overview

To date, there are two types of DDR memory DIMMs—unbuffered and registered. The AMD-761 system controller can be configured to support up to two unbuffered DIMM slots with two banks each, or up to four registered DIMM slots with two banks each. Registered and unbuffered implementations cannot be intermixed.

The AMD-761 system controller embeds the DDR SDRAM memory controller of the system. All programming registers that configure the memory controller reside in PCI configuration space. This space is defined in Bus 0, Device 0, and exists in both Function 0 and Function 1.

Motherboard and Northbridge characteristics are programmed from data provided by the respective designers and manufacturers. This data includes bus speed implementations, memory bus signal strengths and slew rates, and internal memory controller characteristics, etc.

DIMM and memory device (memory chip) timing and configuration data exist in the Serial Presence Detect (SPD) EEPROM on the DIMM.

3.2 DDR DIMMS and DDR SDRAMs

The following section discusses DDR DIMMS and DDR SDRAMS.

3.2.1 DDR Speed Grades

DDR DIMMs adhere to an alternate naming convention associated with a corresponding data transfer rate. The data rate is a function of the clock speed of the memory subsystem, for example, 100-MHz clock or 133-MHz clock. Two names, and their corresponding transfer rates, are currently defined and implemented:

- PC1600
- PC2100

The PC1600 naming convention represents DIMMs with a data transfer rate of 1600 Mbytes per second (1.6 Gbytes per second). This data rate is calculated as follows:

PC1600 data transfer rate = (100-MHz clock) x (2 data transfers/clock) x (8 bytes/transfer)

PC1600 data transfer rate = 1600 Mbytes per second

Similarly, the PC2100 designation represents DIMMs with a data rate of 2100 Mbytes per second (2.1 Gbytes per second). This data transfer rate is calculated as follows:

PC2100 data transfer rate = (133-MHz clock) x (2 data transfers/clock) x (8 bytes/transfer)

PC2100 data transfer rate = 2100 Mbytes per second (rounded)

Note that the CAS latency (CL) parameter of the device does not factor into the PC 1600 and PC2100 transfer rates calculated above. The CAS latency setting is dependent on device frequency, which is used in the calculation of the transfer rates above. The CAS latency values are DDR device-

specific and based on the operating frequency of the device. The CAS latency is specified as the initial latency (in clocks) required by the device before data is returned during a read access. In general, the higher the frequency, the larger the CAS latency value. Typical device CL parameters and their respective frequencies are shown in Table 17.

Table 17. Typical CL Parameter Settings for PC1600 and PC2100

Designation	CAS Latency (CL) Setting	DDR Memory Clock Speed
PC1600	2	100 MHz
PC2100	2.5	133 MHz

Note: *CAS latency settings are valid **only** if an acceptable entry for the corresponding bus speed exists in SPD byte 9 or 23.*

3.2.2 DDR DIMM Data from Serial Presence Detect (SPD) Device

DDR memory systems implemented with the AMD-761 system controller require use of the Serial Presence Detect (SPD) data. This data describes configuration and speed characteristics of the DDR DIMM and DDR SDRAM devices mounted on the DIMM. The SPD is a serial EEPROM that physically exists on the DIMM and is encoded by the DIMM manufacturer. A description of this EEPROM is usually provided on a data sheet for the DIMM itself along with data describing the memory devices (chips) used. The data sheet should also contain the byte values for the DIMM encoded in the SPD on the DIMM. The SPD is accessed via the I^2C bus implemented on the motherboard, normally via registers in a Southbridge agent. Subroutines to access SPD data must be provided in the BIOS or other code that requires access.

The I^2C bus addresses the SPD via a 7-bit address where convention dictates that memory DIMMs respond to an address range beginning with 0xA0. The second memory DIMM responds to 0xA2 and so on.

The I^2C bus specification describes a 7-bit address. However, this scheme actually uses 8 bits. The 8th bit is actually bit 0. The scheme defines bit 0 as the read/write designation of the address. Bit 0 equal to 0 means that the host is executing a WRITE to the address. Bit 0 equal to 1 means that the host is executing a READ from the address. Reality then is that A1 addresses a read operation to DIMM slot #0. A3 addresses a

read operation to DIMM slot #1. A0 addresses a write operation to DIMM slot #0.

3.3 Memory Space Configuration

A DIMM may have one or two sides populated with DDR devices. The term bank refers to one logical side of the DIMM memory. For the purpose of this document, each bank has a corresponding chip select. It is important to point out that double-sided DIMMs require two separate chip-select signals. Therefore, for these types of DIMMs, two separate base address chip-select registers must be programmed. The size of each bank is read from SPD, byte 31. The number of banks on the DIMM is read from SPD byte 5.

The AMD-761 system controller DDR SDRAM controller requires 21 bits of configuration information for each chip select—that is, each side of the DIMM. These 21 bits are within a full 32-bit configuration register that contains 11 reserved bits. Usage of the 32 bits is shown in Table 18 and explained in further detail below.

As previously mentioned, a DIMM socket may be single banked (containing one logical side of DDR SDRAM devices) or double banked (containing two logical sides of DDR SDRAM devices). The DIMM socket may also be empty. If one bank is not present or if the socket is empty—that is, two banks not present—then their corresponding enable bit shown in Table 18 should be set to 0.

Table 18. DIMM Bank Address Bit Definition

Bit(s)	Bank n
0	1 = Enable 0 = Disable
2:1	Address Mode (modes 00 and 11 are reserved)
15:7	Address Mask – Size of this bank
31:23	Base Address – Starting address of this bank

It is important that the registers place the largest logical bank of memory in the lowest address space and then progress in order to higher address space with the smaller sized banks.

When the DIMM socket sides are equally sized, the order of address space programming between them is not important.

Each side/row/bank of DRAM requires 4 bytes as previously stated. The patterns that satisfy the Address Mask and Base Address for various sizes of sides/rows/banks are shown in Table 19.

Table 19. Memory Size Addresses

Bank / Row Size [Address Lines]	Address Mask [31:23]	Base Address [31:23]
8 Mbytes	N/A	0000_0000_1
16 Mbytes	N/A	0000_0001_0
32 Mbytes	0000_0001_1	0000_0010_0
64 Mbytes	0000_0011_1	0000_0100_0
128 Mbytes	0000_0111_1	0000_1000_0
256 Mbytes	0000_1111_1	0001_0000_0
512 Mbytes	0001_1111_1	0010_0000_0
1024 Mbytes (1 Gbyte)	0011_1111_1	0100_0000_0
2048 Mbytes (2 Gbytes)	0111_1111_1	1000_0000_0

The address mask and base address bits are presented as xxxx_xxxx_x to show correspondence with address lines. In practice, the 9 bits of address mask map to bank n, bits 15:7 and the 9 bits of base address map to bank n, bits 31:23.

The minimum memory size or granularity for DDR is 32 Mbytes. However, all base address and address mask bits represent a granularity of 8 Mbytes.

The symmetry of the DDR device—that is, organization of storage elements rows and columns—dictates the addressing mode configuration. The specified addressing mode dictates the physical mapping of the memory address signals to the DDR device address signals. The addressing modes of the AMD-761 system controller memory controller map to industry-standard DDR device symmetries set forth by the Joint Electron Device Engineering Council (JEDEC). Therefore, the addressing mode is set according to the devices on the DIMM.

- Addr_Mode => 01b for 64-Mbit and 128-Mbit DRAMs
- Addr_Mode => 10b for 256-Mbit and 512-Mbit DRAMs

Note: *Modes 00b and 11b are reserved.*

To determine the size of the DDR SDRAM device from SPD data, BIOS needs to read the size of the bank(s) in SPD byte 31 and the device width in byte 13. DDR SDRAM widths are either 4, 8, or 16 for this implementation. A 4-bit device width implies that 16 DDR SDRAM devices exist on a DIMM for a 64-bit bus transfer. An 8-bit device width implies eight DDR SDRAM devices exist on a DIMM for a 64-bit bus transfer, and a 16-bit width implies four DDR SDRAM devices exist on a DIMM for the 64-bit bus transfer. The size of the bank can be deduced as:

Size of Device(Mbits) = Size of Bank x (SDRAM Width)

where the Size of Device is specified in Mbits. Dividing the Size of Device value by eight (8) yields the size of the bank in Mbytes.

If more than 4 Gbytes of total memory are populated in the system, it is the responsibility of BIOS to configure and report only 4 Gbytes to prevent a 4-Gbyte wrap, which would result in aliasing. Table 20 shows the total amount of memory with respect to DDR device density and width.

Table 20. Total Memory

Width and Density	DIMM 0	DIMM 1	DIMM 2	DIMM 3
X16 128 Mbit	128 Mbytes	256 Mbytes	384 Mbytes	512 Mbytes
X8 128 Mbit	256 Mbytes	512 Mbytes	768 Mbytes	1 Gbytes
X4 128 Mbit	512 Mbytes	1 Gbytes	1.5 Gbytes	2 Gbytes
X16 256 Mbit	256 Mbytes	512 Mbytes	768 Mbytes	1 Gbytes
X8 256 Mbit	512 Mbytes	1 Gbytes	1 Gbytes	2 Gbytes
X4 256 Mbit	1 Gbyte	2 Gbytes	3 Gbytes	4 Gbytes
X16 512 Mbit	512 Mbytes	1 Gbytes	1.5 Gbytes	2 Gbytes
X8 512 Mbit	1 Gbyte	2 Gbytes	3 Gbytes	4 Gbytes
X4 512 Mbit	2 Gbytes	4 Gbytes		

Note: *This table assumes double sided DIMMs.*

Note: *Total system maximum is 4 Gbytes.*

Note: *Shaded rows use x4 devices that are as registered DIMMs only.*

This document assumes that BIOS uses the SPD to determine the total amount of memory in the system. This document does **not** specify a sizing algorithm other than utilizing the SPD.

Base Address Chip Select

The Base Address Chip Select bits (Dev 0:F0:0xC0, bits [31:23] through Dev 0:F0:0xDF, bits [31:23]) specify the 8-Mbytes boundary a given chip-select services. Each of the eight chip selects [7:0] have an associated Base Address Chip Select register. Incoming addresses are compared against the value programmed into the Base Address Chip Select register and also the Address Mask bits (Dev 0:F0:0xC0, bits [15:7] through Dev 0:F0:0xDF, bits [15:7]) of this register.

Address Mask

The Address Mask bits (Dev 0:F0:0xC0, bits [15:7] through Dev 0:F0:0xDF, bits [15:7]) specify which address bits to ignore when incoming addresses are compared to the Base Address Chip Select bits Dev 0:F0:0xC0, bits [31:23] through Dev 0:F0:0xDF, bits [31:23]) defined in Base Address Chip Select. If a given bit is set in this register, its corresponding address bit in the address compare is ignored.

Address Mode

The Address Mode bits (Dev 0:F0:0xC0, bits [2:1] through Dev 0:F0:0xDF, bits [2:1]) specify the memory address mapping. The address memory mapping is specific to the symmetry of the device and is shown in Table 21. As can be seen in this table, the maximum page width is 2 Kbytes. This maximum width implies that a new internal bank is accessed on a 2-Kbyte boundary. Note that address modes 00b and 11b are reserved, thus this field should never be specified.

Table 21. AMD-761™ System Controller DDR SDRAM Addressing Modes

Mode	Pins	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode 1 Addr_Mode=01 64Mb x4/8/16 128Mb x4/8/16	**Row**	12	11		24	23	22	21	20	19	18	17	16	15	14	13
	Col	12	11		27	PC	26	25	10	9	8	7	6	5	4	3
		BK	BK													
Mode 2 Addr_Mode=10 256Mb x4/8/16 512Mb x4/8/16	**Row**	12	11	25	24	23	22	21	20	19	18	17	16	15	14	13
	Col	12	11	29	28	PC	27	26	10	9	8	7	6	5	4	3
		BK	BK													

Chip Select Enable

The Chip Select Enable bit (Dev 0:F0:0xC0, bit [0] through Dev 0:F0:0xDF, bit [0]) specifies whether a bank of memory exists for that corresponding chip select. When enabled with a 1b, the incoming address is eligible to be compared with bits [31:23] and [15:7] for chip-select decode. A 0b in this field disables the associated chip select, thus the associated Base Address Chip Select and Address Mask fields are ignored.

Example: Memory Base Address Registers

Table 22 is an example of how to size the Memory Base register for a total of 128 Mbytes using a two-bank DIMM at 64 Mbytes per bank.

Table 22. Memory Sizing Example, 128 Mbytes Total

Registers – Bus:00 Device:00 Function:00																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	83	03	00	00	83	03	00	04	00	00	00	00	00	00	00	00
D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

For the purpose of illustrating memory sizing, the bytes 0xC0–0xDF are the relevant bytes. Configuration bytes C0h, C1h, C2h, and C3h are for Bank 0. Byte C0h contains bits [7:0], C1h bits [15:8], etc. This example shows 64 Mbytes in both banks 0. Configuration bytes C4h, C5h, C6h, and C7h are for bank 1

Bits C0h[7] and C1h[7:0] contain the Address Mask for 64 Mbytes.

Bits C4h[7] and C5h[7:0] contain the Address Mask for 64 Mbytes.

Bit C0h[0] and bit C4h[0] signal Bank Enable.

Bit C2h[7] and bits C3h[7:0] set a Base Address of 0 Mbyte for side/row/bank 0.

Bit C6h[7] and bits C7h[7:0] set a Base Address of 64 Mbytes for side/row/bank 1.

The total memory size is 128 Mbytes. Banks 2–7 are empty. The relevant bytes are set to 0.

Table 23 is an example on how to size the Memory Base register for a total of 320 Mbytes using one-bank DIMM at 64 Mbytes per bank and a two-bank DIMM at 128 Mbytes per bank.

Table 23. Memory Sizing Example, 320 Mbytes Total

Registers – Bus:00 Device:00 Function:00																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	83	03	00	10	00	00	00	00	83	07	00	00	83	07	00	08
D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

3.4 DDR Memory DIMM Timings

One of the most important changes from earlier SDRAM DIMM technology is that conservative settings for CAS Latency (CL) are no longer valid—that is, when there is doubt that the DIMM works using CL=2, falling back to a setting of CL=3 is not an alternative as it was on single data rate devices.

CAS latency for a DIMM **must** be set to a value described in the SPD on the DIMM. A DIMM that is set to something other than a rated value in its SPD cannot be expected to work and most likely will not work.

Industry standards for CL on DDR DIMMS are 1.5, 2.0, and 2.5. Please notice that the AMD-761 system controller supports CL=3.0 as the highest CL setting. Some legacy DDR devices support CL=3.0, but most devices available today specify CL=2.5 as a maximum. The AMD-761 system controller does **not** support CL=1.5.

3.4.1 Memory Timings

The AMD-761 system controller supports the following DDR device timing parameters: t_{CL}, t_{RCD}, t_{RAS}, t_{RP}, t_{RC}, t_{RRD}, t_{WR}, and t_{WTR}. The t_{CL}, t_{RCD}, t_{RAS}, t_{RP}, t_{RC}, and t_{RRD} timings are available from the SPD. The data format of each byte is described in the application note published by IBM and other sources. Matching this data to memory controller settings is a function of speed of the memory bus. Examples of settings are developed for bus speeds of 100 MHz and 133 MHz.

CAS Latency

CAS latency values can occupy multiple bytes in the SPD. CAS latency is the only item governing DIMM setup that has multiple values. Table 24 shows CAS latency settings.

Table 24. CAS Latency Settings

Symbol	Name	SPD Byte	Typical Value	Description
t_{CL}	CAS Latency 0x0x0x54[3:2]	9		Max bus speed for CL=2.5 with AMD-761™ system controller.
			0	DIMM does not support CL=2.5.
			75h	75h equal 7.5 ns. This DIMM can be used @ CL = 2.5 when bus speed is less than or equal to 133 MHz.
			A0h	A0h equals 10 ns. This DIMM can be used @ CL = 2.5 when bus speed is less than or equal to 100 MHz.
		23		Max bus speed for CL=2 with AMD-761™ system controller.
			0	DIMM does not support CL=2.
			75h	75h equal 7.5 ns. This DIMM can be used @ CL = 2 when bus speed is less than or equal to 133 MHz.
			A0h	A0h equals 10 ns. This DIMM can be used @ CL = 2 when bus speed is less than or equal to 100 MHz.

Notes:

1. *Other values in byte 9 represent other maximum bus speeds for CL=2.5. Should another speed occur, CL=2.5 cannot be used beyond its max for this DIMM–that is, byte 9 = 80 means a maximum bus speed of 120 MHz. CL=2.5 can be used for a maximum bus speed of 100 MHz, but not for 133 MHz.*
2. *Other values in byte 23 represent other maximum bus speeds for CL=2. Should another speed occur, CL=2 cannot be used beyond its max for this DIMM–that is, byte 23 = 80 means a maximum bus speed of 120 MHz. CL=2 can be used for a maximum bus speed of 100 MHz, but not for 133 MHz.*

The two entries for supported CAS latency(CL) represent different performance potential. The smaller value for CL (2) would represent best performance. BIOS can choose from any legal CL that exists in the SPD for the DIMM. The AMD-761 system controller supports CL values of 2, 2.5, and 3.

Other timing values in the SPD reflect minimum timings required, based on the corresponding memory bus clock speed. BIOS must program the memory controller configuration with the correct timing values as specified by the DDR device.

t_{RCD} The RAS to CAS delay bits (Dev 0:F0:0x54, bits [1:0]) specify the minimum amount of time required between the opening of a page within the DDR device (via an ACTIVATE command) and the issuance of a READ or WRITE command to that same DDR device's internal bank. This timing parameter is device-specific. Byte 29 of the SPD defines the t_{RCD} timing parameter. Refer to Table 25 on page 160 for typical settings.

t_{RAS} The Row Active bits (Dev 0:F0:0x54, bits [6:4]) specify the minimum amount of time that a page within the DDR device (via an ACTIVATE command) can remain opened within the same internal bank of the DDR device. This timing parameter is device-specific. Byte 30 of the SPD defines the t_{RAS} timing parameter. Refer to Table 25 on page 160 for typical settings.

t_{RP} The Row Precharge time bits (Dev 0:F0:0x54, bits [8:7]) specify the minimum amount of time that the DDR device requires to precharge a row and is specified as the time between the PRECHARGE command and an ACTIVATE command within the **same** internal bank of the DDR device. This timing parameter is DDR device-specific. Byte 27 of the SPD defines the t_{RP} timing parameter. Refer to Table 25 on page 160 for typical settings.

t_{RC} The Row Cycle time bits (Dev 0:F0:0x54, bits [11:9]) specify the minimum amount of time that the DDR device requires between ACTIVATE commands within the **same** internal bank of the DDR device. This timing parameter is DDR device-specific. In short, this requirement specifies the minimum amount of time that the **same** internal bank can recycle row accesses. Byte 41 of the SPD defines the t_{RC} timing parameter. (Note that t_{RC} is new to the SPD and voted in at the September 2000 JEDEC meeting.) Historically, t_{RC} was defined as t_{RAS} + t_{RP}, but this algorithm is not recommended when the SPD information is available. Refer to Table 25 on page 160 for typical settings.

t_{RRD} The Bank to Bank ACTIVATE time bit (Dev 0:F0:0x54, bit [23]) specifies the minimum amount of time that the **same** DDR device can receive back-to-back ACTIVATE commands, even to **different** internal banks. This timing parameter is DDR device-specific. Device manufacturers specify the t_{RRD} parameter to limit current surges within the device, based on row ACTIVATE activity, because row activates require a large amount of

current. Byte 28 of the SPD defines the t_{RRD} timing parameter. Refer to Table 25 on page 160 for typical settings.

Write Recovery

The Write Recovery bits (Dev 0:F0:0x54, bit [25:24]) specify the minimum amount of time that must occur from the last WRITE command to a PRECHARGE command to the **same** internal bank of the DDR device. This device timing parameter is not specified in the SPD, but the recommended setting is 10b and specifies two system clock cycles between a write command and a precharge command to the **same** internal bank. Refer to Table 25 on page 160 for typical settings.

Write to Read

The Write To Read bit (Dev 0:F0:0x54, bit [26]) specifies the minimum amount of time that must occur between the last WRITE command to a following READ command to the **same** internal bank of the DDR device. This device timing parameter is not specified in the SPD, but the recommended setting is 1b and specifies two system clock cycles. Refer to Table 25 on page 160 for typical settings.

Table 25. DDR Device Timing Values

Symbol	Name	SPD Byte	Typical Value	Description
t_{RCD}	Minimum RAS to CAS Delay 0x0x0x54[1:0]	29	50h	Has 2-bit fraction—see SPD definitions. 50h = 20 ns. 2 cycles @100 MHz, 3 @ 133 MHz.
t_{RAS}	Minimum Active to Precharge Time 0x0x0x54[6:4]	30	32h	Integer value. 50-ns requirement. 5 cycles @ 100 MHz, 7 @ 133 MHz.
t_{RP}	Minimum Row Precharge Time 0x0x0x54[8:7]	27	50h	Has 2-bit fraction—see SPD definitions. 50h = 20 ns. 2 cycles @100 MHz, 3 @ 133 MHz.
t_{RC}	Bank Cycle Time 0x0x0x54[11:9]	41		Typically defined as t_{RAS} + t_{RP}. SPD entry available soon. 7 cycles @ 100 MHz, 10 @133 MHz.
t_{RRD}	Minimum Row Active to Row Active Delay 0x0x0x54[23]	28	3Ch	Has 2-bit fraction—see SPD definitions. 3Ch = 15 ns. 2 cycles @100 MHz and 133 MHz.
t_{WR}	Minimum Write to Precharge Time	N/A	N/A	
t_{WTR}	Minimum Write to Read Time	N/A	N/A	

Example configurations are shown in Table 26.

Table 26. Dev 0:F0:0x54 Bit Examples

CL	DIMM	Dev 0:F0:0x54 57 56 55 54
2	100 MHz Unbuffered	16 01 88 B5
2	100 MHz Registered	7E 01 88 B5
2.5	133 MHz Unbuffered	96 01 8C 4A
2.5	133 MHz Registered	F6 01 8E 5A

3.5 Additional Memory Controller Settings

This section discusses configuration features that are specific to the AMD-761 system controller DDR memory controller. The AMD-761 memory controller contains DDR memory controller settings starting at (Dev 0:F0:0x54). These settings are Page Hit Limit, Idle Cycle Limit, Registered DIMM Enable device control (used in this register to specify registered versus unbuffered DIMM), Read Wait State timing control, selectable HOLD time for the DDR address and command buses (selectable per address and command bus A and B), and a selectable wait state for Super Bypass control.

Page Hit Limit

The Page Hit Limit bits (Dev 0:F0:0x54, bits [15:14]) specify the number of consecutive Page Hit requests that are processed by the AMD-761 DRAM controller before choosing a non-page hit request. This feature is designed to reduce starvation (a pending request not fulfilled for an extended period of time) due to a flood of consecutive page hit requests.

Typically, consecutive page hits yield the best DDR DRAM page performance for those requesting devices (such as the CPU or PCI device, etc.). However, starvation of a request because it is a non-page-hit request does not constitute a fair system memory access policy.

When the number of consecutive page hits across **all** internal DDR device internal banks of a given chip select equals the value specified in these bits, the DDR controller arbiter gives priority to a DDR memory request that is **not** a page hit. It was determined that eight consecutive page hit accesses is

adequate to give fair access to the memory sub-system. Therefore, these bits should be set to 10b. A higher page hit limit allows the prioritization of a large amount of consecutive page hits, if available, whereas a lower page hit limit would allow for a greater chance of page interruption should there be an otherwise large amount of page hit requests. Refer to Table 27 on page 165 for typical settings.

Idle Cycle Limit

The Idle Cycle Limit bits (Dev 0:F0:0x54, bits [18:16]) specify the number of system clocks before the memory controller issues a PRECHARGE ALL command to the currently active chip select. This feature is used to tune system performance by closing open pages during periods of memory request inactivity. The idle cycle limit logic does not have any logical indication of page conflicts or bank misses and simply counts the number of system clocks of memory request inactivity. This feature takes advantage of the lack of temporal locality, where a page left open for a specified amount of time is less likely to be accessed again. Therefore, it is more advantageous to precharge the page and incur the page miss overhead rather than the overhead associated with a page conflict.

Analysis shows that eight idle clocks is an adequate amount of system clocks to wait for a following request to the memory sub-system. Therefore, these bits should be set to 001b for best performance. A higher idle cycle limit allows a greater chance for a following request to access an open page. However, temporal locality states that the greater amount of time between accesses reduces the chance of a hit to the open page. A lower idle cycle limit decreases the window of following memory access to utilize an open page. A lower idle cycle limit results in a greater chance of page interruption should there be an otherwise large amount of page hit requests. Refer to Table 27 on page 165 for typical settings.

Registered DIMM Enable

The Registered DIMM Enable bit (Dev 0:F0:0x54, bits [27]) specifies whether the DDR DIMM sockets are populated with registered or unbuffered DIMM modules. This bit is set to 1b by BIOS if the DIMM sockets are populated with DDR-registered DIMM modules. The AMD-761 system controllerAMD-761 system controller memory controller does not support the mixing of registered and unbuffered DDR modules in the same system. The system must be populated

with either all registered or all unbuffered DDR modules. Refer to Table 27 on page 165 for typical settings.

Read Wait State

The Read Wait State bit (Dev 0:F0:0x54, bits [28]) specifies whether more time is needed in the DDR read data round trip loop. The read data round trip loop originates at the AMD-761 system controller DDR CLK outputs and terminates at the AMD-761 system controller internal requester logic. Because all DDR read data is returned with its corresponding DQS signal, read data is captured at the memory controller interface in the DQS clock domain. This data is then held and crosses into the core requester clock domain. However, because of the physical DIMM placement on the motherboard, large round trip delays the response time of the DDR devices, and AMD-761 system controller internal delays may be long enough that an additional wait state must be added to compensate for the delay. When this bit is set to a 1b, the data captured in the DQS clock domain is transferred to a register array that is within the core logic clock domain and physically exists at the pads of the AMD-761 system controller DDR interface. When this bit is set to a 1b, the data is delayed to the requester by one additional system clock period.

Because the Read Wait State bit is related to the full read data round trip and may imply that the read data and DQS are being returned from a far DIMM, when the Read Wait State bit is set to 1b, one additional clock cycle is placed between READ followed by WRITE cycles to prevent data and DQS overlap when accessing a far DIMM for read data and followed immediately by a write cycle.

Because of motherboard timing analysis and AMD-761 system controller timing analysis, it is recommended that this bit be set for 100-MHz and 133-MHz operation. Refer to Table 27 on page 165 for typical settings.

Address Timing for Copy-B

The address timing for Copy-B bit (Dev 0:F0:0x54, bit [29]) specifies additional HOLD time for the address and command bus B. When this bit is set to 1b, the memory address bus (MAB[14:0]), RASB#, CASB#, WEB#, CKEB, and CS[7:6 and 3:2]# is delayed an additional 350 ps (best case) and 600 ps (worst case) to provide additional HOLD time to the DDR device. This bit should be set by BIOS when registered DIMMs are installed and set to 0b when unbuffered DIMMs are installed.

This bit assumes A bus and B chip-select DIMM socket mapping is such that the B bus uses Chip Select bit [7:6] and [3:2]. This motherboard mapping should be adhered to should BIOS want to control the A bus and B bus HOLD timing separately. Refer to Table 27 on page 165 for typical settings.

Address Timing for Copy-A

The address timing for Copy-A bit (Dev 0:F0:0x54, bit [30]) specifies additional HOLD time for the address and command bus A. When this bit is set to 1b, the memory address bus (MAA[14:0]), RASA#, CASA#, WEA#, CKEA, and CS[5:4 and 1:0]# is delayed an additional 350 ps (best case) and 600 ps (worst case) to provide additional HOLD time to the DDR device. This bit should be set by BIOS when registered DIMMs are installed and set to 0b when unbuffered DIMMs are installed.

This bit assumes A bus and B chip-select DIMM socket mapping is such that the B bus uses Chip Select bit [5:4] and [1:0]. This motherboard mapping should be adhered to should BIOS want to control the A bus and B bus HOLD timing separately. Refer to Table 27 on page 165 for typical settings.

Super Bypass Wait State

The Super Bypass Wait State bit (Dev 0:F0:0x54, bit [31]) specifies an additional one system clock wait state for super bypass requests, when set to 1b. A super bypass cycle is a low-latency request to DDR memory from the bus interface unit when all reordering queues are empty. This super bypass cycle allows direct access to DDR memory. For internal timing reasons, this bit must be set for 133-MHz operation. This bit should be set to 0b for 100-MHz operation or below. Refer to Table 27 for typical settings.

Table 27. System Related Timings

Name	0x0x0x54 Bit(s)	Typical Setting	Description
Page Hit Limit	15:14	10b	8 cycles
Idle Cycle Limit	18:16	001b	8 cycles
Registered DIMM Enable	27	x	0 for unbuffered 1 for registered
Read Wait State	28	1	Always set
Address Timing for Copy-B	29	x	0 for unbuffered 1 for registered
Address Timing for Copy-A	30	x	0 for unbuffered 1 for registered
Super Bypass Wait State	31	X	0 < 133 MHz 1 @ 133 MHz

3.6 DRAM Mode/Status Settings

The AMD-761 system controller memory controller contains additional DDR memory controller settings starting at (Dev 0:F0:0x58). These settings are: x4 DDR device symmetry configuration, refresh control (which includes refresh rate, refresh disable, and burst refresh enable), suspend to RAM (STR) control, DDR device initialization control, and AMD-761 system controller DDR clock output control.

Chip-Select Width

The SDRAM Chip-Select Width bits (Dev 0:F0:0x58, bits [7:0]) are used to indicate DDR device data widths installed for the corresponding chip select. The AMD-761 system controller can differentiate between x4 **or** x8/x16 banks by BIOS setting a corresponding bit for the chip select in this register. A bit should be set to 1b to represent a x4 bank or set to 0b to represent a x8/x16 bank.

The x8 and X16 devices use one DQS data strobe per byte, whereas a x4 device uses one DQS data strobe per nibble (4-bit). Because the AMD-761 system controller DRAM controller uses the data mask (DM) signals as DQS data strobes during data transfers to x4 devices, the DRAM controller uses these bits to determine the function for the DM signals. The

AMD-761 system controller provides a data width selection for each chip select, although it is unlikely that a double banked DIMM can support x4 devices on one side and x8/x16 devices on the other. However, this resolution is provided to allow chip-select signal routing flexibility on the motherboard should the same DIMM socket not use neighboring chip-select wiring.

The SPD byte 13 provides DDR device data width information and can be used to set these bits accordingly.

SDRAM Initialization

The SDRAM Initialization bit (Dev 0:F0:0x58, bit [25]), when written to a 1b, initiates the DDR device initialization sequence. However, as mentioned below, the Suspend to RAM bits (Dev 0:F0:0x58, bits [22:21]) must be written to a 01b in order for the initialization sequence to occur. The BIOS should first initialize the DDR timing control registers and drive strength registers prior to setting this bit. This bit remains set after the initialization sequence has completed. Status as to the completion of the initialization sequence can be provided by polling the Mode Register Status (Dev 0:F0:0x58, bit [23]) but only after setting the Mode Register Status bit. This procedure is described below. The SDRAM Initialization bit is reset to 0b during a Suspend To RAM because a system reset is issued in this case.

Mode Register Status

The Mode Register bit (Dev 0:F0:0x58, bit [23]), when written with a 1b, is used to initiate a Load Mode Register command to the DDR devices. The Load Mode Register command programs the CAS latency of the device, burst length, and burst order. The burst length and burst order are fixed to a burst of eight and the device is programmed for interleaved mode. However, the CAS latency is configurable via the CAS Latency bit. BIOS must set the CAS latency bit to its correct value (defined by DDR devices specification and operating frequency) **before** the Mode Register bit is set. This bit is then cleared by the AMD-761 system controller memory controller after the load mode register cycle is issued to the DDR devices. Therefore, after setting this bit, BIOS should poll this bit until it becomes 0b to verify that the Load Mode Register command has been applied to the DDR devices before continuing. The recommended method is to set this bit (after already initializing the CAS Latency bit) when writing to this register to set bits [22:21] of this register to a 01b and bit 25 of this register to a 1b. Because the DDR initialization has priority

over the application of the Load Mode Register command and the Load Mode Register command is the last command applied in the DDR initialization, this bit can be polled to prove status as to when the entire DDR initialization is complete.

Suspend to Ram Control

The Suspend to RAM bits (Dev 0:F0:0x58, bits [22:21]) are used by BIOS to communicate the power-up sequence to the AMD-761 system controller.

The BIOS usage of the Suspend to RAM control bits are defined in the power management section (see Section 4.4.1 on page 191).

Burst Refresh Enable

The Burst Refresh bit (Dev 0:F0:0x58, bit [20]) allows the AMD-761 system controller to skip refreshes that are queued, until the maximum number (four) is reached.

Burst refresh support is a performance enhancement that prevents refresh requests from interfering with memory requests. Refresh requests that would have interfered with memory requests would normally stall the memory accesses or interfere with the open page policy by prematurely closing pages due to the refresh. When burst refresh is enabled and the burst queue is beginning to fill up, the DRAM controller treats the refresh queue requests as an urgent priority.

Refresh Disable

The Refresh Disable bit (Dev 0:F0:0x58, bit [19]) allows the disabling of refresh cycles for debug purposes only. This bit is not reset during a system reset and it is therefore the responsibility of BIOS to write this bit to a 0 to enable refresh cycles.

Cycles per Refresh

The Cycles per Refresh bits (Dev 0:F0:0x58, bits [17:16]) provide a setting to specify the DDR refresh rate. The refresh rate is tied directly to the clock frequency, thus it is important for BIOS to configure the refresh rate based on the AMD-761 system controller frequency. BIOS should first determine the AMD-761 system controller operating frequency by reading (Dev 0:F0:0x58, bits [21:20]) and setting these bits according to Table 28 below. The refresh rate should not be configured slower than that specified by any of the DDR devices installed. (Each DIMM installed may have a different refresh requirement, so it is important to choose the refresh rate that satisfies the least common denominator for all DIMMs.)

Table 28. Refresh Rate

Value	66 MHz	100 MHz	133 MHz
00	30.72 µs	20.48 µs	15.36 µs
01	23.04 µs	15.36 µs	11.52 µs
10	15.36 µs	10.24 µs	7.68 µs
11	7.68 µs	7.68 µs	3.84 µs

DIMM Clock Disable

The DIMM clock disable bits (Dev 0:F0:0x58, bits [31:26]) provide a way to individually disable the six differential DDR clock pairs provided for the DDR DIMMs. After BIOS memory sizing, these bits can be used to disable clocks to empty DDR DIMM slots. The setting of a bit disables the corresponding clock pair. Each clock pair is connected according to the motherboard layout for registered or unbuffered DIMMs. Refer to the appropriate motherboard schematic to verify DDR clock DIMM mapping to a particular DIMM slot.

With a system hard reset, these bits are cleared, thus enabling all clock pairs. Because an AMD-761 system controller system reset is issued during a power-managed S3 state, all clocks are re-enabled following the exit from this state. Therefore, BIOS should return to this register and restore the disabled clock pairs that it had previously disabled during POST.

Note: *DDR clocks are automatically disabled during the S3 power-managed state when unbuffered DIMMs are installed but continue running an additional six clocks when registered DIMMs are installed.*

3.7 ECC and Memory Scrubbing

The AMD-761 system controller DDR SDRAM controller supports error correcting code (ECC) and memory scrubbing. The error correction capability allows the correction of single-bit errors and the detection of multiple-bit errors in any memory quadword. Data is only checked by the memory controller during a read access. A data error may be due to a faulted bit in the DDR device itself, or a faulted bit that occurred during data transmissions from the DDR devices to the AMD-761 system controller memory controller. To support the ECC function, DIMMs must support additional storage for the ECC check bits. When ECC is enabled, the system must have all DDR DIMMs that are 72 bits wide (also called ECC DDR DIMMs). The AMD-761 system controller DDR SDRAM controller provides five ECC modes. All ECC modes work correctly with either unbuffered or registered DDR DIMMs. The five modes supported are:

- ECC Disabled
- High-Performance EC Mode (EC_HiPerf mode)—Error Checking only, no correction, except to the AMD Athlon™ processor
- High-Performance ECC Mode (ECC_HiPerf mode)—Error Checking and Correction
- ECC with Scrubbing (ECC_Scrub mode)—Error Checking and Correction with Scrubbing
- Diagnostic ECC mode (ECC_Diag)

Each mode is discussed below.

The ECC check bits that are stored in the additional DDR devices on the DIMM are generated by the memory controller (based on a Hamming code algorithm) and written into the DIMMs check bit storage during a memory write operation when any ECC function is enabled. A single byte of check bits represents the associated quadword of data that is written into memory.

When any ECC mode is enabled and a read access is performed, the memory controller internally generates check bits based on the data value read (for each quadword of data read) and compares it with the check bits read along with the

data from the check bit storage of the DIMMs. If the generated value does not match the check bit value, then both values are used to detect the number of bits that contain errors and the bit positions that contain errors. If only a single-bit error is detected, the generated check bits and the read check bits are used to correct the bit and pass the corrected data back to the requester that requested the read data. This single-bit error is signalled for system status. A read requester may be either the AMD Athlon™ processor, PCI, AGP, APC, or GART. The detection of more than a single-bit error signals a multiple-bit system error and this data is **not** corrected. When any of the AMD-761 system controller ECC features are enabled, all DDR DIMMs installed must support ECC and all memory locations must be written to (initialized) prior to system operation to generate check bit values that match the data written for every location of memory. It is the responsibility of the BIOS to initialize all memory locations **prior** to any ECC function being enabled.

The additional logic to support the ECC function is costly in both silicon real estate and system timing. In the ECC modes that support data correction, one additional system clock must be used to generate the corrected data. However, because the AMD Athlon processor checks for its own errors, data is passed directly through the AMD-761 system controller without an additional system clock delay.

The detailed implementation of error detection and correction differs dependent on whether the read or write is from the processor or PCI, APC, AGP, or GART and whether the write is a full quadword or less than a full quadword in size. The processor generates ECC for all full quadword writes and checks and corrects (if necessary) on all reads. For processor, PCI, APC, AGP, or GART partial quadword writes, the memory system performs a read-modify-write operation by reading the existing memory location, correcting the memory data if necessary, merging in the modified bytes, generating new ECC, and writing the new value to memory. A read-modify-write operation is used only for all partial quadword writes. The data read from memory during a read-modify-write operation is checked and corrected before the merge/write operation. A detailed operation is further described in Table 29 on page 171.

Table 29. AMD-761™ System Controller ECC Behavior (with ECC Enabled)

Operation	ECC Generated By:	ECC Checked By:	SBEs[1] Corrected By:
AMD Athlon™ Processor System Bus Read	DRAM	AMD-761™ System Controller and AMD Athlon Processor	AMD Athlon Processor
AMD Athlon Processor System Bus Full Quadword Writes	AMD Athlon Processor	None	None
AMD Athlon Processor System Bus Partial Quadword Writes	AMD-761 System Controller RMW on each QW	AMD-761 System Controller[2]	AMD-761 System Controller[2]
PCI/APCI/GART[3] Read	DRAM	AMD-761 System Controller	AMD-761 System Controller
PCI/APCI/GART[3] Full Quadword Writes	AMD-761 System Controller	None	None
PCI/APCI/GART[3] Partial Quadword Writes	AMD-761 System Controller RMW on each QW	AMD-761 System Controller[2]	AMD-761 System Controller[2]

Notes:
1. Single-bit error (SBE).
2. The data read from memory is checked and corrected before the merge/write.
3. APCI =Alternate PCI on AGP interface.
4. The scrubbing circuit detects, corrects read errors, and writes the corrected data to memory.

Memory scrubbing not only corrects single-bit errors to the requesters and detects multiple-bit errors, but also writes the corrected single-bit error value back into memory when this feature is enabled. Refer to “ECC_Mode” on page 172 for more information regarding the memory scrubbing feature and configuration.

In addition to the status bits and chip-select identification, the AMD-761 system controller allows single-bit and/or multiple-bit errors to optionally assert SERR# to allow monitoring, logging, and analysis of ECC errors by software. SysECCEn bit should be set in the AMD Athlon processor when setting "Report ECC Syndrome case." SysECCEn has an MSR address of MSR C001_0010[15].

3.7.1 ECC and Memory Scrubbing Configuration

SERR_Enable

The System Error Enable bits (Dev 0:F0:0x48, bits [15:14]) control the AMD-761 system controller reporting of ECC errors to the system via the SERR# pin on the PCI bus. Note that SERR# assertion is still subject to the normal PCI SERR# Enable (Dev 0:F0:0x04, bit [8]). Error reporting options are as follow:

- 00 = SERR# assertion disabled
- X1 = Multiple bit errors force SERR# assertion
- 1X = Single bit errors force SERR# assertion

ECC_Diag

The Error Correcting Code Diagnostic Mode Enable (Dev 0:F0:0x48, bit [12]) provides a way to purposely corrupt the ECC check bits. When this mode is enabled, the AMD-761 system controller always writes 0x00h to the ECC check bit byte. During partial writes, the RMW sequence still occurs, but the ECC bits are always written to 0x00. This bit is useful for logic testing and ECC driver development. A check bit value of 0x00 is a valid check bit code, so care should be used to not corrupt a location where the user **does not** expect this valid check bit value to exist. In the ECC_Diag mode, the AMD-761 system controller always writes 0x00 to the ECC byte to aid testing of the ECC logic.

For reads, the ECC circuitry is unaffected by the ECC_Diag bit. The ECC code returned from memory is checked, and errors are reported in the ECC_Status bits as usual. Correction is not performed in this mode to PCI, AGP, APC, or GART. However, as mentioned earlier, because the AMD-761 system controller simply passes ECC and read data information directly to the AMD Athlon processor, the processor may correct this data if this feature is enabled in the processor.

ECC_Mode

The Error Correcting Code mode bits enable a specific ECC mode. These fields can be used in the following cases:

- Disable ECC checking. In this mode, ECC is neither generated nor maintained in the memory, and correction is not performed. This mode is intended for memory systems that are only 64 bits in width.
- Enable ECC error checking mode **only** where data is still checked and errors are still reported, but data destined for the PCI or APCI/GART is **not** corrected. This approach

provides the benefit of detecting an error but does not incur the one clock penalty that is necessary for data correction for data destined for the PCI or AGP. Data and ECC check bits are still passed from the DDR devices to the AMD Athlon processor, which performs its own data error detection and correction. Therefore, data correction to the AMD Athlon processor is not inhibited in this mode. This mode provides all the benefits of parity checking with little or no performance impact. It is useful in systems that desire status information but not the overhead that is associated with error correcting or scrubbing. A system can transition between the EC_HiPerf mode, ECC_HiPerf mode, and ECC_Scrub mode dynamically, thereby getting the desired benefits of each mode as needed.

- Enable ECC error checking **and** correction mode. Data destined for the PCI or APCI/GART is corrected but at the expense of one clock cycle. As always, data and ECC check bits are still passed from the DDR devices to the AMD Athlon processor, which performs its own data error detection. The AMD-761 system controller provides a high-performance ECC mode (ECC_HiPerf) that provides all the data integrity benefits of ECC but without the overhead of scrubbing. In this mode, ECC is written into memory during writes (partial writes result in a RMW sequence), and correction is performed on reads. ECC checking is performed and the status indicators provide valid information regarding errors. This mode is useful in systems that need status information and data integrity but not the overhead that is associated with scrubbing. A system can transition between the EC_HiPerf mode, ECC_HiPerf mode, and ECC_Scrub mode dynamically, thereby attaining the desired benefits of each mode as needed.
- Enable ECC_Scrub mode where error checking, data correction, and memory scrubbing are enabled. Memory scrubbing corrects a detected single-bit error in the DDR memory. When a single-bit error is detected, additional cycle overhead is associated with correcting the single-bit error in memory. ECC with scrubbing (ECC_Scrub) mode is the ECC mode of highest reliability. In ECC_Scrub mode, ECC is written into memory during writes (partial writes result in a RMW sequence), and corrected data is provided to the PCI/APCI/GART on reads. The AMD-761 system controller checks the ECC returned from memory and sets

the ECC status indicators. In addition, the controller also corrects any single-bit errors in memory.

ECC_Status The Error Correcting Code Status bits indicate the status of the ECC detect logic as follows:

- 00 = No error
- X1 = MED: Multi-bit error detect
- 1X = SED: Single-bit error detect

The ECC status bits and corresponding failing chip-select indicators (see bits below) are set by the first error detected of each type (SED or MED). The AMD-761 system controller does not log any new errors of each type or assert SERR# until software clears the associated ECC_Status bit by writing a 1.

ECC_CS_MED The Multiple Bit Error Chip Select status provides the binary encoded chip select for the first multiple-bit error detected by the AMD-761 system controller. The Failing ECC Chip Select is a binary encoded field and is valid only when the ECC_Status bits indicate a multi-bit error was detected.

ECC_CS_SED The Single-Bit Error Chip Select status provides the binary encoded chip select for the first single-bit error detected by the AMD-761 system controller. The Failing ECC Chip Select is a binary encoded field and is valid only when the ECC_Status bits indicate a single-bit error was detected.

3.8 Programmable Delay Lines (PDL)

This section describes the method used to create the delays necessary for proper DQS operation on the AMD-761 system controller DDR interface. The configuration registers used to control the delays are located in Device 0:Function 1. Note that for most systems, the BIOS should simply set the values recommended in Section 7 on page 211. The following sections provide a detailed description of the PDL operation and the options for BIOS configuration.

For memory reads, the DDR devices drive the DQS pins edge-aligned with the data, and the AMD-761 system controller must "adjust" the incoming DQS to capture the data. The adjusting of the incoming DQS requires delaying the DQS accordingly for each byte or nibble. Because this timing is very tight, the

AMD-761 system controller implements a Programmable Delay Line (PDL) to adjust the incoming DQS.

Each PDL is composed of a selectable buffer chain that is used to delay the incoming DQS strobe for placing the DQS within the valid data window. A separate PDL is implemented for each DQS pin (nine total in non-x4Mode) with additional PDLs (for a total of 18 in x4Mode) placed on the input of the data mask (DM) pins for use when accessing a x4 DIMM. The PDL is only used for read data capture. Because the propagation delay of an individual buffer of the PDL is a function of process, voltage and temperature (PVT), a mechanism is required to compensate for these three variables. This calibration mechanism determines the appropriate delay to apply across PVT. A calibration mechanism is placed near every two PDLs to accurately sense PVT near the actual PDLs used to delay the incoming DQS strobes. Each calibration mechanism is hand placed within the AMD-761 system controller to match gate for gate the actual PDL. This approach minimizes error between the calibration mechanism and the actual PDLs.

The range of each PDL is from 1 ns to 2.5 ns (worst case). The resolution of the PDL is equal to one buffer delay inside the AMD-761 system controller. That is, the value in the PDL register that controls the “tap” point of the PDL delay chain represents the number of internal buffer propagation delays. Because the propagation delay of an internal buffer can vary over PVT, the number of buffers (and therefore the value in the PDL control register) can be different at different times (and different across the same AMD-761 system controller device or even different across selected AMD-761 system controller devices), but it can still represent the same delay value in time units.

Board effects (signal skews, cross talk, etc.) are incorporated in the timing budget analysis, and they combine to reduce the effective data-valid window width presented to the AMD-761 system controller. The PDL hardware assumes that the effects are symmetric—that is, they shrink the setup and hold times equally. If this symmetry is not the case for the system, then the AMD-761 system controller allows the BIOS to compensate for these effects.

The internally delayed DQS (output of the PDL) is used inside the AMD-761 system controller to capture the corresponding

data byte (for x8 and x16 devices) or data nibble (for x4 devices) on a read cycle. The time value of the amount of delay to be applied to each DQS is fixed and is only dependent on the frequency of the system clock. Therefore, the DQS delay required is known *a priori* and is listed in Table 30. What is not known is how many internal buffer delays equal this required time value over PVT, which is the purpose of the PDL calibration mechanism.

Table 30. Default DQS Delay versus System Clock Frequency

System Clock Frequency	DQS Delay (ns)	DQS Delay (% of CCLK2X Period)
100 MHz	2.0500 ns	41.0%
133 MHz	1.5625 ns	41.7%

Because the propagation delay of an individual buffer internal to the AMD-761 system controller is a function of PVT, a mechanism is required to compensate for these three variables. As previously mentioned, the delay value is known, but the number of buffers that provides this delay value is not known for a given PVT point. The calibration mechanism provides this piece of information. The mechanism used is a simple measurement of how many buffer delays are required to equal the system clock period. Because the system clock is generated by a PLL in the AMD-761 system controller, and it is already compensated for PVT, the system clock period is independent of PVT. Therefore, the clock period can be assumed to be a constant and can be used to correlate the PDL values (Cal_Dly and Act_Dly) to units of time.

Each calibration mechanism inside the AMD-761 system controller measures the 2X SYSCLK period in buffer delays. This measurement can take a few hundred clock cycles, therefore it is done off-line. The calibration mechanism computes a Cal_Dly value that is then transferred into the PDL control register (Act_Dly) at a time when the DQS pins are not active as inputs.

The calibration is automatically performed once after reset and once after self-refresh exit, and the resultant value is transferred to each PDL. Re-calibration can be initiated via software. The AMD-761 system controller also has a mode that enables periodic auto calibration.

Periodic auto-calibration mode re-computes the Cal_Dly values and transfers this value into the PDLs. All nine (or 18) calibration mechanisms are enabled/disabled together for auto-calibration. This mode is useful in adjusting the delay values during operation. In effect, auto-calibration can adjust for voltage and temperature (VT) drifts during operation. Note that the AMD-761 system controller also allows re-calibration to occur completely under software control when this (auto-calibration) mode is disabled.

The auto-calibration period is configurable, and the possible periods are 10000, 1000000, 10000000 clock cycles (at 100 MHz, these periods are equal to 100 μs, 10 ms, and 100 ms, while at 133 MHz it is somewhat faster). The setting of the auto-calibration period should be based on the actual characteristics of the system.

Software can control when calibration is done (except for the first computation at reset or an exit from self-refresh). It can either configure the AMD-761 system controller for auto-calibration (via the Auto_Cal_En bit), or it can initiate a single recomputation (via the SW_ReCal bit). If software initiates a single recomputation (via the SW_Recal bit), it should also poll for this computation to be done.

Because auto-calibration registers are not initialized at reset, it is the responsibility of the BIOS to initialize the SW_Cal_Dly. The SW_Cal_Dly value that BIOS provides is based on a value provided after AMD-761 silicon characterization. The hardware computes the Cal_Dly value that is applied to the PDL based on the SW_Cal_Dly programmed. The SW_Cal_Dly bits are used by AMD-761 system controller to update the delay times in both auto-calibration mode as well as software-initiated calibrations. For example, if the delay required is 1.7 ns and the system clock frequency is 133 MHz, the following is the derivation of the SW_Cal_Dly value:

- The half-period of system clock = 3.75 ns.
- 1.7 ns = 45.33% of the half-period.
- The SW_Cal_Dly value is 0.4533 x 256 = 116 (rounded to nearest integer) = 0x74.

The AMD-761 system controller allows software to optionally write to the Act_Dly bits that control each PDL. The value written to the Act_Dly bits is the number of buffer delays

required (rather than a percentage of the clock period). To determine the number of buffer delays, software must first read the Clk_Dly bits and scale this value for the required Act_Dly. For example, if Clk_Dly is 75 buffer delays at 100 MHz, and the BIOS desires a delay of 2.1 ns, the following is the derivation of the Act_Dly value:

- 75 buffer delays = half-period of system clock = 5 ns
- 2.1 ns = 2.1 / 5 x 75 = 31.5 buffer delays
- The Act_Dly value is either 31 or 32 (depending on rounding desired) = 0x1F or 0x20.

The AMD-761 system controller provides a configuration bit (Act_Dly_Inh) that inhibits the auto calibration state machine from updating the Act_Dly values after the computation of Clk_Dly and Cal_Dly is completed. If this mode is used, the PDLs (Act_Dly values) are not updated with new Cal_Dly values (whether auto-calibration is enabled or whether software initiates a re-calibration). However, the PDLs are always updated at reset. Upon exit from self-refresh, the Act_Dly_Inh bit determines whether the PDLs are updated or not. This feature can be useful for diagnostic purposes.

SW_Recal

The Software Re-calibration bit (Dev 0:F1:0x40, bit [7]) provides a way for software to force a re-calibration cycle. This action is allowed only when the auto calibration feature is **disabled**. A re-calibration is forced when this bit is written to a 1b. This bit also provides status by being cleared when the calibration has completed. BIOS may find it useful to be aware of the completion of the calibration, although from a functional perspective, the DDR memory controller does not require it. When the re-calibration is complete, the hardware recomputes the Cal_Dly values for all PDLs, based on the values of their SW_Cal_Dly fields.

Use_Act_Dly

The Use Actual Delay bit (Dev 0:F1:0x40, bit [6]) provides a way for software to change the PDL setting manually, which is done by updating the Act_Dly field directly. BIOS should set this bit to indicate to the hardware that it has written to the Act_Dly fields and wants to update the PDLs (all 18) with the newly written Act_Dly values. This method should be used only when SW_Recal and Auto_Cal_En bits are not set. If Auto_Cal_En is set, writes to this bit are ignored.

Auto_Cal_En The Auto Calibration Enable bit (Dev 0:F1:0x40, bit [5]) provides a way for BIOS to enable the PDL auto calibration function. When this bit is set, all of the Cal_Dly values are recomputed periodically (according to the setting of the Auto_Cal_Period field) for all PDLs, based on the values of their SW_Cal_Dly fields. If the Act_Dly_Inh bit is not set, the Cal_Dly values are also applied to the Act_Dly.

Note: *Once Auto_Cal_En is set to 1, clearing it makes the bit a 0, but the auto-calibration logic may perform one more update, depending on when the Auto_Cal_En bit is cleared. Therefore, BIOS should at least wait for the amount of time specified by the Auto_Cal_Period field after clearing the Auto_Cal_En bit before attempting to change any of the PDL parameters.*

Note: *This bit should not be set if the system clock frequency is 66 MHz.*

Act_Dly_Inh The Actual Delay Update Inhibit bit (Dev 0:F1:0x40, bit [4]) provides a way for BIOS to inhibit an auto-calibration value from updating the PDLs. The setting of this bit affects both auto-calibration and software-initiated calibration but not the Use_Act_Dly method. After an exit from self-refresh, the setting of this bit determines whether the Act_Dly value is updated or not.

Note: *The internal logic tests this bit just prior to updating the Act_Dly, so the other bits in this register should be taken into consideration when writing to this bit.*

Auto_Cal_Period The Auto-Calibration Period (Dev 0:F1:0x40, bits [1:0]) bits specify how often an auto-calibration occurs. The auto-calibration periods are as follows:

- 00 = 10000 system clocks
- 01 = 1000000 system clocks
- 10 = 10000000 system clocks
- 11 = Reserved

BIOS should configure this field before setting the Auto_Cal_En bit. This field should not be altered while Auto_Cal_En is set.

Clk_Dly The auto-calibrator's Clock Delay (Dev 0:F1:0x44, bit [31:24] through Dev 0:F1:0x88, bits [31:24]) is read-only and provides

the number of PDL buffer delays required to make up a 2X SYSCLK period. This value is used to calculate the actual PDL value. The value returned from this field divided by the clock frequency is the average delay per tap of the PDL.

SW_Cal_Dly The auto-calibrator's Software Calibration Delay (Dev 0:F1:0x44, bits [23:16] through Dev 0:F1:0x88, bits [23:16]) provides BIOS access to the overall percentage of the buffers required, based on the total number of buffer delays shown in the Clk_Dly field. This value is used to calculate the actual PDL value. This value should be:

- 69h at 100 MHz (2.0500 ns 41.0%)
- 6Bh at 133 MHz (1.5625 ns 41.7%)

Cal_Dly The auto-calibrator's Calculated Delay (Dev 0:F1:0x44, bits [15:8] through Dev 0:F1:0x88, bits [15:8]) is read-only and provides the calculated delay based on the auto-calibrator's finding of Clk_Dly and the BIOS-specified SW_Cal_Dly. This value is the final calibration value that is used for the PDL if the Act_Dly_Inh bit (Dev 0:F1:0x40, bit [4]) is not set. If the Act_Dly_Inh bit is set, this calculated value is **not** used to update the PDLs.

Act_Dly The auto-calibrator's Actual Delay (Dev 0:F1:0x44, bits [7:0] through Dev 0:F1:0x88, bits [7:0]) directly specifies the number of PDL taps. BIOS can manually update the PDL by writing a PDL tap value into this register and writing a 1b to the Use Actual Delay bit (Dev 0:F1:0x40, bit [6]). This action should only be done when the auto-calibration logic is disabled by writing a 0b to (Dev 0:F1:0x40, bit [5]). Manually updating the PDL while the auto-calibration logic is enabled could result in unpredictable system operation.

3.8.1 Manual PDL Window Detection

The recommended value specified in the SW_Cal_Dly field (Dev 0:F1:0x44, bits [23:16] through Dev 0:F1:0x88, bits [23:16]) is based on calculated round trip timing assuming worst case AMD-761 system controller conditions, worst case DDR DIMM device conditions, and board routing. The most critical timing relationship during a DDR DIMM read is the round trip data delays and the DQS/data relationship relative to each other. Many factors affect the DQS/data relationship. Because of these factors, BIOS itself can determine a precise

SW_Cal_Dly value by performing a manual window detection rather than using the specified values.

Manual window detection can be accomplished with the following steps:

- Disable the PDL auto-calibration feature by setting Dev 0:F1:0x40, bit [5] = 1b0. Disabling auto-calibration prevents auto-calibration interference while BIOS manipulates this process manually.
- Determine the operating range of each PDL by adjusting each PDL tap from minimum to maximum to determine the data window range. This determination is accomplished by multiple iterative writes to alter the PDL and reading back "expect" data from DDR memory after each PDL tap is altered. For x8/x16 devices, this process is performed at the byte resolution. For x4 devices, this process is performed at the nibble resolution. The Actual Delay is adjusted via Dev 0:F1:0x44, bits [7:0] through Dev 0:F1:0x88, bits [7:0]. After the Actual Delay is configured, BIOS must write a 1b to the Use Actual Delay bit (Dev 0:F1:0x40, bit [6]) to apply the new Actual Delay value.
- Once the operational range for each byte (for x8/x16 devices) or for each nibble (for x4 devices) is determined, the center point for this window can be determined by dividing these ranges by two, which yields the “target window PDL tap.”
- The average PDL tap value must be determined for knowledge of the expected delay per tap of the PDL. This value can be retrieved by performing a software-initiated calibration. First set the Actual Delay Update Inhibit Dev 0:F1:0x40, bit [4] to a 1b to prevent a calibration update. Initiate a calibration by writing a 1b to Dev 0:F1:0x40, bit [7], and then polling this bit to become a 0b to determine when the calibration is complete. The total number of PDL taps that make up 5 ns (for 100-MHz operation) or 3.75 ns (for 133-MHz operation) can be found in the Clock Delay field for each calibrator in Dev 0:F1:0x44, bits [31:24], through Dev 0:F1:0x88, bits [31:24]. By dividing the appropriate period (as applies to the frequency of the AMD-761 system controller) by the values found in the Clock Delay fields yields the “average delay per PDL tap.”

- Once the appropriate PDL value is determined for each byte or nibble (as it applies), this value must be converted into a Software Calibration Delay value for the auto-calibration logic. This value can be calculated by multiplying the "target window PDL tap" (found above) by the "average delay per PDL tap," which yields the "required PDL tap delay" as a function of time (ns).
- The Software Calibration delay is specified as a percentage. Therefore, the Software Calibration delay = ((operating period/2) / required PDL tap delay) x 256). The value determined in this calculation must be applied to the Software Calibration Delay field Dev 0:F1:0x44, bits [23:16], through Dev 0:F1:0x88, bits [23:16].
- Clear the Actual Delay Update Inhibit Dev 0:F1:0x40, bit [4] to allow calibration updates and then enable the auto-calibration system by writing a 1b to Dev 0:F1:0x40, bit [5].

3.9 DDR I/O Drive Strength

The DDR I/O pads are SSTL-2 compatible. The DDR pads have configurable slew rate and drive strength control of N and P transistors, separately. It is the responsibility of BIOS to initialize the pad drive strength and slew rate before any memory accesses. The DDR I/O drive strength and slew controls exist at (Dev 0:F1:0x8C) through (Dev 0:F1:0x9B). Drive strength and slew control are provided for both the P and N transistors to allow for a fine adjustment for proper DDR SSTL-2 crossover points and rise/fall edge rates.

Separate drive strength and slew control is provided for the following:

- Data strobes (DQS)

Note: *If any chip select is configured to support a x4 DIMM, the DM buses inherit the drive strength and slew setting specified for the data strobes (DQS). Otherwise, the DM pins inherit the drive strength specified for the MDAT pins. This inheritance occurs because a x4 DIMM access uses the DM signals as data strobes (DQS) signals.*

- Data bus (MDAT), ECC bus (MECC), and data mask bus (DM) (See preceding note.)
- Device clock output (CLKOUTH/L)

Note: *The AMD-761 system controller provides differential clocks, CLKOUTH and CLKOUTL, for the DDR DIMMs. This single CLKOUT drive strength and slew setting applies for both polarities of CLKOUT.*

- Device Chip Select (CS[7:0]#)
- Command bus A (RASA#, CASA#, WEA#, and CKEA#)
- Command bus B (RASB#, CASB#, WEB#, and CKEB#)
- Memory address bus A (MAA[14:0])
- Memory address bus B (MAB[14:0])

Signal integrity studies have shown that P and N slew settings of 101b and a P drive strength setting of 11b and an N drive strength setting of 10b for **all** of the signal groups specified above provide adequate edge rates across various unbuffered and registered DIMM devices and population. A proper drive strength and slew setting for (Dev 0:F1:0x8C, bits [31:0]) is 0E_2D_0E_2Dh.

4 Power Management

This chapter provides the BIOS requirements for the AMD-761™ system controller's various power management states. The AMD-761 system controller includes logic specifically for the support of the following Advanced Configuration and Power Interface (ACPI) states:

- C2 Stop Grant (probed)
- S1 Power-On Suspend
- S3 Suspend to RAM

This chapter discusses the BIOS requirements for the AMD-761 system controller only, and does not include special requirements for the processor, Southbridge, or the operating system support of each power management state.

Note: *To accommodate the S3 state, some of the AMD-761 system controller register bits are not initialized to a known value at power-on with the RESET# signal. The BIOS must initialize all of these bits for proper operation, especially when enabling power management features as described in this section. BIOS must also perform a save and restore of all relevant configuration bits in the processor and chipset to support the Suspend to RAM feature.*

Table 31 on page 186 summarizes the various features required by the AMD-761 system controller to support the different power management states.

Note: *ACPI C3 state is not supported by the* AMD-761 system controller*, and the BIOS must not declare C3 support to the operating system through the Fixed ACPI Description Table.*

The BIOS should declare the following values:

- A value of 0 in the PM2_CNT_BLK field in the Fixed ACPI Description Table (FADT)
- A value of 0 in the PM2_CNT_LEN field of the FADT
- A value of 0 in the X_PM2_CNT_BLK field of the FADT if this ACPI 2.0 extension is supported by the operating system.

Table 31. AMD-761™ System Controller Power Management Features for ACPI Support

AMD-761 system controller Power Management Feature	ACPI State			
	C1	C2	S1	S3
Disconnect processor when Halt special cycle is detected on AMD Athlon™ system bus. ■ Enabled by BIU Status/Control (Dev 0:F0:0x60, bit 18)	X			
Disconnect processor when Stop Grant special cycle is detected on AMD Athlon™ processor system bus. ■ Enabled by BIU Status/Control (Dev 0:F0:0x60, bit 17 for CPU 0)		X	X	X
Memory controller forces DRAM to self-refresh mode ■ Enabled by BIU Status/Control (Dev 0:F0:0x60) and Mode/Status Register (Dev 0:F0:0x70, bit 18)		X	X	X
DCSTOP# assertion by Southbridge causes AMD-761 system controller to gate off clock trees and DRAM clocks for lower power ■ Enabled when the Stp_Grant_Discon_En bit is set in the BIU Status/Control Register (Dev 0:F0:0x60, bit 17).			X	X
RESET# assertion in S3 state causes AMD-761 system controller to gate off I/O rings so power can be removed from AGP, PCI, and processor interfaces while VDD_CORE and DDR interface remains powered. ■ Enabled when the Stp_Grant_Discon_En bit is set in the BIU Status/Control Register (Dev 0:F0:0x60, bit 17).				X

Each of the various power management features may be optionally enabled with specific configuration bits in the AMD-761 system controller's host bridge configuration space as described in the following sections.

4.1 C1 Halt State Requirements

The processor enters the C1 Halt state after executing a Halt instruction and generating a Halt special cycle on the AMD Athlon™ system bus. The AMD-761 system controller supports two options for the Halt state:

1. Forward the Halt special cycle to the PCI bus but otherwise continue normal operation (no power savings).
2. Disconnect the processor and then forward the Halt special cycle to the PCI bus (processor enters very low-power state).

The first option is the recommended mode and requires no special setup in the AMD-761 system controller other than to write a 0 to the Halt_Discon_En bit in the BIU Status/Control register (Dev 0:F0:0x60, bit 18). This action causes the AMD-761 system controller to react to the Halt special cycle on the AMD Athlon system bus by forwarding the cycle to the PCI bus but not attempting any processor disconnect. There is no significant power savings in this mode.

The second option requires that the Halt_Discon_En bit be set, which forces the AMD-761 system controller to initiate a processor disconnect for lower power using the PROCRDY/CONNECT protocol on the AMD Athlon™ system bus. The PCI and AGP arbitration remains enabled in this state, thus any DMA cycles that require a probe of the processor's cache causes the AMD-761 system controller to reconnect using the PROCRDY/CONNECT protocol. There is some additional latency imposed when this mode is enabled, because each processor probe requires a reconnect of the CPU. When the AMD Athlon system bus is disconnected, the processor enters a very low-power state.

The AMD-766™ peripheral bus controller Southbridge does not require any special initialization for either of the above two modes.

4.2 C2 Stop Grant State Requirements

The processor enters the C2 Stop Grant state and issues a Stop Grant special cycle on the AMD Athlon processor system bus in response to the assertion of the STPCLK# input signal by the Southbridge. The AMD-761 system controller supports two options for the Stop Grant state:

1. Wait for a Stop Grant Special Cycle from both installed processors and fForward the Stop Grant special cycle to the PCI bus, but otherwise continue normal operation (no significant processor power savings).
2. Disconnect the processor, enter self-refresh, and then forward the Stop Grant special cycle to the PCI bus. This power management state provides a lower power clock

controlled state that allows snooping of the processor cache. If the AMD Athlon processor system bus is disconnected, the processor enters a very low-power state.

The first option requires no special setup in the AMD-761 system controller other than to write a 0 to the Stp_Grant_Discon_En bit in the BIU Status/Control register (Dev 0:F0:0x60, bit 17). This action causes the AMD-761 system controller to react to the Stop Grant special cycle on the AMD Athlon processor system bus simply by forwarding the cycle to the PCI bus, but not attempting any processor disconnect. No significant power savings occur in this mode. When this option is selected, the BIOS should not declare support for the C2 state in the Fixed ACPI Description Table.

The second option requires that the following AMD-761 system controller configuration bits be initialized:

- The Stp_Grant_Discon_En must be set in the BIU Status/Control register. When this bit is set, the AMD-761 system controller flushes internal queues after receiving the Stop Grant special cycle, force the DDR DRAM into self-refresh mode, and forward the Stop Grant special cycle to the PCI bus to the Southbridge.
- DRAM refresh must be enabled by writing a 0 to the Ref_Dis test bit in the DRAM Mode/Status register (Dev 0:F0:0x58, bit 19).
- Self-refresh must be enabled by writing a 1 to the Self_Ref_En bit in the Status/Control register (Dev 0:F0:0x70, bit 18).

DMA cycles initiated from the PCI bus or AGP interface's PCI bus can be probed in the C2 state. When a cacheable access is initiated on these interfaces, the AMD-761 system controller initiates a connect sequence on the AMD Athlon system bus via the PROCRDY/CONNECT protocol.

This mode requires specific configuration registers in the to be initialized for proper generation of the STPCLK# signal and resume events.

4.3 S1 Power-On Suspend State Requirements

The ACPI S1 state uses the Southbridge DCSTOP# signal to gate off the AMD-761 system controller's internal clock trees for a very low-power state. All voltages remain powered on in this mode.

To the AMD-761 system controller, the configuration register initialization required for S1 support is the same as that required for C2 support as described in Section 4.1 on page 186. The AMD-761 system controller requires the following BIOS/drivers for S1 support:

- The Stp_Grant_Discon_En must be set in the BIU Status/Control register. When this bit is set, the AMD-761 system controller flushes internal queues after receiving the Stop Grant special cycle, forces the DDR DRAM into self-refresh mode, and forwards the Stop Grant special cycle to the PCI bus to the Southbridge.
- DRAM refresh must be enabled by writing a 0 to the Ref_Dis test bit in the DRAM Mode/Status register (Dev 0:F0:0x58, bit 19).
- Self-refresh must be enabled by writing a 1 to the Self_Ref_En bit in the Status/Control register (Dev 0:F0:0x70, bit 18).
- To ensure that no probes are generated, all PCI/AGP traffic must be prevented by the peripheral software drivers before entering the S1 state when DCSTOP# is asserted. It is expected that the drivers have already placed each PCI/AGP peripheral into the D3 state prior to STPCLK# assertion by the Southbridge.

The S1 state is supported by the AMD-761 system controller for both unbuffered and registered DDR DIMMs. However, when registered DIMMs are installed in the system (according to the Reg_DIMM_En bit in the DRAM Timing register in Dev 0:F0:0x54), the DRAM clocks (CLKOUT[5:0], CLKOUT[5:0]#) continue to be driven active. This action is required because the registered DIMMs do not support removal of the clock input unless in reset.

The S1 sleep state has a very low resume latency because the PLLs are already running. The AMD-761 system controller

simply enables its clock trees and reconnects the processor. Because no power is removed from the system, and the RESET# signal is not asserted, all AMD-761 system controller configuration registers retain their original value prior to entering the S1 state.

The S1 sleep state requires specific configuration registers in the AMD-768 peripheral bus controller or AMD-766 peripheral bus controller to be initialized for proper generation of the STPCLK# and DCSTOP# signals and resume events.

4.4 S3 Suspend to RAM State Requirements

The ACPI S3 state achieves maximum power savings and low-latency resume by shutting off most system power supplies while retaining system context in DRAM. This action requires that the AMD-761 system controller core voltage remain powered on along with the DRAM and part of the Southbridge, while the remaining platform components are powered off.

For any system enabling the S3 state, a number of core logic PCI configuration registers and processor MSRs must be saved or restored prior to suspending or restoring S3. Also, certain hidden bits must be unmasked. These requirements apply to all platforms regardless of segment and whether or not AMD PowerNow!™ is used.

To the AMD-761 system controller, the configuration register initialization required for S3 support is the same as that required for S1 support. The AMD-761 system controller requires the following of the BIOS/drivers for S3 support:

- The Stp_Grant_Discon_En must be set in the BIU Status/Control register. When this bit is set, the AMD-761 system controller flushes internal queues after receiving the Stop Grant special cycle, force the DDR DRAM into self-refresh mode, and forward the Stop Grant special cycle to the PCI bus to the Southbridge.
- DRAM refresh must be enabled by writing a 0 to the Ref_Dis test bit in the DRAM Mode/Status register (Dev 0:F0:0x58, bit 19).

- Self-refresh must be enabled by writing a 1 to the Self_Ref_En bit in the Status/Control register (Dev 0:F0:0x70, bit 18).
- To ensure that no probes are generated, all PCI/AGP traffic must be prevented by the peripheral software drivers before entering the S3 state when DCSTOP# is asserted. It is expected that the drivers have already placed each PCI/AGP peripheral into the D3 state prior to STPCLK# assertion by the Southbridge.
- The Suspend to RAM control bits (STR_Control[1:0]) in the DRAM Mode/Status register (Dev 0:F0:0x58) must be properly controlled by BIOS to force the AMD-761 system controller to properly enter and exit the S3 state. Refer to Section 4.4.1 on page 191 for details.

To accommodate S3 support, the AMD-761 system controller does not initialize most of the memory controller configuration registers to a known value when RESET# is asserted. It is important that these registers be properly initialized by BIOS during the power-up configuration. Once initialized, the AMD-761 system controller retains these values when resuming from the S3 state.

4.4.1 STR Bit Control for S3 Support

The STR_Control bits are provided to allow BIOS to communicate state changes to the AMD-761 system controller's power management logic. Proper control of these bits is required to ensure that the correct sequence is followed when the AMD-761 system controller is entering and exiting the Suspend to RAM state.

Each of the three STR_Control modes are described below.

Power-On Reset (00) The AMD-761 system controller always sets the STR_Control bits to this value when the RESET# pin is asserted—that is, when powering up from the S3, S4, S5, and Mechanical Off states). The AMD-761 system controller memory controller always drives the DRAM CKE pins Low in this state, forcing the DRAMs inactive, and the memory controller configuration registers retain the values they had prior to the RESET# assertion.

Normal Resume (01) BIOS should write this value to the STR_Control bits when resuming from the S4 (Suspend to Disk), S5 (Soft Off), or Mechanical Off states. This action forces the AMD-761 memory controller to follow the normal DRAM initialization sequence as follows:

- Assert CKE pins to enable clocks at the DRAM DIMMs
- Perform required DRAM initialization sequence, including writes to DRAM mode registers, etc.

The BIOS should then follow the normal initialization sequence in this mode, including DRAM configuration and memory sizing, etc.

After a hard reset, BIOS should set these bits to 01b and bit 25 of this register (DRAM Init) to a 1b within the same configuration write. If this register is not set to a 01b, setting bit 25 of this register has no effect. This pattern is written by BIOS to inform the AMD-761 system controller memory controller that this is a power-on reset rather than a Suspend To RAM wakeup from reset.

Resume from S3 (1X) BIOS should write this value to the STR_Control bits when resuming from the S3 (Suspend to RAM) state. This action instructs the AMD-761 system controller memory controller to perform the proper DDR protocol to exit self-refresh but not attempt to re-initialize the DDR DRAM devices—that is, mode register writes, etc.). Note that this bit is ignored by the memory controller after it exits self-refresh, until the bit is cleared by RESET#. Problems are thus avoided when the AMD-761 system controller periodically enters and exits self-refresh for C2, S1 and clock throttling.

As shown in Figure 5 on page 193, when BIOS writes a 1X to the STR_Control field upon exiting the S3 state, the AMD-761 system controller simply takes the DRAM out of self-refresh mode. At this time all of the AMD-761 memory controller configuration registers retain their original values programmed prior to entry to the S3 state, thus allowing BIOS immediate access to memory for the restoration of all other system configuration registers and context restoration. Refer to Section 1.1.3 on page 4 for a list of the AMD-761 system controller configuration registers that are not set to a known value when the RESET# pin is asserted.

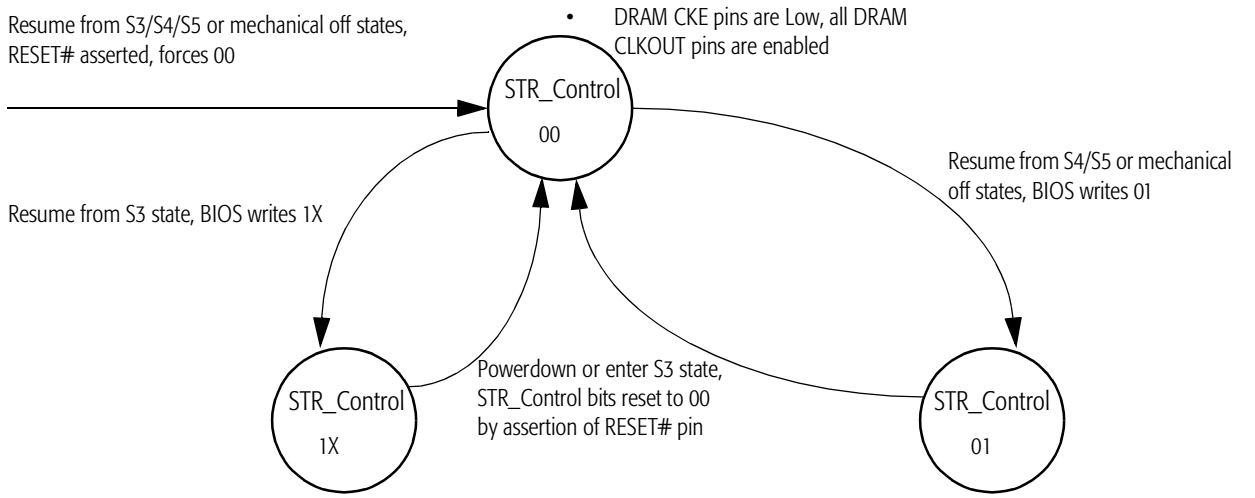

Figure 5. Suspend to RAM (STR_Control) Bits Usage

4.5 Clock Throttling

Clock throttling is a power management mechanism that periodically causes the assertion of the STPCLK# signal to the processor to achieve lower system power. Clock throttling can be accomplished through a combination of hardware and software and can be performed at regular intervals—that is, modulating the STPCLK# pin or through a more sophisticated system such as implementing thermal sensors on the motherboard.

The AMD-761 system controller supports clock throttling with the same hardware mechanisms that are used for C2 support and requires the following BIOS configuration register initialization.

- The Stp_Grant_Discon_En must be set in the BIU Status/Control register. When this bit is set, the AMD-761 system controller flushes internal queues after receiving the Stop Grant special cycle, forces the DDR DRAM into

self-refresh mode, and forwards the Stop Grant special cycle to the PCI bus to the Southbridge.

- DRAM refresh must be enabled by writing a 0 to the Ref_Dis test bit in the DRAM Mode/Status register (Dev 0:F0:0x58, bit 19).
- Self-refresh must be enabled by writing a 1 to the Self_Ref_En bit in the Status/Control register (Dev 0:F0:0x70, bit 18).

DMA cycles initiated from the PCI bus or AGP interface PCI bus can be probed while in the Stop Grant state during clock throttling. When a cacheable access is initiated on these interfaces, the AMD-761 system controller initiates a connect sequence on the AMD Athlon system bus via the PROCRDY/CONNECT protocol.

Note that when using clock throttling, the Southbridge must be programmed to wait for the Stop Grant special cycle before changing the state of the STPCLK# signal.

4.6 DDR DRAM Clock Enables

The AMD-761 system controller is designed to provide BIOS the ability to disable any unused DDR DRAM clock pairs to reduce power and system noise. These clock pairs are controlled by the Clk_Dis[5:0] field in the DRAM Mode/Status register (Dev 0:F0:0x58). The AMD-761 system controller provides six differential clock pairs to support up to two unbuffered DIMMs or four registered DIMMs. The usage of these clocks is motherboard-specific (i.e., which clock pairs connect to which DIMM clock inputs).

The Clk_Dis bits are initialized to 0 when RESET# is asserted, thus guaranteeing that all DRAM clock pairs are enabled when exiting the S3 state.

It is recommended that clock pairs that are connected to unused DIMM slots be disabled by BIOS. Note that because the values programmed by BIOS during power-on initialization are not maintained when entering the S3 state, BIOS is required to write to the Clk_Dis field when restoring the AMD-761 system controller configuration registers.

5 PCI Bus Interface

This chapter provides additional details of some of the AMD-761™ system controller PCI interface options that affect system performance and compliance to the *PCI Local Bus Specification*, Revision 2.2, as well as some recommended settings for the AMD-761 system controller configuration register bits.

The features and options discussed are as follows:

- PCI delayed transactions and target latency
- PCI transaction ordering
- Special arbitration options for Southbridges with legacy DMA requirements
- Performance enhancement options, including read prefetching and PCI chaining

5.1 Delayed Transactions and Ordering Rules Usage

The AMD-761 system controller provides three transaction operating modes for the PCI bus host bridge interface as listed in Table 32 on page 196. BIOS should program the bits listed in Table 32 to only one of these combinations for best results.

Table 32. AMD-761™ Processor System Controller PCI Read Transaction Options

PCI_DT_En Dev 0:F0:0x4C, bit 2	PCI_OR_En Dev 0:F0:0x4C, bit 1	Tgt_Latency Dev 0:F0:0x84, bit 23	Description
0 Disabled	0 Disabled	0 Disabled	No PCI transaction ordering or target latency rules are enforced. Delayed transactions are disabled, but masters are not retried by the AMD-761™ system controller during memory reads (unless the PCI_WR_Post_Rty bit is set in the PCI Arbitration Register at Dev 0:F0:0x84). This mode is not fully PCI 2.2-compliant because the AMD-761 system controller host bridge may consume greater than 32 PCI bus clocks during memory read transactions, and transaction ordering is not strictly enforced.
1 Enabled	0 Disabled	1 Enabled	Delayed transactions are enabled and target latency rules are enforced. This mode is not fully PCI 2.2-compliant because transaction ordering rules are not strictly enforced.
1 Enabled	1 Enabled	1 Enabled	Delayed transactions are enabled, target latency and transaction ordering rules are enforced. This mode provides full PCI 2.2-compliance.

The effects of the settings described in Table 32 above are described further in the following sections.

5.1.1 Delayed Transactions and Target Latency

Delayed transactions and read target latency should be enabled and disabled together in the AMD-761 system controller, such that both bits are either set or cleared.

- Setting the read target latency bit (Tgt_Latency) forces the AMD-761 system controller to disconnect the current PCI memory read cycle in progress when the defined maximum allowable latency has expired. This latency is defined in the *PCI Local Bus Specification*, Revision 2.2, as 16 PCI clocks (32 PCI clocks for host bridges that must snoop processor caches). When the read target latency is reached, the AMD-761 system controller asserts the STOP# signal, thus disconnecting the PCI master (retry). The master is then obligated by protocol to retry the same cycle after re-arbitration, in anticipation that the read has completed in the memory subsystem, thus the next read cycle falls within the maximum target latency.
- Setting the delayed transaction enable (PCI_DT_En) causes the AMD-761 system controller to latch the address and read command that was initiated by the external master

when the read target latency timer expires, thus allowing the PCI target and memory controller logic to independently complete the read so that the next time the original master retries the read, the data is ready to return immediately (assumes the PCI_WR_Post_Rty bit is not set in the PCI Arbitration Register (Dev 0:F0:0x84, bit 14).

There are two reasons delayed transactions may be enabled:

1. For systems that **must** meet the target latency requirement, delayed transactions are better because the memory read cycle is queued in the AMD-761 system controller memory controller after the PCI master is disconnected and while it is re-arbitrating for the PCI bus. This action provides a higher likelihood that when the master retries the transaction, the read data is immediately available.
2. Delayed transactions free up the PCI bus during the time that the memory subsystem is retrieving the read data, for peer-to-peer PCI traffic between other PCI masters and agents. Unfortunately, this type of traffic is rare in most systems.

It should be noted that the AMD-761 system controller supports only a single-level delayed transaction queue, thus the performance benefit may be minimal and may actually be worse with delayed transactions enabled under some conditions.

The following sections provide examples of PCI read transactions with delayed transactions enabled and disabled. Note that in both examples the read target latency feature enable is set the same as the delayed transaction feature enable.

Delayed Transactions and Target Latency Disabled

This example assumes that a memory read transaction is initiated by a PCI master and that the AMD-761™ system controller is unable to return data within the specified 32 PCI clock latency.

1. The AMD-761 system controller initiates a memory read to the memory controller and simultaneously issues a probe to the processor. The memory subsystem is unable to return the data within 32 PCI clocks, so it continues to hold the bus (DEVSEL# active, STOP#, and TRDY# inactive).

2. A second PCI master requests the bus to access main memory, and it receives a bus grant from the AMD-761 system controller PCI arbiter, but it must wait until the memory read cycle initiated by the previous master is completed. If this master's cycle was targeted to another PCI agent, it still could not begin the transaction because the bus is tied up by the previous master and the AMD-761 system controller.
3. Some number of PCI clocks later, the memory subsystem returns read data to the master completing the transaction. The bus goes idle, so the next master begins its transaction.

Delayed Transactions and Target Latency Enabled

This example assumes that a memory read transaction is initiated by a PCI master and that the AMD-761 system controller is unable to return data within the specified 32 PCI clock latency.

1. The AMD-761 system controller latches the memory read command and the address, and initiates a memory read to the memory controller and simultaneously issues a probe to the processor. The memory subsystem is unable to return the data within 32 PCI clocks, so it asserts the STOP# signal while TRDY# remains inactive. This action causes the master that originated the cycle to disconnect, and it must re-arbitrate for the bus. Meanwhile, the AMD-761 system controller memory controller continues to process the enqueued memory read transaction.
2. A second PCI master's bus request is now granted.
   - If the request is a read from main memory, the AMD-761 system controller retries the cycle but does not queue the transaction because it already has an outstanding delayed transaction in progress.
   - If the request is to a peer PCI agent, then the transaction can continue in parallel to the memory cycle being completed by the AMD-761 system controller.
3. The original master wins bus arbitration and retries its read command, and the AMD-761 system controller now responds with the read data within the specified maximum target read latency.

In summary, if compliance to the target latency rules is desired, then it is recommended that delayed transactions enable and the target latency bits are enabled.

5.1.2 Transaction Ordering Rules

The *PCI Local Bus Specification*, Revision 2.2, defines various transaction ordering rules to accommodate the producer-consumer model and to prevent deadlock conditions on the bus under certain conditions.

The AMD-761 system controller provides the ability to optionally disable strict adherence to the transaction ordering rules if desired. The ordering rules are defined such that data and its associated flags are visible by any agent on any segment of the PCI bus. In typical systems, however, this visibility is not necessary, as both data and flags typically reside in main system memory. It may be possible to achieve slightly better PCI bus performance when ordering rules compliance is disabled, because PCI masters attempting to read main memory are not disconnected to force the flushing of posted write FIFOs in the AMD-761 system controller.

Figure 6 on page 201 illustrates an example system implementation with data and associated flags stored in different locations. In this example, the flag is stored in main memory (DRAM) and the data is stored in the PCI agent.

The sections that follow describe the behavior in a system with and without ordering rules compliance.

With Ordering Rules Enabled

Using Figure 6 as an example, the following case describes the behavior of the AMD-761 system controller when ordering rules are followed.

1. The processor writes data (memory write) destined to an agent on the PCI bus, and the data is posted in the AMD-761 system controller PCI posting buffer.
2. The processor then sets a flag in memory, informing the PCI agent that the data is written.
3. The PCI master reads the flag, but this action causes the data previously written by the processor to be flushed from the AMD-761 system controller posted write buffer. The PCI master is disconnected by the AMD-761 system controller (STOP# active with TRDY# inactive) to allow the AMD-761 system controller to write the data to the PCI agent.

4. The PCI master regains bus ownership and attempts to read the flag again. This time it successfully reads the flag and the previously posted write data has already been written to the master's target interface.

It should be noted that this configuration is rare, as most systems place the data **and** the flag in main memory.

With Ordering Rules Disabled

Using Figure 6 as an example, the following case describes the behavior of the AMD-761 system controller when ordering rules are not followed.

1. The processor writes data (memory write) destined to an agent on the PCI bus, and the data is posted in the AMD-761 system controller PCI posting buffer.
2. The processor then sets a flag in memory, informing the PCI agent that the data is written.
3. The PCI master reads the flag, but the associated data (previously written by the processor) has not been flushed from the AMD-761 system controller posted write buffer. This situation results in a data incoherency.

Again, as in the case when ordering rules are enabled, note that this configuration is rare, as most systems place the data **and** the flag in main memory. The AMD-761 system controller provides the ordering rules feature for compliance to the *PCI Local Bus Specification*, Revision 2.2.

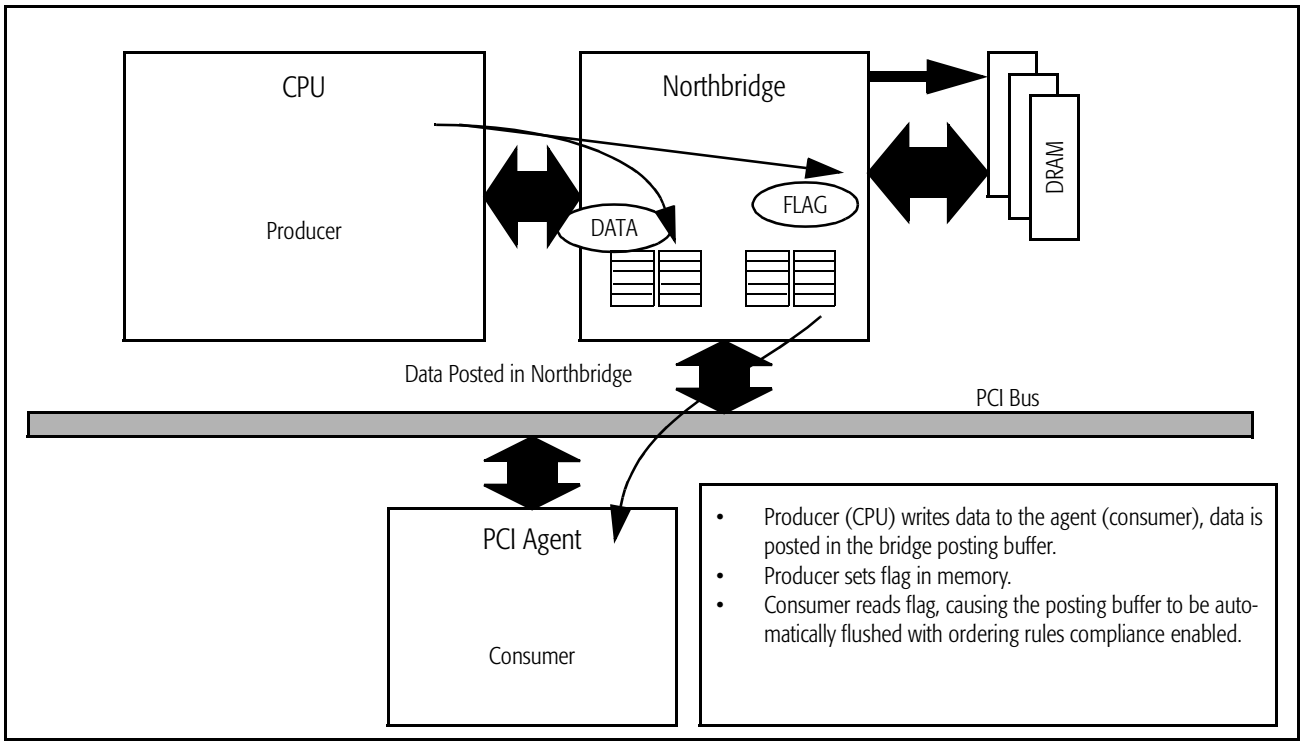

Figure 6. Example of System with Flag and Data Stored across PCI Bus Domain

5.1.3 Special Arbitration Considerations for the Southbridge

To accommodate legacy DMA as is supported in the AMD-766™ peripheral bus controller (the devices connected to the AMD-761 system controller's SBREQ# and SBGNT# pins), the AMD-761 system controller makes special exceptions in the arbitration for the Southbridge.

- The Southbridge is not preempted or disconnected when it gains access to the PCI bus as a master. This design prevents potential deadlock conditions that can occur with legacy DMA. There are no BIOS requirements to enable or disable this functionality.
- Before winning bus arbitration, the AMD-761 system controller's internal memory read and write queues can optionally be locked and flushed. This option is controlled by the SB_Lock_Dis bit in the PCI Arbitration Control register (Dev 0:F0:0x84, bit 8). This bit is cleared for normal operation.

By default, the AMD-761 system controller does not allow the SBREQ# PCI request to be preempted by requests on the normal REQ#[6:0] pins, and it does not disconnect the Southbridge once it has started a transfer.

5.2 PCI Performance Optimization Options

In addition to transaction level options as listed in Section 5.1 on page 195, the AMD-761 system controller PCI bus interface provides various system level options that can be used to tune the system performance. Each of these options are described in the following sections.

5.2.1 Read Prefetching

When the AMD-761 system controller is the target of PCI memory read accesses to system memory, the AMD-761 system controller's PCI target interface initiates a probe of the AMD Athlon™ processor's cache and a read of eight quadwords (a single cache line) from memory. Setting the read prefetching bit (PCI_Pref_En, Dev 0:F0:0x84, bit 1) causes the AMD-761 system controller to prefetch another eight quadwords from memory, speculating that the PCI master will request another cache line at the next cache-aligned address.

The obvious advantage to read prefetching is that masters that are reading multiple contiguous cache lines of data can stream this data more effectively on the PCI bus. The disadvantage is that it could result in wasted bandwidth of the memory subsystem of the prefetched data that is purged because it was not needed by the PCI master.

5.2.2 PCI Chaining

PCI chaining is a feature designed to optimize memory writes from the processor to the PCI bus. Chaining simply causes write combining at the PCI interface, such that four quadword CPU memory writes to contiguous addresses are chained together, resulting in a single PCI burst-write instead of separate nonburst writes.

PCI chaining is enabled by the PCI_Chain_En bit in the PCI Arbitration Control register (Dev 0:F0:0x84). It is recommended that this bit always be set for optimal performance.

5.2.3 PCI Bus Parking

The *PCI Local Bus Specification*, Revision 2.2, requires that a default bus owner be designated that always drives the bus to a known value to prevent the bus from floating for long idle periods. The AMD-761 system controller provides two options for bus parking:

- Park on the AMD-761 system controller—that is, CPU accesses to PCI agents
- Park on the last master that had bus tenure

Arbitration latency on an idle bus for the agent that has default ownership (bus is parked on that agent) is zero PCI clocks, whereas it is two PCI clocks for all other masters.

PCI bus parking is controlled by the Park_PCI bit in the PCI Arbitration Control register (Dev 0:F0:0x84). It is recommended that this bit be cleared to 0 to force parking the bus on the AMD-761 system controller.

6 AGP Interface

This chapter details some of the specific BIOS requirements for programming the AMD-761™ system controller's AGP interface.

6.1 AGP Dynamic Compensation Requirements

To accommodate the high-speed requirements of 4X AGP rates, the AMD-761 system controller provides circuitry designed to automatically compensate for motherboard impedance on the AGP interface over the range of temperature and voltage, by dynamically adjusting the drive strength of the AMD-761 system controller I/O pads when 1.5-V signalling is selected by the AGP card. This action requires proper initialization by BIOS as described in this section. Two separate 32-bit configuration registers are used to control AGP I/O characteristics:

1. AGP Dynamic Compensation register, Dev 0:F0:0xB4
2. AGP Compensation Bypass register, Dev 0:F0:0xB8

Two modes are provided in the AGP compensation circuitry:

- Automatically compensate once or at regular intervals by adjusting the drive strengths of the AGP interface I/O cells. In this case, BIOS is not required to program the drive strength values.
- Bypass the compensation and allow BIOS to write drive strength values directly to the I/O cells.

The AMD-761 system controller allows the AGP strobe signals (ADSTB[1:0], ADSTB[1:0]#) to be controlled independently from all other AGP signals, including the ability to bypass compensation for one set of signals while the other set is compensated and vice-versa. The slew rate for the AGP interface pins is also programmable by BIOS but is not changed by the autocompensation logic.

Additional compensation details are provided in the following sections, and specific programming recommendations are listed in Section 6.3 on page 209.

6.1.1 The AGP 4X Dynamic Compensation Register

AGP compensation is controlled by the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4). This register contains additional fields that are not directly related to compensation but control various attributes of the AMD-761 system controller AGP interface. This section provides additional details about the fields related to compensation.

PVal, NVal

The PVal and NVal are read-only fields that can be used to determine the drive strength values being automatically written to the AGP I/O pads by the compensation logic. These apply only to the signals used for data transfer and status/control—that is, not the AGP strobes. Typically the values read back allow BIOS to determine if the correct compensation resistors are installed on the motherboard.

Quantum_Cnt, Always_Compensate

These fields are used to enable 1.5-V signalling compensation at regular intervals, which is the suggested method for all 4X AGP non-strobe signals. The Quantum_Cnt field can be programmed for the maximum value (6.4 seconds), because it is not expected that a more frequent adjustment is required. The compensation is scheduled by the AMD-761 system controller such that changing the drive strength values does not interfere with AGP traffic.

If compensation bypass is selected for both the data transfer and strobe pins (both the BYPXfer and BYPStrb bits are set in the Compensation Bypass register) then these fields are ignored.

Do_Compensate, Comp3.3

These bits can be used in two cases:

- To force a normal, single compensation cycle in 1.5-V signalling mode to update the AGP I/O drive strengths, and to prevent any further updates. In this case, the Do_Compensate bit may be set (Comp3.3 should be cleared), and the AGP interface must not be enabled until this bit is read back as a 0, indicating that the compensation cycle is complete.

- To force a single compensation cycle in 3.3-V signalling mode (typically used for debug only). In this case, both the Do_Compensate and the Comp3.3 bits should be set, and the AGP interface must not be enabled until this bit is read back as a 0, indicating that the compensation cycle is complete.

If compensation bypass is selected for both the data transfer and strobe pins (both the BYPXfer and BYPStrb bits are set in the Compensation Bypass register) then these fields are ignored.

6.1.2 Selection of 1.5- or 3.3-V AGP Signalling

The selection of the AGP signalling type (1.5 V versus 3.3 V) is done by the AGP card via the TYPEDET# pin when it is installed in the AGP slot. AGP cards operating in 3.3-V signalling mode have their TYPDET# pin unconnected. Cards operating in 1.5-V signalling mode have the pin connected to VSS, forcing it to 0. The AMD-761 system controller latches the value of the TYPEDET# pin at reset, and BIOS can read this value in the Configuration Status register (Dev 0:F0:0x88, bit 25). The allowable rates at each signalling level are shown in Table 33 as listed in the *Accelerated Graphics Port Interface Specification*, Revision 2.0.

Table 33. Allowable AGP Rate versus Signalling Level

AGP Rate	1.5-V Signalling	3.3-V Signalling
1X	Supported	Supported
2X	Supported	Supported
4X	Supported	Not Supported

Section 6.3 on page 209 describes the recommended initialization sequence for reading this value and configuring various AMD-761 system controller parameters accordingly.

6.2 Feature Override Bits for AGP Cards

The AMD-761 system controller supports 1X, 2X, and 4X AGP rates as well as fast writes. The capability to support these features is normally reported to the operating system via the AGP Status register (Dev 0:F0:0xA4) as defined by the *Accelerated Graphics Port Interface Specification*, Revision 2.0. The operating system is thus able to determine and select the highest rate supported by both the AGP card and the AMD-761 system controller.

The AGP interface of the AMD-761 system controller includes two configuration bits that can be used to override the AGP Status register and to prevent reporting 4X and fast write capability. These bits are required to allow operation with AGP cards that operate with 3.3-V signalling, but still report 4X capability to the operating system. The problem thus created is because the operating system attempts to place the card and the AMD-761 system controller into 4X mode, but this speed is not supported when 3.3-V signalling is selected. The solution is for the AMD-761 system controller to report capability of a maximum of 2X AGP speed in this configuration.

The two override bits are described below, and specific programming recommendations are listed in Section 6.3.

4X_Override This bit is used to force the 4X rate bit to 0 in the AGP Status register (Dev 0:F0:0xA4, bit 2). After reset, the rate field in the AGP Status register is set to all 1s, indicating support for a maximum of 4X AGP speed. Setting the 4X_Override bit automatically forces this field to 011, indicating a maximum of 2X support. This override mechanism is required because the AGP Status register is defined as a read-only register in the AGP specification.

FW_Enable This bit indirectly enables fast write support in the AMD-761 system controller. Fast write support is reported to the operating system through the AGP Status register as described above for the rate field, but the FW status bit in the AGP Status register defaults to 0 (not supported) in the AMD-761 system controller. The FW_Enable bit should be set if this feature is desired.

Section 6.3 provides guidelines for setting these bits.

6.3 BIOS Initialization Requirements

This section lists the steps in an algorithm recommended to properly configure the AMD-761 system controller AGP fast write and rate features, as well as the compensation and slew rate values.

This BIOS algorithm must properly detect the AGP card's signalling type (1.5 V or 3.3 V) and enable the appropriate features as listed in the steps below. Note that these steps are require **before** the AGP interface is enabled.

1. Detect the signalling level (1.5 V or 3.3 V) by reading the value of the TYPEDET# pin that was latched by the AMD-761 system controller at reset. This value can be read in the Configuration Status register, Dev 0:F0:0x88, bit 25.
   - If 0, then 1.5-V signalling is selected by the AGP card. If 1, then 3.3-V signalling is used.
2. Configure the override bits according to the signalling level as listed in Table 34 on page 210 and the following notes.
   - If 1.5 V, then the 4X_Override bit should be cleared, and the FW_Enable bit should be set in the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4, bits 6 and 7, respectively). This action causes the AGP Status register (Dev 0:F0:0xA4) to report 4X and fast write capability to the operating system.
   - If 3.3 V, then the 4X_Override bit should be set, and the FW_Enable bit should be cleared in the AGP 4X Dynamic Compensation register (Dev 0:F0:0xB4, bits 6 and 7, respectively). This action causes the AGP Status register (Dev 0:F0:0xA4) to report a maximum rate of 2X, and no fast write capability to the operating system.
3. Program the appropriate compensation, drive strength, bypass, and slew rates to the AGP I/O pads in the AGP 4X Dynamic Compensation and AGP Compensation Bypass register according to Table 34 below.

Table 34. AGP I/O Settings for 1.5- and 3.3-V Signalling

Register	Bit/Field Name	Bits	1.5-V Value TYPEDET# = 0	3.3-V Value TYPEDET# = 1
Dev 0:F0:0xB4	FW_Enable	[7]	1	0
	4X_Override	[6]	0	1
	Comp3.3	[5]	0	0
	PCI	[2]	0	0
	Always_Compensate	[1]	1	0
	Do_Compensate	[0]	0	0
Dev 0:F0:0xB8	BYP_PDrvXfer	[31:28]	Don't Care	Don't Care
	BYP_NDrvXfer	[27:24]	Don't Care	Don't Care
	BYPXfer	[23]	0	0
	PSlewXfer	[19:18]	11	11
	NSlewXfer	[17:16]	11	11
	BYP_PDrvStrb	[15:12]	1111	Don't Care
	BYP_NDrvStrb	[11:8]	1111	Don't Care
	BYPStrb	[7]	1	0
	PSlewStrb	[3:2]	11	11
	NSlewStrb	[1:0]	11	11

6.4 AGP Miniport Driver Requirements

AMD has found that some early generation 4x AGP cards were not consistently implemented using published 4x AGP guidelines for AGP signal impedance and routing. These AGP cards do not work reliably with the default AGP drive-strengths of the AMD-761 system controller. As a result, AMD has developed a mini-port solution to adjust the AMD-761 system controller AGP drive strengths to the optimal levels for these early generation AGP cards as identified by the vendor and device ID in PCI configuration space. AMD does not plan for any current or future generation AGP cards to experience any incompatibilities with the AMD-761 system controller. If a card is identified that requires a drive strength change, the AMD mini-port or the AGP card is updated to allow compatibility.

7 Recommended BIOS Settings

This chapter provides the recommended BIOS settings for the initialization of some of the key AMD-761™ system controller configuration registers.

Registers that change based on the system implementation, such as memory space and sizing, AGP GART region, DDR DIMM timing, etc., are not included here because they are very platform-specific.

The following notes apply to the recommended settings tables in this section:

- All items keyed as BOLD CAPITALS should be set or controlled by BIOS. This is **mandatory**. No setting can be assumed by default.
- Refer to the actual configuration register descriptions for details of each bit. These can be found in "AMD-761™ System Controller Programmer's Interface" on page 9 of this document.
- The final and precise definition of bits in the SPD of a DDR DIMM can be found in JEDEC reference materials and specifications.
- Values that are shown as *x..xh* or *x..xb* must be set by BIOS. Numerical Values shown with *h* or *b* are **preferred** settings.

For any system enabling the S3 state, a number of core logic PCI configuration registers and processor MSRs must be saved or restored prior to suspending or restoring S3. Also, certain hidden bits must be unmasked. These requirements apply to all platforms regardless of segment and whether or not AMD PowerNow!™ is used.

7.1 PCI Bus 0, Device 0, Function 0 Registers

PCI Bus 0, Device 0, contains configuration registers that are mostly specific to the AMD-761 system controller and its processor, DDR SDRAM, AGP, and PCI bus interfaces. The Bus 0, Device 0 space contains two separate functions as follows:

- Function 0 contains standard PCI configuration space, timing and arbitration control for each interface, and memory decode registers.
- Function 1 contains DDR drive strength control and calibration control for the programmable delay lines (PDLs) of the DRAM interface.

Registers ----- Bits	Register Bit Name	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x00h	**PCI ID**					
31:16	Device ID	700Eh		r		Single-processor DDR Northbridge
15:0	Vendor ID	1022h		r		AMD
0x0x0x04h	**PCI Command and Status**					
31	PERR	0b		r		Not supported
30	SERR Sent	yb		c		R/W/1C, from AMD-761™ system controller
29	Master ABRT	yb		u		R/W/1C, from bus master
28	Target ABRT	yb		u		R/W/1C, from bus master target
27	Target ABRTS Signaled	0b		r		Not supported
26:25	DEVSEL_Timing	01b		r		
24	Data_PERR	0b		r		
23	FastB2B	0b		r		
22	UDF	0b		r		
21	66M	0b		r		
20	Cap_Lst	1b		r		
19:10	Reserved	000h		r		
9	FBACK	0b				
8	SERR, System Error Enable	yb		u		0 = Disable, 1 = Enable
7	Step	0b		r		
6	PERR	0b		r		
5	VGA Palette Snoop	0b		r		
4	MWINV	0b		r		
3	SCYC	0b		r		
2	MSTR	1b		r		
1	MEM	1b		B		PCI memory access enable
0	IO	0b		r		IO access disable on PCI bus
0x0x0x08h	**PCI Rev ID and Class Code**					
31:24	Class Code	06h		r		Bridge device
23:16	Sub_Class Code	00h		r		Host/PCI bridge
15:8	Prog. I/F	00h		r		Host/PCI bridge
7:0	Revision ID	1yh		r		Rev B1 = 11h, B2=12h, B3=13h

KEY:

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A= AGP setup by BIOS
o = Setup by OS or OS driver
u = PCI operational user interface
c = Calculated/set by AMD-761™ internal logic
F = Performance enhancement set by BIOS
E = Elective BIOS function

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x0Ch	**PCI Latency Timer and Header Type**					
31:24	Reserved	00h		r		
23:16	Header_Type	00h		r		
15:8	Lat_Timer	20h		**B**		
7:0	Reserved	00h		r		
0x0x0x10h	**BAR0:AGP Virtual Address Space**					
31:25	AGP Base Address Register 0 GART AGP Aperture Address	xxxx_xxxb		**A**		
24:4	Base Address Low	0b00_000h		r		Always 0 = 32 Mbytes minimum
3	Flags BAR0 mem as Prefetchable	1b		r		PCI specification
2:1	BAR0 Type mem as 32 bits	00b		r		PCI specification
0	Flags BAR0 as MEMORY Address Space	0b		r		PCI specification
0x0x0x14h	**BAR1:GART Memory Mapped Register Base**					
31:12	GART Memory Mapped Base Address Register Settable portion of Address	xxxx_xh		**A**		
11:4	GART Memory Mapped Base Address Register Low, hardwired to force 4 Kbytes	00h		r		
3	BAR1 mem Prefetchable	1b		r		PCI specification
2:1	BAR1 Type mem as 32 bits	00b		r		PCI specification
0	Flags BAR1 as MEMORY	0b		r		PCI specification

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x34h	**AGP/PCI Capabilities Pointer**					
31:8	Reserved	000000h		r		
7:0	Capabilities Pointer	A0h		r		AGP function pointer First item in AGP capabilities list
0x0x0x44h	**Extended BIU Control**					
31:11	Reserved	000h		r		
10:8	P0_WrDataDly	yyyb		r		
7:4	Reserved	0b		r		
3	P0_2BitPF	1b		**B**		Must be set for AMD Athlon™ processor
2:0	Reserved	0b		**B**		Must be set by BIOS
0x0x0x48h	**ECC Mode/Status**					
31:16	Reserved	0000h		r		
15:14	SERR_Enable	xxb		**B**		00b = ECC/SERR Disabled 1xb = SERR on Multi_Bit Errors x1b = SERR on Single Bit Errors See SERR# 0x0x0x4[8]
13	Reserved	0b		r		
12	ECC_Diag	0b		**B**		0 = Disable, 1= Enable
11:10	ECC_Mode SPD # 11	xxb		**B**	SPD	00b = NO ECC or ECC Disabled 01b = Data Errors Reported 10b = Data Errors Corrected for Memory and PCI /AGP 11b = Data Errors Corrected and Memory Scrubbed
9:8	ECC_Status	00b		**B**		00b = No Error x1b =MED Multi Bit Error Detect 1xb =SED Single Bit Error Detect R/W/1C
7:4	ECC_CS_MED	yh		c		CS of first MED
3:0	ECC_CS_SED	yh		c		CS of first SED

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x4Ch	**PCI Control**					
31:04	Reserved	0000h		r		
4:3	Reserved	00b		**B**		Must be set by BIOS
2	PCI_DT_En	0b		**B**		0= Disable Delayed Transactions 1= Enable Delayed Transactions
1	PCI_OR_EN	0b		**B**		0= Disable Ordering Rules Compliance 1 = Enable PCI Ordering Rules Compliance
0	Func1_En	0b		**B**		1= Enable 0x0x1xRR Access
0x0x0x50h	**AMD Athlon™ System Bus Dynamic Compensation**					
31:24	Reserved	00h		r		
23:20	PVal	yh		c		P Transistor Value in Use
19:16	NVal	yh		c		N Transistor Value in Use
15:12	Byp_P	0h		**B**		P Transistor Value Used if Byp = 1
11:8	Byp_N	0h		**B**		N Transistor Value Used if Byp = 1
7:5	SlewCntl	011b		**B**		
4	Byp	0b		**B**		1 = Enable Byp_P and Byp_N
3:0	Reserved	0h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x54h	**SDRAM Timing**					
31	SPBWaitState	xb		**B**	FSB	0 @ 100-MHz FSB 1 @ 133-MHz FSB
30	AddrTiming_A SPD # 21	xb		**B**	SPD	0 @ Unbuffered DIMM 1 @ Registered DIMM
29	AddrTiming_B SPD # 21	xb		**B**	SPD	0 @ Unbuffered 1 @ Registered
28	RD_Wait_State	1b		**B**		Must = 1
27	Reg_DIMM_En SPD # 21	xb		**B**	SPD	0 @ Unbuffered DIMM 1 @ Registered DIMM
26	t_{WTR} = Write Data In to Read Command Delay	1b		**B**		0 = 1 Clock 1 = 2 Clocks
25:24	t_{WR} = Write Recovery Time	10b		**B**		00b=1 Clock, 01b=Reserved 10b=2 Clocks, 11b=3 Clocks
23	t_{RRD} = Active Bank A to Active Bank Command Delay SPD # 28	xb		**B**	SPD	0 = 2 Clocks 1 = 3 Clocks
22:19	Reserved	000_0b		r		
18:16	Idle cycle to wait before pre-charging the idle bank Include bit 24 above	001b		**B**		000 = 0 cyc, 001 = 8 cyc (safe) 010 = 12 cyc, 011 = 16 cyc 100 = 24 cyc, 101 = 32 cyc 110 = 48 cyc, 111 = Disable
15:14	Page Hit request before a nonPage hit	10b		**B**		00 = 1 cyc, 01 = 4 cyc 10 = 8 cyc (safe), 11 = 16 cyc
13:12	Reserved	00b		r		
11:9	t_{RC} = Bank Cycle Time $t_{RAS} + t_{RP}$ *or SPD# 41 (new, not yet implemented)*	xxxb		**B**	FSB and SPD	000 = 3 cyc, 001 = 4 cyc 010 = 5 cyc, 011 = 6 cyc 100 = 7 cyc, 101 = 8 cyc (safe) 110 = 9 cyc, 111 = 10 cyc
8:7	t_{RP} = Precharge Time SPD # 27	xxb		**B**	FSB SPD	00 = 3 cyc (safe), 01 = 2 cyc 10 = 1 cyc, 11 = 4 cyc

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x54h	**SDRAM Timing**					
6:4	t_{RAS} = Minimum Bank Active Time SPD # 30	xxxb		B	FSB and SPD	000 = 2 cyc, 001 = 3 cyc 010 = 4 cyc, 011 = 5 cyc 100 = 6 cyc 101 = 7 cyc (safe) 110 = 8 cyc, 111 = 9 cyc
3:2	t_{CL} = CAS Latency SPD # 25 or # 23 or # 9	xxb		B	FSB and SPD	00 = 3 cyc (optional on DIMM, **not** recommended) 01 = 2 cyc, recommended 10 = 2.5 cyc, 11-reserved
1:0	t_{RCD} – RAS to CAS Latency SPD # 29	xxb		B	FSB and SPD	00 = 1 cyc, 01 = 2 cyc 10 = 3 cyc (safe), 11 = 4 cyc

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7.1.1 Example Settings for Memory Timing

The table below provides example BIOS settings for the DRAM Timing register, for both 100-MHz and 133-MHz bus speeds. Note some register bits change based on the DIMM type:

- *U* for Unbuffered DIMMs
- *R* for registered DIMMs

Note also that SPD values observed to date are from production DIMMs. Future additions and changes to the SPD bytes should be expected.

0x0x0x54h	SDRAM Timing	100 MHz		133 MHz		SPD	ns	
		U	R	U	R			
31	SPBWaitState	0b		1b				0 @ 100 MHz , 1 @ 133 MHz FSB
30	AddrTiming_A SPD # 21	0b	1b	0b	1b			0 @ Unbuff, 1 @ Reg DIMM
29	AddrTiming_B, SPD # 21	0b	1b	0b	1b			0 @ Unbuff, 1 @ Reg DIMM
28	RD_Wait_State	1b		1b				Must = 1
27	Reg_DIMM_En, SPD # 21	0b	1b	0b	1b			0 @ Unbuff, 1 @ Reg DIMM
26	t_{WTR} = Write Data In to Read CMD	1b		1b				0 = 1 Clock, 1 = 2 Clocks
25:24	t_{WR} = Write Recovery Time	10b		10b				00b=1 Clock, 01b=Reserved 10b=2 Clocks, 11b=3 Clocks
23	t_{RRD}=ActBnkAtoActBnkCMD SPD # 28	0b		0b		**3Ch**	15	0 = 2 Clocks, 1 = 3 Clocks
22:19		0000b		0000b				
18:16	Idle cycle to wait before precharging the idle bank	001b		001b				000 = 0 cyc, 001 = 8 cyc (safe) 010 = 12 cyc, 011 = 16 cyc 100 = 24 cyc, 101 = 32 cyc 110 = 48 cyc, 111 = Disable
15:14	Page Hit request before a nonPage hit	10b		10b				00 = 1 cyc, 01 = 4 cyc 10 = 8 cyc, (safe) 11 = 16 cyc
13:12		00b		00b				
11:9	t_{RC} = Bank Cycle Time t_{RAS} + t_{RP} or SPD# 41(new, not yet implemented)	100b		110b to 111b		**41h to 46h**	65 to 70	000 = 3 cyc, 001 = 4 cyc 010 = 5 cyc, 011 = 6 cyc 100 = 7 cyc, 101 = 8 cyc (safe) 110 = 9 cyc, 111 = 10 cyc
8:7	t_{RP} = Precharge Time SPD # 27	01b		00b		**50h**	20	00 = 3 cyc (safe), 01 = 2 cyc 10 = 1 cyc, 11 = 4 cyc
6:4	t_{RAS} = Minimum Bank Active Time SPD # 30	011b		100b to 101b		**2Dh to 32h**	45 to 50	000 = 2 cyc, 001 = 3 cyc 010 = 4 cyc, 011 = 5 cyc 100 = 6 cyc, 101 = 7 cyc (safe) 110 = 8 cyc, 111 = 9 cyc
3:2	t_{CL} = CAS Latency SPD # 25 (Not Available) # 23 # 9	---- 01b 01b 10b 10b		---- ---- 01b --00b-- 10b		 **A0h 75h** **A0h 75h**		00 = 3 cyc (optional on DIMM, **not** recommended) 01 = 2 cyc, recommended 10 = 2.5 cyc 11 = reserved (See 00 above.)
1:0	t_{RCD} – RAS to CAS Latency SPD # 29	01b		10b		**50h**	20	00 = 1 cyc, 01 = 2 cyc 10 = 3 cyc (safe), 11 = 4 cyc

Registers ----- Bits	Description	Initialized/ Required value	Actual Value	Key	fcn( )	Notes
0x0x0x58h	**SDRAM Mode/Status**					
31	Clk_Dis5 – DIMM Clock 5	xb		E	MB	0=Enable, 1=Disable
30	Clk_Dis4 – DIMM Clock 4	xb		E	MB	0=Enable, 1=Disable
29	Clk_Dis3 – DIMM Clock 3	xb		E	MB	0=Enable, 1=Disable
28	Clk_Dis2 – DIMM Clock 2	xb		E	MB	0=Enable, 1=Disable
27	Clk_Dis1 – DIMM Clock 1	xb		E	MB	0=Enable, 1=Disable
26	Clk_Dis0 – DIMM Clock 0	xb		E	MB	0=Enable, 1=Disable
25	SDRAM Init	1b		**B**		Set to start memory controller. All other memory config bits should be set before setting this bit. Stays set, can be reset but not to 0.
24	Reserved	0b		r		
23	Mode register status	xb		**B**		To be set before or with SDRAM Init. Causes writing of the memory mode register when SDRAM Init is set. After setting, drops to 0 when function complete. Cannot be set to 0.
22:21	STR_Control = Suspend to RAM Control	xxb		**B**		Set <---> Last Power State 01b <---> MOFF, S4 or S5 10b <---> S3 Refer to "S3 Suspend to RAM State Requirements" on page 190 for details.
20	Burst refresh enable	0b		**B**		0-Disable, 1-Enable
19	Ref_Dis = Refresh Disable	0b		**B**		1 = Disable Refresh = Debug Bit
18	Reserved	0b		**B**		
17:16	Cycles per (between) Refresh SPD # 12	xxb		**B**	FSB and SPD	@100 MHz FSB: 00 = 2K cyc, 01 = 1.5K cyc 10 = 1K cyc, 11 = 0.75K cyc @133-MHz FSB: 00=1.5K cyc, 01=1.1K cyc 10=0.75K cyc, 11=0.37K cyc
15:8		0_0h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
7	CS7_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
6	CS6_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
5	CS5_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
4	CS4_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
3	CS3_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
2	CS2_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
1	CS1_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices
0	CS0_X4Mode Chip-Select x4 Enable SPD # 13	xb		**B**	SPD	0=x8/x16, 1=x4 DIMM devices

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x60h	**BIU0 Status/Control**					
31	Probe enable for CPU0	1b		**B**		0=Disable, 1=Enable
30:28	Reserved	000b		**B**		
27:25	Xca_Probe_Cnt	010b		**B**		
24:22	Xca_RD_Cnt	110b		**B**		
21:19	Xca_WR_Cnt	110b		**B**		
18	AMD Athlon system bus halt disconnect enable	0b		**B**		0=Disable 1=Enable Refer to "Power Management" on page 185 for details.
17	AMD Athlon system bus stop grant disconnect enable	1b		**B**		0=Disable, 1=Enable Refer to "Power Management" on page 185 for details.
16:14	Probe limit	110b		**B**		0-7 = 1 to 8 probes 110b = 7 recommended
13:10	Ack limit 0000 = 1 un-acked command 0001 = 2.....	0011b		r		This field should be used to set up SysAckLimit in AMD Athlon™ (+1 to this value) (SYSCFG)
9	Bypass_ En Super Bypass Enable	1b		**B**		0=Disable, 1=Enable
8:7	SysDC_Out_ delay	yyb		r		From init logic
6:3	SysDC_In_ delay	yyyyb		r		From init logic
2	WR2_RD	yb		r		From init logic
1:0	RD2_WR	yyb		r		From init logic
0x0x0x64h	**BIU0 SIP**					
31	ClkFwd Offset	0b		**B**		0=Delay groups 1 and 3 1=No delays
30:0	RO from Init/SIP logic	yyyb yy_yyyyh		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x70h	**MRO Status/Control**					
31:19	Reserved	0b		r		
18	Self_Ref_En	1b		**B**		Enable memory self refresh for S1/S3 states.
17:11	Reserved	0000000b		**B**		
10	PCI pipe enable	1b		**B**		0 = MRO checks outstanding read probe before PCI transactions 1 = MRO pipelines PCI transactions
9	PCI Block Write Enable	1b		**B**		0 = BIU does RID/INV probes, forcing MRO MWQ to wait for data movement 1 = BIU does NOP/INV probes for PCI full-block writes
8:0	Reserved	000h		**B**		
0X0X0X80h	**Who AM I**					
31:17	Reserved	00b 000h		r		
16	BIU0 present	1b		c		
15:8	First AMD Athlon system bus ID	00h		c		
7:0	Who AM I	00h		c		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn()	Notes
0x0x0x84h	**PCI Arbitration Control**					
31:24	AGP VGA BIOS address decode	0Fh		**A**		System config dependent Bit 31: 0D_C000 = 0D_FFFF Bit 30: 0D_8000 = 0D_BFFF … Bit 24: 0C_0000 = 0C_3FFF One or more of these bits should be set if an AGP card has a ROM BIOS.
23	Tgt_Latency	0b		**B**	0x0x0 x84[3]	0=AMD-751™ System Controller-Compatible 1=PCI Maximum Target Latency Rule. When =1, 0x0x0x84[3] must = 0.
22:18	Reserved	000_00b		r		
17	AGP Chaining	1b		**B**		Enabled = 1, when set CPU writes to AGP are chained
16	PCI Chaining	1b		**B**		Enabled = 1, when set CPU writes to PCI are chained
15	MDA Support	0b		**A**		Enabled = 1, allows monochrome adapter for AGP device driver debug. Normally 0. See *AMD-761™ System Controller Data Sheet*, order# 24088, for information.
14	PCI Write-Post retry	1b		**B**		1 = Enables retry on PCI if there are pending posted writes
13	AGP Write Post retry	1b		**B**		1 = Enables retry on AGP if there are pending posted writes
12	Dis Rd Data Err	1b		**B**		0 = Returns read data error to processor on master abort or target abort 1 = AMD-761™ system controller returns all 1s on data read error

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
11	Dis AGP Early Probe	0b		**A**		1 = Disable early snoop from AGP master running a PCI cycle to memory
10	Dis PCI Early Probe	0b		**B**		1 = Disable early probe request for write cycles from an external PCI master
9	Dis AGP arbiter pipelining	0b		**A**		1 = Disable AGP arbiter from pipelining grants onto bus
8	Southbridge lock disable	0b		**B**		1 = Disable flushing function performed before granting bus to the Southbridge
7	PM register enable	xb		**P**		1 = Enables R/W accesses to PM register at 0:0x18 BAR2 – AGP Power management
6	15-Mbytes hole enable	xb		**B**		1 = Enable a memory hole at 15-16 Mbytes
5	14-Mbytes hole enable	xb		**B**		1 = Enable a memory hole at 14-15 MBytes
4	EV6 mode	1b		**B**		1 = Enable PCI decoding in EV6 mode. Used for opening buffers in 640K to 1-Mbyte memory address space. Legacy USB/SCSI devices sometimes need this capability.
3	Target latency timer disable	1b		**B**	0x0x 0x84 [23]	1 = Disable AMD-751™ system controller target latency timer on both PCI and AGP's PCI interfaces
2	ApcPreEn	0b		**B**		1 = Disables AMD-751 system controller to prefetch data from SDRAM when a PCI master on AGP bus reads from main memory
1	PciPreEn	0b		**B**		1 = Enables AMD-751 system controller to prefetch data from SDRAM when a PCI master on PCI bus reads from main memory
0	ParkPCI	0b		**B**		0 = PCI arbiter parks on processor accesses to PCI 1 = Enables parking on an external PCI master

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Registers ---- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0x88h	**Config Status**					
31:29	AGP_Clk_Mux	yyyb		r		
28:26	Sys_Clk_Mux	yyyb		r		
25	Type_Det	yb		r		0=1.5-V AGP Card Signalling 1=3.3-V AGP Card Signalling
24	S2K_Thresh	yb		r		
23	K7_PP_En	1b		r		
22	IG_PP_En	1b		r		
21:20	Clk_Speed	yyb		r		FSB speed: 00b=100 MHz 01b=66 MHz 10b= Reserved 11b=133 MHz
19:18	Reserved	yyb		r		
17:16	S2K_Bus_Len	yyb		r		
15	Tristate_En	yb		r		
14	Nand_En	yb		r		
13	Bypass_PLLs	yb		r		
12	Dis_Divider	yb		r		
11:8	Reserved	yh		r		
7	Sip_ROM	yb		r		
6	Reg_DIMM_En	yb		r		0=Unbuffered, 1=Registered
5	In_Clk_En	yb		r		
4	Out_Clk_En	yb		r		
3:0	CPU0_Divider	yh		r		
0x0x0x9Ch	**PCI Top of Memory**					
31:24	PCI Memory Top	xxh		B		Actual Memory Size AD[31:24]
23:0	Reserved	000_0000h		r		

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Registers ---- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xA0h	**AGP Capability Identifier**					
31:24	Reserved	00h		r		
23:20	Major_Rev	2h		r		
19:16	Minor_Rev	0h		r		
15:8	Next_Pointer	00h		r		Null = Final item on list
7:0	Cap_ID	02h		r		02h = AGP
0x0x0xA4h	**AGP Status Register**					
31:24	Max_ReqQ_Depth	0Fh		r		Max # AGP Command Requests
23:10	Reserved	00b 000h		r		
9	SBA	1b		r		Side Band Addressing Supported
8:6	Reserved	000b		r		
5	R4G	0b		r		Fixed at 4 Gbytes Maximum
4	FW	yb		r	0x0x 0B4 [7]	1 = Fast Write Support 0 = Fast Write Not Supported
3	Reserved	0b		r		
2:0	Rates	111b		r		AMD-761 system controller supports 1x/2x/4x
0x0x0xA8h	**AGP Command Register**					
31:10	Reserved	0000_0h 00b		r		
9	SBA_Ena Sideband addressing enable	yb		o		Set by operating system agent, **not** BIOS. 0 = Disable, 1 = Enable
8	AGP_Ena AGP operation enable	yb		o		Set by operating system agent, **not** BIOS. 0 = Disable, 1 = Enable
7:6	Reserved	0b		r		
5	Greater than 4G address support	0b		r		0 = Disable, 1 = Enable
4	Fast_Writes	yb		o	0x0x0 B4[7]	0=Disabled, 1=Enabled
3	Reserved	0b		r		
2:0	AGP data transfer mode	yyyb		o		001b=1x, 010b=2x,100b=4x

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xACh	**AGP Virtual Address Space Size Register**					
31:17	Reserved	yyyb 000h		r		
16	VGA_IA_En	xb		**B**		0 = No ISA aliasing on address [15:0] 1 = Force AMD-751™ system controller to alias ISA address [15:0]
15:4	Reserved	000h		r		
3:1	VA_Size AGP aperture size	xxxb		**A**		000 = 32 Mbytes 001 = 64 Mbytes 010 = 128 Mbytes 011 = 256 Mbytes 100 = 512 Mbytes 101 = 1 Gbyte 110 = 2 Gbytes 128 Mbytes recommended
0	GARTEna AGP aperture base address enable	xb		**A**		0 = Disable register 1 = Enable register 0:0x10 (BAR0) and start GART
0x0x0xB0h	**Gart/AGP Mode Control**					
31:21	Reserved	00h 000b		r		
20	Reserved	0b		**B**		
19	NonGART Snoop	0b		**B**		Debug/Performance register 0 = Disable probes 1 = Enable probes
18	Reserved	0b		**B**		
17	GART page directory cache enable	0b		**B**		Debug/Performance register 0 = Disable, 1 = Enable
16	GART Index Scheme control	yb		o		0 = 2-Level, 1 = 1-Level Mode
15:0	Reserved	00h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xB4h	**AGP 4x Dynamic Compensation**					
31:28	PVal	yh		c		P transistor strength, xfer I/O pads
27:24	NVal	yh		c		N transistor strength, xfer I/O pad
23	Reserved	0b		r		
22	DisStrb	0b		**A**		1=Disable ADSTB[1:0}#
21:16	Quantum_Cnt	000001b		**A**		100-ms intervals for Always_Compensate
15:8	Reserved	00h		r		
7	FW_Enable	xb		**A**	B4/BF	0=Disable, 1=Enable Controls 0x0x0xA4h[4] and 0x0x0xA8h[4] Refer to "Feature Override Bits for AGP Cards" on page 208 for details.
6	4x_Override	xb		**A**	B4/BF	0=Disabled, 1=Enabled -> Forces 0x0x0xA4h[0]->010b->2x AGP Refer to "Feature Override Bits for AGP Cards" on page 208 for details.
5	Comp3.3	0b		**A**		Do_Compensate=1 shows PVal and NVal when Comp3.3 =1 with 3.3-V AGP cards
4:3	Reserved	0b		r		
2	PCI drive strength	0b		**A**		Normally = 0
1	Always_Compensate	xb		**A**	B4/BB	0=Disable, 1=Enable Refer to "AGP Interface" on page 205 for details.
0	Do_Compensate	0b		**A**		Set to init dynamic compensation Clears when finished

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xB8h	**AGP Compensation Bypass**					
31:28	BYP_PDrvXfer	xh		**A**	B4/BB	P Drive bypass value for data Refer to "BIOS Initialization Requirements" on page 209 for details.
27:24	BYP_NDrvXfer	xh		**A**	B4/BB	N Drive bypass value for data Refer to "BIOS Initialization Requirements" on page 209 for details.
23	BYPXfer	xb		**A**	B4/BB	1=Enable Drive Bypass for Data Refer to "BIOS Initialization Requirements" on page 209 for details.
22:20	Reserved	000b		r		
19:18	BYP_PSlewXfer	xxb		**A**	B4/BB	P slew rate value for data Refer to "BIOS Initialization Requirements" on page 209 for details.
17:16	BYP_NSlewXfer	xxb		**A**	B4/BB	N slew rate value for data Refer to "BIOS Initialization Requirements" on page 209 for details.
15:12	BYP_PDrvStrb	xh		**A**	B4/BB	P drive bypass value for strobes Refer to "BIOS Initialization Requirements" on page 209 for details.
11:8	BYP_NDrvStrb	xh		**A**	B4/BB	N drive bypass value for strobes Refer to "BIOS Initialization Requirements" on page 209 for details.

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
7	BYPStrb	xb		**A**	B4/BB	1=Enable Drive Bypass for Strobes Refer to "BIOS Initialization Requirements" on page 209 for details.
6:4	Reserved	000b		r		
3:2	BYP_PSlewStrb	xxb		**A**	B4/BB	P slew rate value for strobes Refer to "BIOS Initialization Requirements" on page 209 for details.
1:0	BYP_NSlewStrb	xxb		**A**	B4/BB	N slew rate value for strobes Refer to "BIOS Initialization Requirements" on page 209 for details.

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7.1.2 Examples: AGP Compensation Register Settings (0xB4-0xBB)

TYPEDET# 0x0x0x88[25]

Type_Det = 1 indicates that a card in the AGP slot is a 3.3-V signalling card, which supports 2X AGP maximum. A 3.3-V signalling card **cannot** run above 2X AGP.

Type_Det = 0 indicates that a card in the AGP slot is a 1.5-V signalling card, which supports 4X AGP maximum. A 1.5-V signalling card can run at 1X, 2X, or 4X AGP rates.

Refer to "AGP Interface" on page 205 for details on how the value of the Type_Det bit and the settings of the AGP compensation register affect the settings in AGP Compensation Bypass register.

Type_Det = 1 2X AGP Maximum Type_Det =1 == 3.3-V card in AGP slot									
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**No Option**
	48h	00h	01h	C5h	0Fh	FFh	0Fh	C5h	

Type_Det = 0 4X AGP Maximum, Reduced to 2X AGP with 4X_Override									
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 1**
	4Ah	00h	01h	D8h	8Fh	FFh	04h	D8h	4x_Override and Always_Compensate
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 2**
	48h	00h	01h	D8h	8Fh	FFh	84h	D8h	4x_Override and Bypass

Type_Det = 0 4xAGP Maximum, Options of Always Compensate, Bypass and Fast Writes									
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 1**
	02h	00h	01h	D8h	8Fh	FFh	04h	D8h	Always_Compensate
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 2**
	82h	00h	01h	D8h	8Fh	FFh	04h	D8h	Always Compensate and Fast Writes
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 3**
	00h	00h	01h	D8h	8Fh	FFh	84h	D8h	Bypass
0x0x0x..	**B4h**	**B5h**	**B6h**	**B7h**	**B8h**	**B9h**	**BAh**	**BBh**	**Option 4**
	80h	00h	01h	D8h	8Fh	FFh	84h	D8h	Bypass and Fast Writes

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xC0h	**Memory Base Address Register 0**					
31:23	CS_Base Chip-Select Base 0 Bank 0 base address Starting address of the bank Map to AD[31:23]	xxh xb		**B**		Set by memory sizing routines 0000_0000_0b = 0 0000_0001_0b = 16 Mbytes 0000_0010_0b = 32 Mbytes 0000_0011_0b = 48 Mbytes 0000_1000_0b = 128 Mbytes 0001_0000_0b = 256 Mbytes 0010_0000_0b = 512 Mbytes, etc.
22:16	Reserved	000b 0h		r		
15:7	CS_Mask Chip-Select Mask 0 Bank 0 address mask Sizes the bank Map to AD[31:23]	xxh xb		**B**		Set by memory sizing routines 0000_0000_1b = 16 Mbytes 0000_0001_1b = 32 Mbytes 0000_0011_1b = 64 Mbytes 0000_0111_1b = 128 Mbytes 0000_1111_1b = 256 Mbytes 0001_1111_1b = 512 Mbytes 0011_1111_1b = 1 Gbyte 0111_1111_1b = 1 Gbyte
6:3	Reserved	0h		r		
2:1	Addr_Mode Size of Device = Size of Bank x (Primary SDRAM Width /8)	xxb		**B**	SPD # 31 and 13	01b=SDRAM device <256 Mbits 10b=SDRAM device >128 Mbits 00b and 11b are reserved
0	Enable/Disable Bank 1	xb		**B**		0=Disable CS, 1=Enable CS
0x0x0xC4h	**Memory Base Address Register 1**					
31:23	Chip-Select Base 1	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 1	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 1	xb		**B**		As 0x0x0xC0h above

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xC8h	**Memory Base Address Register 2**					
31:23	Chip-Select Base 2	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 2	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 2	xb		**B**		As 0x0x0xC0h above
0x0x0xCCh	**Memory Base Address Register 3**					
31:23	Chip-Select Base 3	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 3	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 3	xb		**B**		As 0x0x0xC0h above

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Memory Rules

1. Memory must be organized so that the largest banks occupy the lowest addresses.
2. All memory registers must be initialized, even when they are 0 memory registers do not default to 0.
3. Unbuffered memories can be configured two deep, registered memories can be configured four deep. In all cases, unused memory registers must be zeroed.

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x0xD0h	**Memory Base Address Register 4**					
31:23	Chip-Select Base 4	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 4	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 4	xb		**B**		As 0x0x0xC0h above
0x0x0xD4h	**Memory Base Address Register 5**					
31:23	Chip-Select Base 5	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 5	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 5	xb		**B**		As 0x0x0xC0h above
0x0x0xD8h	**Memory Base Address Register 6**					
31:23	Chip-Select Base 6	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 6	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 6	xb		**B**		As 0x0x0xC0h above
0x0x0xDCh	**Memory Base Address Register 7**					
31:23	Chip-Select Base 7	xxh xb		**B**		As 0x0x0xC0h above
22:16	Reserved	000b 0h		r		As 0x0x0xC0h above
15:7	Chip-Select Mask 7	xxh xb		**B**		As 0x0x0xC0h above
6:3	Reserved	0h		r		As 0x0x0xC0h above
2:1	Addr_Mode	xxb		**B**		As 0x0x0xC0h above
0	Enable/Disable Bank 7	xb		**B**		As 0x0x0xC0h above

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7.1.3 PCI Bus 0, Device 0, Function 1 Registers

The Device 0, Function 1 registers are used for the purpose of controlling the DDR SDRAM interface drive strengths, and calibration of the Programmable Delay Lines (PDLs).

All Function 1 register bits are defaulted to an unknown value as required for the AMD-761 system controller to support the Advanced Configuration and Power Interface (ACPI) S3 (Suspend to RAM) state.

For proper operation, it is absolutely necessary that BIOS initialize all Function 1 register bits.

Please obtain the *AMD-761™ System Controller Revision Guide*, order# 23613, for the most current information for each silicon revision.

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x40h	**DDR PDL Calibration Control**					
31:8	Reserved	0000_000h		r		
7	SW_Recal Set after setting SW_Cal_Dly	0b		**B**		Write 1=>Calibration 0=Calibration Complete 1=Calibration Not Complete
6	Use_Act_Dly Use Actual Delay	0b		**B**		0=Disable, 1=Enable SW_Recal and Auto_Cal_En Must = 0 When Use_Act_Dly = 1
5	Auto_Cal_En Auto Calibration Mode	1b		**B**		0=Disable 1=Enable Refer to *AMD-761™ System Controller Revision Guide*, order# 23613, for special instructions for Revision B2 silicon.
4	Act_Dly_Inh Actual Delay Update Inhibit	0b		**B**		0=Disable 1=Enable Refer to *AMD-761™ System Controller Revision Guide*, order# 23613, for special instructions for Revision B2 silicon.
3:2	Reserved	00b		r		
1:0	Auto_Cal_Period Auto-Calibration Period	01b		**B**		00=10000 System Clocks 01=1000000 System Clocks 10=10000000 System Clocks 11=Reserved
0x0x1x44h	**DDR PDL Configuration Register 0**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x48h	**DDR PDL Configuration Register 1**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x4Ch	**DDR PDL Configuration Register 2**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		from SW_Recal or Direct Write
0x0x1x50h	**DDR PDL Configuration Register 3**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		from SW_Recal or Direct Write
0x0x1x54h	**DDR PDL Configuration Register 4**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x58h	**DDR PDL Configuration Register 5**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x5Ch	**DDR PDL Configuration Register 6**					
31:24	Clk_Dly	yyh		c		Half Period of the Sys. Clk.
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x60h	**DDR PDL Configuration Register 7**					
31:24	Clk_Dly	yyh		c		Half Period of the Sys. Clk.
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x64h	**DDR PDL Configuration Register 8**					
31:24	Clk_Dly	yyh		c		Half Period of the Sys. Clk.
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x68h	**DDR PDL Configuration Register 9**					
31:24	Clk_Dly	yyh		c		Half Period of the Sys. Clk.
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x6Ch	**DDR PDL Configuration Register 10**					
31:24	Clk_Dly	yyh		c		Half Period of the Sys. Clk.
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
KEY:	**B= Mandatory BIOS function** **P= Power management setup by BIOS** r = Hardcoded and reserved	**A= AGP setup by BIOS** o = Setup by OS or OS driver u = PCI operational user interface		c = Calculated/set by AMD-761™ internal logic F = Performance enhancement set by BIOS E = Elective BIOS function		

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x70h	**DDR PDL Config Register 11**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x74h	**DDR PDL Config Register 12**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x78h	**DDR PDL Config Register 13**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x7Ch	**DDR PDL Config Register 14**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x8h	**DDR PDL Config Register 15**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x8h	**DDR PDL Config Register 16**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write
0x0x1x8h	**DDR PDL Config Register 17**					
31:24	Clk_Dly	yyh		c		Half Period of the System Clock
23:16	SW_Cal_Dly	xxh		**B**	FSB	Delay for DQS: 100 MHz = 69h 133 MHz = 6Bh
15:8	Cal_Dly	yyh		c		SW_Cal_Dly in # of Buffers
7:0	Act_Dly	xxh		c		From SW_Recal or Direct Write

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x8Ch	**DDR DQS/MDAT Pad Config**					
31:30	Reserved	00b		r		
29:27	PSlewMDAT	101b		**B**		Slowest 000b <-> 111b Fastest MDAT Rising Edge Slew Rate
26:24	NSlewMDAT	101b		**B**		Slowest 000b <-> 111b Fastest MDAT Falling Edge Slew Rate
23:20	Reserved	0h		r		
19:18	PDrvMDAT	11b		**B**		Weakest 00b<->11b Strongest MDAT P Transistor Drv Strength
17:16	NDrvMDAT	10b		**B**		Weakest 00b<->11b Strongest MDAT N Transistor Drv Strength
15:14	Reserved	00b		r		
13:11	PSlewDQS	101b		**B**		Slowest 000b <-> 111b Fastest DQS Rising Edge Slew Rate
10:8	NSlewDQS	101b		**B**		Slowest 000b <-> 111b Fastest DQS Falling Edge Slew Rate
7:4	Reserved	0h		r		
3:2	PDrvDQS	11b		**B**		Weakest 00b<->11b Strongest DQS P Transistor Drv Strength
1:0	NDrvDQS	10b		**B**		Weakest 00b<->11b Strongest DQS N Transistor Drv Strength

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x90h	**DDR CLK/CS Pad Configuration**					
31:30	Reserved	00b		r		
29:27	PSlewCLK	101b		**B**		Slowest 000b <-> 111b Fastest CLK Rising Edge Slew Rate
26:24	NSlewCLK	101b		**B**		Slowest 000b <-> 111b Fastest CLK Falling Edge Slew Rate
23:20	Reserved	0h		r		
19:18	PDrvCLK	11b		**B**		Weakest 00b<->11b Strongest CLK P Transistor Drv Strength
17:16	NDrvCLK	10b		**B**		Weakest 00b<->11b Strongest CLK N Transistor Drv Strength
15:14	Reserved	00b		r		
13:11	PSlewCS	101b		**B**		Slowest 000b <-> 111b Fastest CS Rising Edge Slew Rate
10:8	NSlewCS	101b		**B**		Slowest 000b <-> 111b Fastest CS Falling Edge Slew Rate
7:4	Reserved	0h		r		
3:2	PDrvCS	11b		**B**		Weakest 00b<->11b Strongest CS P Transistor Drv Strength
1:0	NDrvCS	10b		**B**		Weakest 00b<->11b Strongest CS N Transistor Drv Strength

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x94h	**DDR CMDB/CMDA Pad Configuration**					
31:30	Reserved	00b		r		
29:27	PSlewCMDB	101b		**B**		Slowest 000b <-> 111b Fastest CMDB Rising Edge Slew Rate
26:24	NSlewCMDB	101b		**B**		Slowest 000b <-> 111b Fastest CMDB Falling Edge Slew Rate
23:20	Reserved	0h		r		
19:18	PDrvCMDB	11b		**B**		Weakest 00b<->11b Strongest CMDB P Transistor Drv Strength
17:16	NDrvCMDB	10b		**B**		Weakest 00b<->11b Strongest CMDB N Transistor Drv Strength
15:14	Reserved	00b		r		
13:11	PSlewCMDA	101b		**B**		Slowest 000b <-> 111b Fastest CMDA Rising Edge Slew Rate
10:8	NSlewCMDA	101b		**B**		Slowest 000b <-> 111b Fastest CMDA Falling Edge Slew Rate
7:4	Reserved	0h		r		
3:2	PDrvCMDA	11b		**B**		Weakest 00b<->11b Strongest CMDA P Transistor Drv Strength
1:0	NDrvCMDA	10b		**B**		Weakest 00b<->11b Strongest CMDA N Transistor Drv Strength

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x0x1x98h	**DDR MAA/MAB Pad Configuration**					
31:30	Reserved	00b		r		
29:27	PSlewMAB	101b		**B**		Slowest 000b <-> 111b Fastest MAB Rising Edge Slew Rate
26:24	NSlewMAB	101b		**B**		Slowest 000b <-> 111b Fastest MAB Falling Edge Slew Rate
23:20	Reserved	0h		r		
19:18	PDrvMAB	11b		**B**		Weakest 00b<->11b Strongest MAB P Transistor Drv Strength
17:16	NDrvMAB	10b		**B**		Weakest 00b<->11b Strongest MAB N Transistor Drv Strength
15:14	Reserved	00b		r		
13:11	PSlewMAA	101b		**B**		Slowest 000b <-> 111b Fastest MAA Rising Edge Slew Rate
10:8	NSlewMAA	101b		**B**		Slowest 000b <-> 111b Fastest MAA Falling Edge Slew Rate
7:4	Reserved	0h		r		
3:2	PDrvMAA	11b		**B**		Weakest 00b<->11b Strongest MAA P Transistor Drv Strength
1:0	NDrvMAA	10b		**B**		Weakest 00b<->11b Strongest MAA N Transistor Drv Strength

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7.2 PCI Bus 0, Device 1, Function 0 Registers

Device 1 registers provide the necessary controls for the AMD-761 system controller's internal PCI-to-PCI bridge and AGP controller functions.

The PCI to PCI bridge functions as a logical bridge between the Host PCI bus and the AGP interface and contains the normal PCI configuration registers for such a device. Most of these bits are read-only.

Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x1x0x00h	**PCI ID**					
31:16	Device ID	700Fh		r		AMD-761™ system controller
15:0	Vendor ID	1022h		r		AMD
0x1x0x04h	**PCI Command and Status**					
31	PERR_Rcv	0b		r		Not supported
30	SERR Sent	yb		u		R/W/1C, from AMD-761 system controller
29	Master ABRT	0b		r		R/W/1C, from bus master
28	Target ABRT	0b		r		R/W/1C, from bus master target
27	Target ABRTS Signaled	0b		r		Not supported
26:25	DEVSEL_Timing	01b		r		
24	Data_PERR	0b		r		
23	FastB2B	0b		r		
22	UDF	0b		r		
21	66M	1b		r		Support 66 MHz on device 1
20	Cap_Lst	0b		r		
19:10	Reserved	00b 00h		r		
9	FBACK	0b				
8	SERR, System Error Enable	yb		u		0 = Disable, 1 = Enable
7	Step	0b		r		
6	PERR	0b		r		
5	VGA Palette Snoop	0b		r		
4	MWINV	0b		r		
3	SCYC	0b		r		
2	MSTR	1b		**B**		DMA enabled on APCI
1	MEM	1b		**B**		Memory access enable on APCI
0	IO	1b		**B**		IO access Enabled on APCI
0x1x0x08h	**PCI Rev ID and Class Code**					
31:24	Class Code	06h		r		Bridge device
23:16	Sub_Class Code	04h		r		Host/PCI bridge
15:8	Prog. I/F	00h		r		Host/PCI bridge
7:0	Revision ID	00h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x1x0x0Ch	**AGP/PCI Header Type**					
31:24	Reserved	00h		r		
23:16	Header_Type	01h		r		
15:8	Pri_Lat_Timer	40h		**B**		
7:0	Reserved	00h		r		
0x1x0x18h	**AGP/PCI Sub Bus Num/ Secondary Latency Timer**					
31:24	Secon_Lat_Timer	40h		**B**		
23:16	Sub_Bus_Num	01h		**B**		
15:8	Secon_Bus_Num	01h		**B**		
7:0	Pri_Bus_Num	00h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x1x0x1Ch	**PCI Command and Status**					
31	PERR_Rcv	0b		r		Not supported
30	SERR_Rcv	yb		u		R/W/1C from AMD-761™ system controller
29	Master ABRT	yb		u		R/W/1C from bus master
28	Target ABRT	yb		u		R/W/1c from bus master target
27	Target ABRTS Signaled	0b		r		Not supported
26:25	DEVSEL_Timing	01b		r		
24	Data_PERR	0b		r		
23	FastB2B	0b		r		
22	UDF	0b		r		
21	66M	1b		r		
20	Cap_Lst	0b		r		
19:16	Reserved	0h		r		
15:12	IO_Lim[15:12]	xh		**B**		Upper 4 bits defining top address that is used by the bridge to forward I/O transactions from one interface to another.
11:8	IOLimit_R	1h		r		Lower 4 bits defining top address that is used by the bridge to forward I/O transactions from one interface to another. 0x1 indicates that 32 bit I/O address decoding is available
7:4	IOBase [15:12]	xh		**B**		Writable 4 bits that defines bottom address that is used by the bridge to forward I/O transactions from one interface to another.
3:0	IOBase_R	1h		r		Lower 4 bits defining bottom address that is used by the bridge to forward I/O transactions from one interface to another. 0x1 indicates that 32 bit I/O address decoding is available.

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x1x0x20h	**AGP/PCI Memory Limit and Base**					
31:20	MLim[31:20]	xxxh		**B**		Memory Limit Address defining top address to be used by AGP target graphics controller for control registers and buffers. The lower 20 bits are 0xFFFFF for 1-Mbyte granularity.
19:16	Reserved	0h		r		
15:4	MBase[31:20]	xxxh		**B**		Memory Limit Address defining lower address to be used by AGP target graphics controller for control registers and buffers. The lower 20 bits are 0xFFFFF for 1-Mbyte granularity.
3:0	Reserved	0h		r		
0x1x0x24h	**AGP/PCI Prefetchable Memory Limit and Base**					
31:20	MLim [31:20]	xxxh		**B**		Prefetchable Memory Limit Address defining top address to be used by AGP target graphics controller for control registers and buffers. The lower 20 bits are 0xFFFFF for 1-Mbyte granularity.
19:16		0h		r		
15:4	MBase [31:20]	xxxh		**B**		Prefetchable Memory Base Address defining lower address to be used by AGP target graphics controller for control registers and buffers. The lower 20 bits are 0xFFFFF for 1-Mbyte granularity.
3:0	Reserved	0h		r		

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Registers ----- Bits	Description	Initialized/ Required Value	Actual Value	Key	fcn( )	Notes
0x1x0x30h	**AGP/PCI I/O Limit and Base**					
31:24	Reserved	00h		r		
23:16	IO_ Lim [23:16]	xxh		**B**		This field defines the upper limit (inclusive) of the 24bit I/O addresses passed to the AGP/PCI bus.
15:8	Reserved	00h		r		
7:0	IO_ Base [23:16]	xxh		**B**		This field defines the base (inclusive) of the 24bit I/O addresses passed to the AGP/PCI bus.
0x1x0x3Ch	**AGP/PCI Interrupt and Bridge Control**					
31:24	Reserved	00h		r		
23	Bridge_Fast_B2B_En	0b		r		
22	Secon_Bus_ Reset	0b		r		
21	Mas_Abort_Mode	0b		r		
20	Reserved	0b		r		
19	VGA_En	1b		**B**		
18	ISA_En	0b		**B**		
17	SERR_En	yb		u		
16	Par_Resp_En	0b		r		
15:8	Int_Pin	xxh		**B**		Enabled by 0x1x0x40[0]
7:0	Int_Line	xxh		**B**		
0x1x0x40h	**Miscellaneous Device 1 Control**					
31:1	Reserved	000b 0000000h		r		
0	Int_Pin_Cntl	xb		**B**		1=Enable 0x1x0x3C[15:8]

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