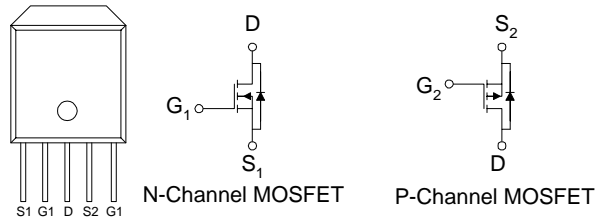


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature DPAK Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	20 @ $V_{GS} = 4.5V$	51
	16 @ $V_{GS} = 10V$	41
-30	33 @ $V_{GS} = -4.5V$	-41
	23 @ $V_{GS} = -10V$	-31



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	20	-20	
Continuous Drain Current ^a	$T_A=25^\circ C$ I_D	51	-41.0	A
Pulsed Drain Current ^b	I_{DM}	± 40	± 40	
Continuous Source Current (Diode Conduction) ^a	I_S	30	-30	A
Power Dissipation ^a	$T_A=25^\circ C$ P_D	50	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-1			
Gate-Body Leakage	I _{GSS}	V _{GS} = -20 V, V _{DS} = 0 V	P			±100	nA
		V _{GS} = 20 V, V _{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -10 V	P	-50			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	N			16	mΩ
		V _{GS} = 4.5 V, I _D = 8.4 A				20	
		V _{GS} = -10 V, I _D = -8.5 A	P			23	
		V _{GS} = -4.5 V, I _D = -6.8 A				33	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 10 A	N		40		S
		V _{DS} = -15 V, I _D = -9.5 A	P		31		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =10A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-10A	N		12		nC
Gate-Source Charge	Q _{gs}		P		13		
			N		3.3		
Gate-Drain Charge	Q _{gd}		P		5.8		
			N		4.5		
			P		12		
Switching							
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =25Ω, P-Channel V _{DD} =-15V, V _{GS} =-10V, I _D =-1A R _{GEN} =15Ω	N		20		nS
Rise Time	t _r		P		15		
			N		9		
Turn-Off Delay Time	t _{d(off)}		P		16		
			N		70		
Fall-Time	t _f		P		62		
			N		20		
			P		46		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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