AME, Inc.

Preliminary

AME9003 **CCFL Backlight Controller**

■ General Description

The AME9003 is AME's next generation direct drive CCFL controller. Like its cousins, the AME9001 and AME9002, the AME9003 controller provides a cost efficient means to drive single or multiple cold cathode fluorescent lamps (CCFL), driving 3 external MOSFETs that, in turn, drive a wirewound transformer that is coupled to the CCFL.

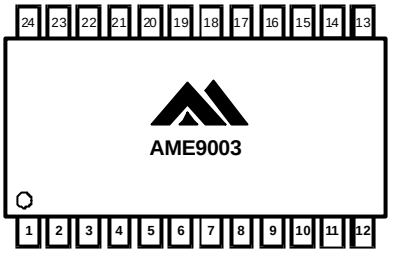
The AME9003, like the AME9002 includes extra circuitry that allows for a special one second start up period wherein the voltage across the CCFL is held at a higher than normal voltage to allow older tubes (or cold tubes) a period in which they can" warm up". During this one second startup period the driving frequency is adjusted off of resonance so that the tube voltage can be controlled. As soon as the CCFL " strikes" the special start up period ends and the circuit operates in its normal mode. However the AME9003 uses an extra capacitor to accurately set the start up interval. In addition to that the AME9003 features a soft start AND soft finish on each dimming cycle edge in order to minimize any audible vibrations during the dimming function.

The AME9003 also includes features such as, dimming control polarity selection, undervoltage lockout and fault detection. It is designed to work with input voltages from 7V up to 24V. When disabled the circuit goes into a zero current mode.

■ Features

- Small 24 pin QSOP package
- 24 pin PDIP/SOIC also available
- Drives multiple tubes
- Special 1 second start up mode
- Automatically checks for common fault conditions
- 7.0V < Vbatt < 24V
- Low component count
- Low Idd < 3.5mA
- <1uA shutdown mode
- Battery UV lockout
- Brightness polarity select
- Soft-start, soft-finish dimming

■ Pin Configuration

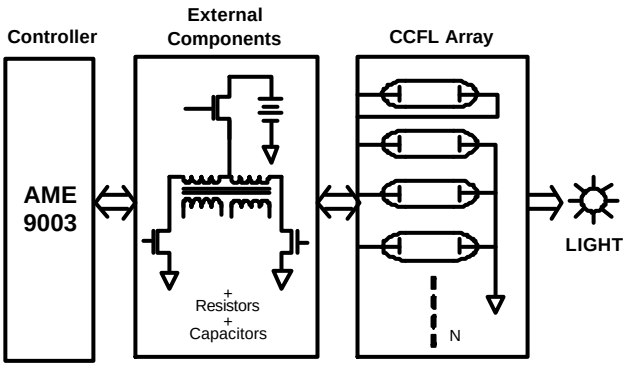


AME9003

1. VREF	13. OUTC
2. CE	14. OUTAPB
3. SSC	15. OUTA
4. RDELTA	16. VBATT
5. SSC1ST	17. BRPOL
6. RT2	18. VDD
7. VSS	19. CT1
8. OVPH	20. FB
9. OVPL	21. COMP
10.FCOMP	22. BRIGHT
11.CSDET	23. SSV
12.BATTFB	24. PNP

Evaluation Board Available !!

■ System Block Diagram



■ Applications

- Notebook computers
- LCD/TFT displays

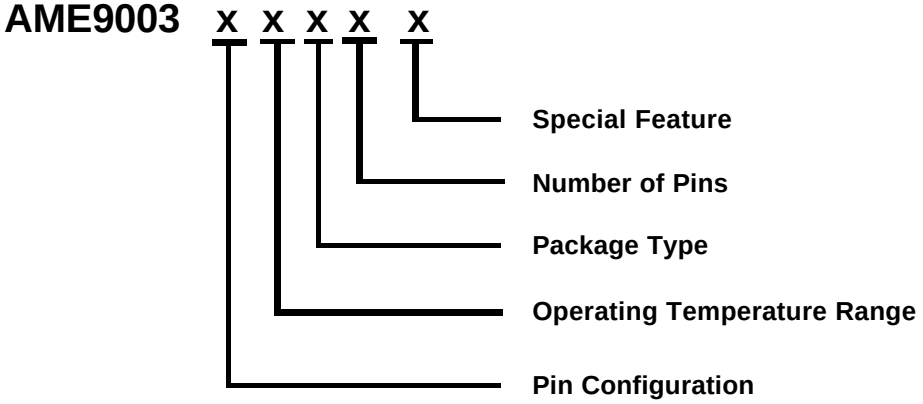
■ Pin Description

Pin #	Pin Name	Pin Description
1	VREF	Reference. Compensation point for the 3.4V internal voltage reference. Must have bypass capacitor connected here to VSS.
2	CE	Chip enable. When low (<0.4V) the chip is put into a low current (~0uA) shutdown mode.
3	SSC	Blanking interval ramp. During the first cycle this pin sources 1.5uA. The first cycle is used to define the initial start up period, often on the order of one second. During subsequent cycles SSC sources 140μA. This is primarily used to provide a "blanking interval" at the beginning of every dimming cycle to temporarily disable the fault protection circuitry. The blanking interval is active when V(SSC) < 3.0 volts. (See application notes.)
4	RDELTA	A resistor connected from this pin to VDD determines the amount that the voltage at FCOMP modulates the switching frequency. The frequency is inversely proportional to the voltage at FCOMP.
5	SSC1ST	A capacitor added between this pin and SSC is used to define the one second initial start up period. SSC1ST is connected to VSS for the start up period and floats for subsequent periods.
6	RT2	A resistor from this pin to VSS sets the minimum frequency of the VCO. The voltage at this pin is 1.5V
7	VSS	Negative supply. Connect to system ground.
8	OVPH	Over voltage protection input (HIGH). Indirectly senses the voltage at the secondary of the transformer through a resistor (or capacitor) divider. During the initial start up period, if OVPH is > 3.3V, FCOMP is driven towards VSS (increasing the frequency) and SSV is reset to zero (which decreases the duty cycle). After the initial start up period is completed the circuit will shut down if OVPH is > 3.3V.
9	OVPL	Over voltage protection input (LOW). During the initial start up period if OVPL < 2.5 volts then FCOMP is allowed to ramp up (decreasing the oscillator frequency allowing the circuit to get closer to resonance). If, during the initial start up period, OVPL > 2.5 volts then FCOMP is held at its original value (not allowed to increase so the oscillator frequency stays constant). This action is designed to hold the voltage across the CCFL constant while the CCFL "warms up".
10	FCOMP	Frequency control point. Initially this pin is at VSS which yields a maximum switching frequency. Depending on the voltage at OVPL and OVPH the pin FCOMP will normally ramp upwards lowering the switching frequency towards the circuit's resonant frequency.

■ Pin Description

Pin #	Pin Name	Pin Description
11	CSDET	Current sense detect. Connect this pin to the CCFL current sense resistor divider. During the initial startup period this pin senses that the CCFL has struck when V(CSDET) > 1.25 volts. If, after the initial start up period, this pin is below 1.25V for 8 consecutive clock cycles after SSC > 3V then the circuit will shutdown.
12	BATTFB	UVLO feedback pin. If this pin is above 1.5V then the OUTA pin is allowed to switch, if below 1.25V then OUTA is disabled.
13	OUTC	Drives one of the external NFETs, opposite phase of OUTAPB.
14	OUTAPB	Drives one of the external NFETs, opposite phase of OUTC.
15	OUTA	Drives the high side PFET.
16	VBATT	Battery input. This is the positive supply for the OUTA driver.
17	BRPOL	Brightness polarity control. When this pin is low the CCFL brightness increases as the voltage at the BRIGHT pin increases. When this pin is high the CCFL brightness **decreases** as the voltage at the BRIGHT pin increases.
18	VDD	Regulated 5V supply input.
19	CT1	Sets the dimming cycle frequency. Usually about 100Hz.
20	FB	Negative input of the voltage control loop error amplifier.
21	COMP	Output of the voltage control loop error amplifier.
22	BRIGHT	Brightness control input. A DC voltage on this controls the duty cycle of the dimming cycle. This pin is compared to a 3V ramp at the CT1 pin. Analog brightness control may be accomplished by small modifications to the external circuitry.
23	SSV	Soft start ramp for the voltage control loop. (20uA source current.) The voltage at SSV clamps the voltage at COMP to be no greater than SSV thereby limiting the increase of the switching duty cycle.
24	PNP	Drives the base of an external PNP transistor used for the 5V LDO.

■ Ordering Information



Pin Configuration	Operating Temperature Range	Package Type	Number of Pins	Special Feature
A: 1 . VREF 2 . CE 3 . SSC 4 . RDELTA 5 . FAULTB 6 . RT2 7 . VSS 8 . OVPH 9 . OVPL 10. FCOMP 11. CSDET 12. BATTFB 13. OUTC 14. OUTAPB 15. OUTA 16. VBATT 17. BRPOL 18. VDD 19. CT1 20. FB 21. COMP 22. BRIGHT 23. SSV 24. PNP	E: -40°C to 85°C	J: SOIC (300 mil) P: Plastic DIP T: QSOP	H: 24	Z: Lead free

■ Ordering Information (contd.)

Part Number	Marking*	Output Voltage	Package	Operating Temp. Range
AME9003AETH	AME9003AETH xxxxxxxx yyww	N/A	QSOP-24	- 40°C to + 85°C
AME9003AETHZ	AME9003AETH xxxxxxxx yyww	N/A	QSOP-24	- 40°C to + 85°C
AME9003AEPH	AME9003AEPH xxxxxxxx yyww	N/A	PDIP-24	- 40°C to + 85°C
AME9003AEPHZ	AME9003AEPH xxxxxxxx yyww	N/A	PDIP-24	- 40°C to + 85°C
AME9003AEJH	AME9003AEJH xxxxxxxx yyww	N/A	SOIC-24	- 40°C to + 85°C
AME9003AEJHZ	AME9003AEJH xxxxxxxx yyww	N/A	SOIC-24	- 40°C to + 85°C

Note: yyww represents the date code
* A line on top of the first letter represents lead free plating such as $\overline{\text{A}}$ME9003
Please consult AME sales office or authorized Rep./Distributor for the availability of output voltage and package type .

■ Absolute Maximum Ratings

Parameter	Maximum	Unit
Battery Voltage (VBATT)	25	V
Enable	5.5	V
ESD Classification	B	

Caution: Stress above the listed absolute maximum rating may cause permanent damage to the device

■ Recommended Operating Conditions

Parameter	Rating	Unit
Battery Voltage (VBATT)	7 - 24	V
Ambient Temperature Range	- 40 to + 85	^{o}C
Junction Temperature	- 40 to + 125	^{o}C

■ Thermal Information

Parameter	Maximum	Unit
Thermal Resistance (QSOP - 24)	325	^{o}C / W
Maximum Junction Temperature	150	^{o}C
Maximum Lead Temperature (10 Sec)	300	^{o}C

■ Electrical Specifications

TA= 25°C unless otherwise noted, VBATT = 15V, CT1 = 0.047uF, RT2 = 56K

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
5V supply (VSUPPLY)						
Output voltage	V_{DD}		4.9	5.15	5.35	V
Line regulation	V_{DDLINE}	7<Vbatt<24	-0.5		0.5	%
Load regulation	V_{DDLOAD}	Vbatt=7V, 0mA < Iload < 25mA	-0.2		0.2	%
Temperature drift	V_{DDTC}	-10C < Ta < 70C		0.5		%
3.4V reference (VREF)						
Initial voltage	V_{REF}	Vbatt = 15V, Iref = 0	3.3	3.4	3.5	V
Line regulation	$V_{REFLINE}$	7< Vbatt < 24V	-0.1		0.1	%
Temperature drift	V_{REFTC}	-10C <Ta < 70C		100		ppm/C
Brightness oscillator (CT1, BRIGHT)						
Full Scale Brightness Threshold	$V_{CT1,HIGH}$		2.9		3.1	V
Zero Scale Brightness Threshold	$V_{CT1, LOW}$		0		100	mV
Frequency Accuracy	F_{CT1}		70		130	Hz
Frequency Range	F_{CT1}	Note 1	10		1000	Hz
Line regulation	$LINE_{CT1}$	7< Vbatt < 24V	-1		1	%
Temperature drift	TC_{CT1}	-10C < Ta < 70C		=+-3		%
Comparator offset	VOS_{CT1}			10		mV
Vco oscillator (RT2, RDELTA)						
Initial frequency	$F_{VCO(OUTA)}$	Note 2	47		52	kHz
Line regulation	$LINE_{VCO}$	7< Vbatt < 24V	-0.8		0.8	%
Temperature drift	TC_{VCO}	-10C < Ta < 70C		+-1.5		%
VCO pullin range	$PULL_{VCO}$		RT2/(RDELTA X 5)			%
Error amplifiers (FB, COMP)						
Offset voltage, WRT Vref	V_{OS}			50		mV
Input bias current	I_B			1		nA
Input offset current	I_{OS}			1		nA
Open loop gain	A_{OL}			70		dB
Unity gain frequency	F_T			1		Mhz
Output high voltage (comp)	V_{OH}	I_{SOURCE} = 50uA	3.32			V
Output low voltage	V_{OL}	I_{SINK} = 500uA			0.4	V
COMP 100% Duty	V_{COMP}			3		V
COMP 0% Duty	V_{COMP}			0		V

■ Electrical Specifications(contd.)

TA= 25°C unless otherwise noted, VBATT = 15V, CT1=0.047uF, RT2 = 56K

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output A (OUTA)						
Peak current	I_{PEAKA}			1		Amp
Output Low Voltage	V_{OL}	0.2mA			10.55	V
Output High Voltage	V_{OH}	-5mA	14.4			V
Other outputs (OUTAPB, OUTC)						
Peak current	I_{PEAKBC}			1		Amp
Output Low Voltage	V_{OL}	I_{SINK} = 10mA			0.25	V
Output High Voltage	V_{OH}	I_{SOURCE} = 10mA	VDD - .7			V
Soft start clamps (SSC, SSV)						
Initial SSC current	$I_{SSCINIT}$	Note 3	1.0	1.3	1.6	uA
Normal SSC current	I_{SSC}		200	250	350	uA
SSV current	I_{SSV}	Both source and sink	7	10	13	uA
SSV Operation Range	V_{SSV}		0		5.5	V
Other parameters						
CE high threshold	CE_{HIGH}		1.5			V
CE low threshold	CE_{LOW}				0.4	V
OVPH threshold	OVP_{HI}		3.2	3.3	3.55	V
OVPL threshold	OVP_{LO}		2.3	2.5	2.7	V
CSDET threshold	V_{THCS}		1.2	1.25	1.35	V
FCOMP charging current	I_{FCOMP}		8	10	12	uA
FCOMP operating range	V_{FCOMP}	R=1 Mega Ohm	0		5	V
BATTFB high threshold	$V_{THBATHI}$		1.4	1.5	1.6	V
BATTFB low threshold	$V_{THBATLO}$		1.15	1.25	1.35	V
Average supply current	I_{BATT}	No FET gate current		2.5	6	mA
Average off current	I_{OFF}	In the application			10	uA
BRPOL high threshold	$BROPOL_{HIGH}$		4.5	5		V
BRPOL low threshold	$BROPOL_{LOW}$				0.5	V

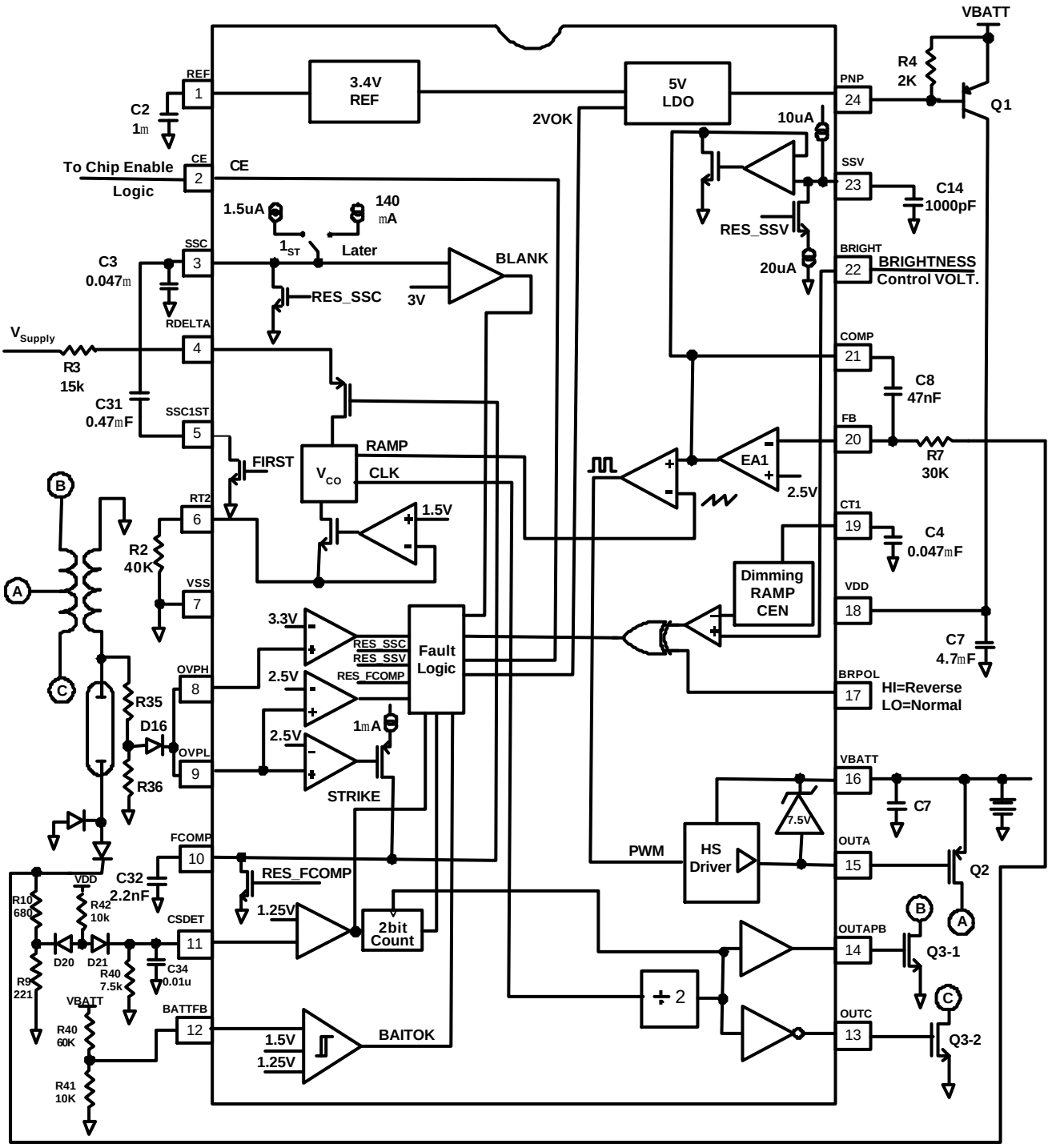
Note1: $F = \frac{1}{4xR2xC11}$

Note2: RDELTA=200kΩ, FCOMP=0

Note3: $T=(C3+C31) \cdot \frac{3V}{1.3uA}$

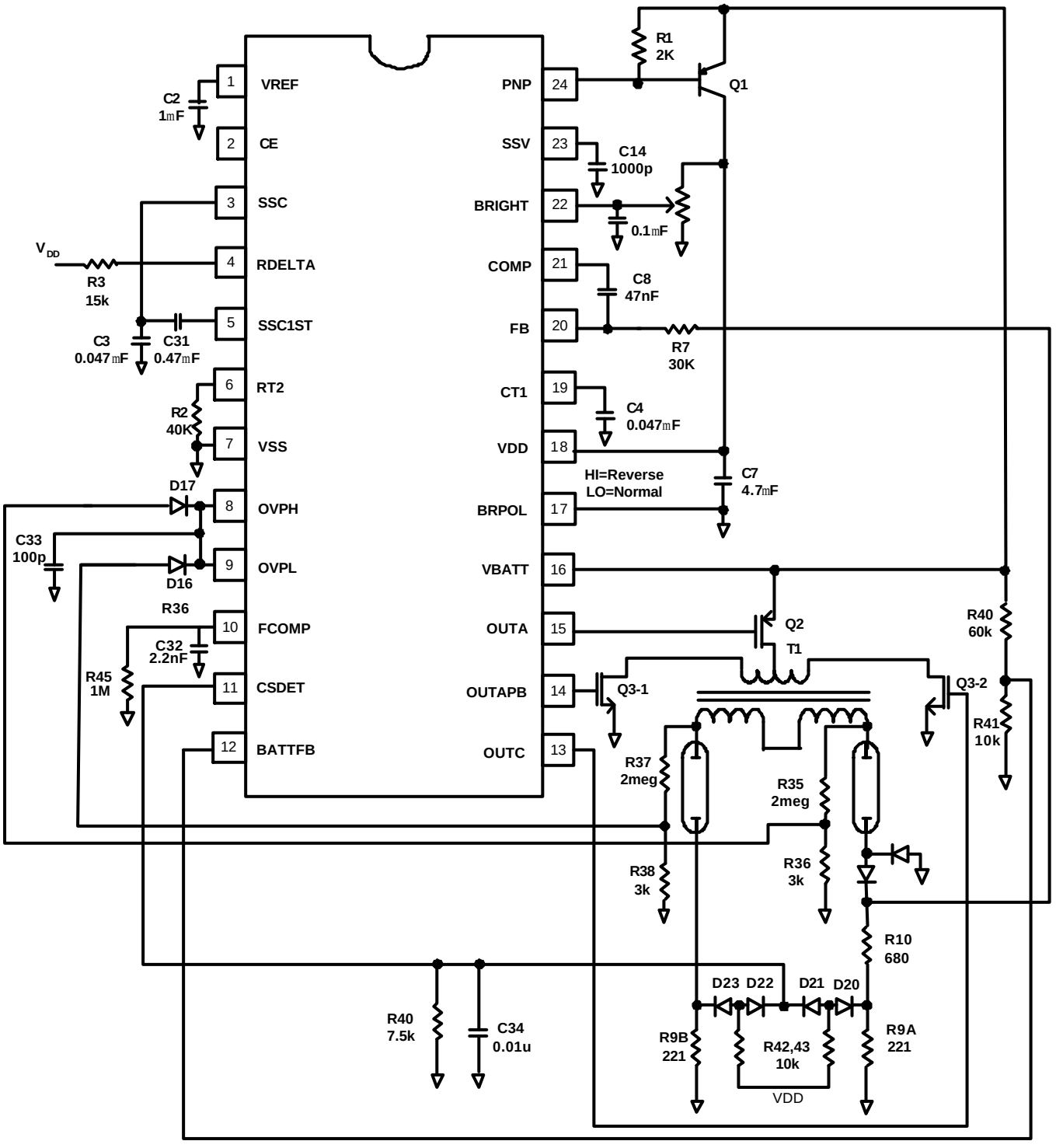
■ Block Diagram

Figure 1



■ Application Schematic

Figure 2. Double Tube Application Schematic (7V < Vbatt < 24V)



■ Application Notes

Overview

The AME9003 application circuit drives a CCFL (cold cathode fluorescent lamp) with a high voltage sine wave in order to produce an efficient and cost effective light source. The most common application for this will be as the backlight of either a notebook computer display, flat panel display, or personal digital assistant (PDA).

The CCFL tubes used in these applications are usually glass rods that can range from several cm to over 30cm and 2.5mm to 6mm in diameter. Typically they require a sine wave of 600V and they run at a current of several milliamperes. However, the starting (or striking) voltage can be as high as 2000V. At start up the tube looks like an open circuit, after the plasma has been created the impedance drops and current starts to flow. The starting voltage is also known as the striking voltage because that is the voltage at which an arc "strikes" through the plasma. The IV characteristic of these tubes is highly non-linear.

Traditionally the high voltage required for CCFL operation has been developed using some sort of transformer - LC tank circuit combination driven by several small power mosfets. The AME9003 application uses one external PMOS, 2 external NMOS and a high turns ratio transformer with a centertapped primary. Lamp dimming is achieved by turning the lamp on and off at a rate faster than the human eye can detect, sometimes called "duty cycle dimming". These "on-off" cycles are known as dimming cycles. Alternate dimming schemes are also available.

Steady State Circuit Operation

Figure 1 shows a block diagram of the AME9003. Throughout this datasheet like components have been given the same designations even if they are on a different figure. The block diagram shows PMOS Q2 driving the center tap primary of T1. The gate drive of Q2 is a pulse width modulated (PWM) signal that controls the current into the transformer primary and by extension, controls the current in the CCFL. The gate drive signal of Q2 drives all the way up to the battery voltage and down to 7.5 volts below Vbatt so that logic level transistors may be used without their gates being damaged. An internal clamp prevents the Q2 gate drive (OUTA) from driving lower than Vbatt-7.5V.

NMOS transistors Q3-1 and Q3-2 alternately connect the outside nodes of the transformer primary to VSS. These transistors are driven by a 50% duty cycle square wave at one-half the frequency of the drive signal applied to the gate of Q2.

Figure 3 illustrates some ideal gate drive waveforms for the CCFL application. Figure 4 and 5 are detailed views of the power section from Figures 1 and 2. Figure 5 has the transformer parasitic elements added while Figure 4 does not. Referring to Figures 4 and 5, NMOS transistors Q3-1 and Q3-2 are driven out of phase with a 50% duty cycle signal as indicated by waveforms in Figure 3. The frequency of the NMOS drive signals will be the frequency at which the CCFL is driven. PMOS transistor, Q2, is driven with a pulse width modulated signal (PWM) at twice the frequency of the NMOS drive signals. In other words, the PMOS transistor is turned on and off once for every time each NMOS transistor is on. In this case, when NMOS transistor Q3-1 and PMOS transistor Q2 are both on then NMOS transistor Q3-2 is off, the side of the primary coil connected to NMOS transistor Q3-1 is driven to ground and the centertap of the transformer primary is driven to the battery voltage. The other side of the primary coil connected to NMOS transistor Q3-2 (now "off") is driven to twice the battery voltage (because each winding of the primary has an equal number of turns).

Current ramps up in the side of the primary connected to Q3-1 (the "on" transistor), transferring power to the secondary coil of transformer. The energy transferred from the primary excites the tank circuit formed by the transformer leakage inductance and parasitic capacitances that exist at the transformer secondary. The parasitic capacitances come from the capacitance of the transformer secondary itself, wiring capacitances, as well as the parasitic capacitance of the CCFL. Some applications may actually add a small amount of parallel capacitance (~10pF) on the output of the transformer in order to dominate the parasitic capacitive elements.

When the PMOS, Q2, is turned off, the voltage of the transformer centertap returns to ground as does the drain of NMOS transistor Q3-2 (the drain of Q3-2 was at twice the battery voltage). Halfway through one cycle, NMOS transistor Q3-1 (that was on) turns off and NMOS transistor Q3-2 (that was off) turns on. At this point, PMOS transistor Q2 turns on again, allowing current to ramp up in the side of the primary that previously had no current. Energy in the primary winding is transferred to the secondary winding and stored again in the leakage inductance L_{leak}, but this time with the opposite polarity. The current alternately goes through one primary winding then the other.

The duty cycle of PMOS transistor Q2 controls the amount of power transferred from the primary winding to the secondary winding in the transformer. Note that the CCFL circuit can work with PMOS transistor Q2 on con-

Figure 3. Idealized Gate Drive Waveforms

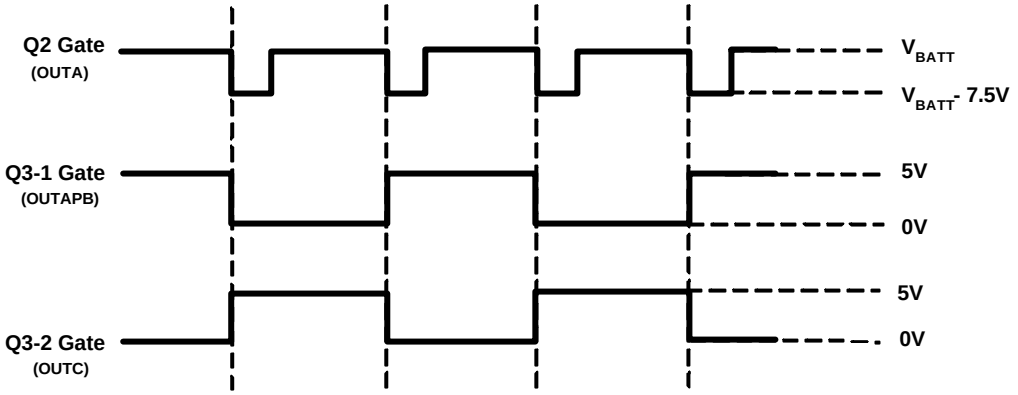


Figure 4.
Power Stage Single Tube Components
(Same component designations used throughout)

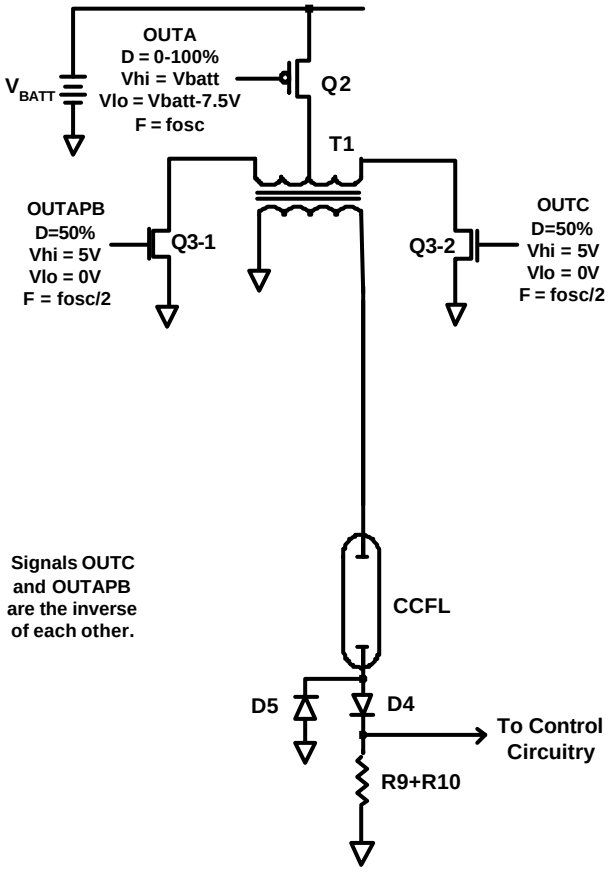
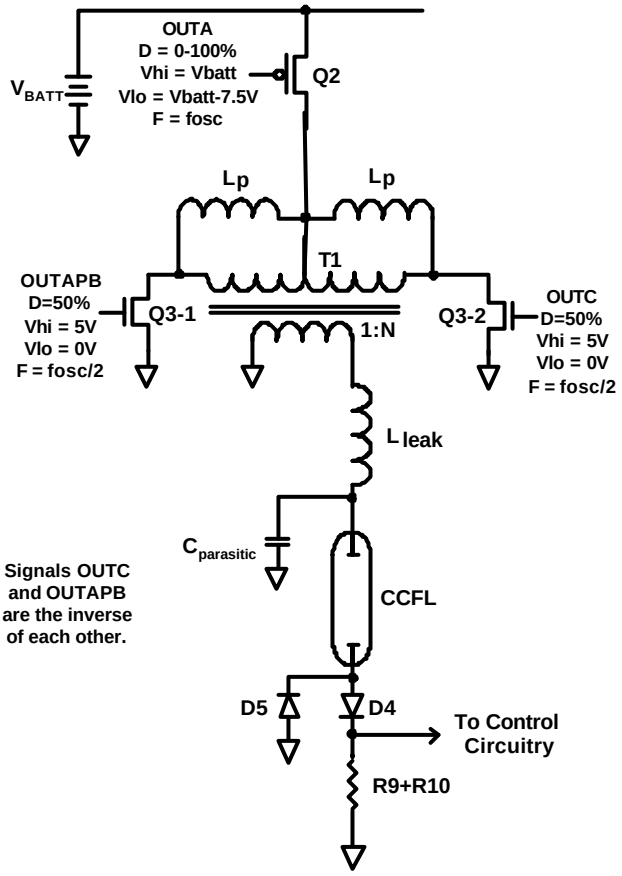


Figure 5.
Power Stage Single Tube Components with parasitic elements
(Same component designations used throughout)



stantly (i.e. a duty cycle of 100%), although the power would be unregulated in this case.

Figures 6,7 illustrates various oscilloscope waveforms generated by the CCFL circuit in operation. These figures show that the duty cycle of the gate drive at Q2 decreases as the battery voltage increases from 9 V to 21 V (as one would expect in order to maintain the same output power).

The first three traces in Figures 6 and 7 show the gate drive waveforms for transistors Q2, Q3-1, and Q3-2, respectively. As mentioned before, the gate drive waveform for transistor Q2 drives up to the battery voltage but down only to approximately 7.5 V below the battery voltage. The fourth trace (in Figures 6,7) shows the voltage at centertap of the primary winding (it is also the drain of PMOS transistor, Q2). This waveform is essentially a ground to a battery voltage pulse of varying duty cycle. When the centertap of the primary is driven high, current increases through PMOS transistor, Q2 as indicated by the sixth trace down from the top. In region I the drain current of Q2 is equal and opposite to the drain current of Q3-1 since the gate of Q3-1 is high and Q3-1 is on. In region III the drain current of Q2 will be equal and opposite to the drain current of Q3-2 (not shown). In region II when PMOS transistor Q2 is switched off, the current through this transistor, after an initial sharp drop, ramps back down towards zero.

In Figures 6 and 7 the fifth trace down from the top shows the drain voltage of Q3-1. (The trace for NMOS transistor Q3-2, not shown, would be identical, but shifted in time by half a period.) The seventh trace down from the top shows the current through the NMOS transistor Q3-1, which is equal to the current in PMOS transistor Q2 for the portion of time that PMOS transistor Q2 is conducting (see region I, for example). As the current ramps up in the primary winding, energy is transferred to the secondary winding and stored in the leakage inductance L_{leak} (and any parasitic capacitance on the secondary winding). If the current in the NMOS transistor is close to zero when that NMOS transistor is turned off that means that the CCFL circuit is being driven close to its resonant frequency. If the circuit is being driven too far from its resonant point then there will be large residual currents in the transistors when they are turned off causing large ringing, lower efficiency and more stress on the components. So called "soft switching" is achieved when the MOS drain current is zero while the MOS is being turned off. The driving frequency and transformer parameters should be chosen so that soft switching occurs.

Once PMOS transistor Q2 completes one on/off cycle, it is repeated again with the alternate NMOS transistor conducting. This complementary operation produces a symmetric, approximately sinusoidal waveform at the input to the CCFL load, as shown by the bottom trace in Figures 6 and 7.

The operation of the CCFL circuit can be divided into 4 regions (I, II, III, and IV) as shown in Figures 6 and 7. Figure 8-1 shows the equivalent transformer and load circuit model for region I. During region I, one of the primary windings is connected across the battery, the current in that winding increases and energy is coupled across to the secondary. No current flows in the other winding because its NMOS is turned off and its body diode is reverse biased. The drain of that NMOS stays at twice the battery voltage because both primary windings have the same number of turns and the battery voltage is forced across the other primary winding.

Figure 8-2 shows the equivalent transformer and load circuit model for region II. During region II, the battery is disconnected from the primary winding. In this configuration, current flows through both of the primary windings. The current decreases very quickly at first then ramps down to zero at a rate that is slower than the current ramped up. The initial drop is due to the almost instantaneous change in inductance when current flow shifts from one portion of the primary winding to both portions of the primary.

Figure 8-3 shows the equivalent transformer and load circuit model for region III. During region III, the primary winding opposite from the one used in region I is connected across the battery, increasing current in that primary winding but in a direction opposite to that of region I. Energy is coupled across to the secondary as in region I but with opposite polarity. No current flows in the undriven winding because its NMOS is turned off and its body diode is reverse biased. The drain of that NMOS stays at twice the battery voltage because both primary windings have the same number of turns and the battery voltage is forced on the other primary. Region III is, effectively, the inverse of region I.

Figure 8-4 shows the equivalent transformer and load circuit model for region IV. During region IV, the battery is disconnected from the primary winding. In this configuration, current flows through both of the primary windings with opposite polarity to that in region II. The current decreases very quickly at first then ramps down to zero at a rate that is slower than the current ramped up. Once again, the initial drop is due to the effective change in inductance when current flow shifts from one portion of the primary winding to both portions of the primary. Region IV is effectively the inverse of region II.

Figure 6. Typical Waveforms V_{BATT}=9V

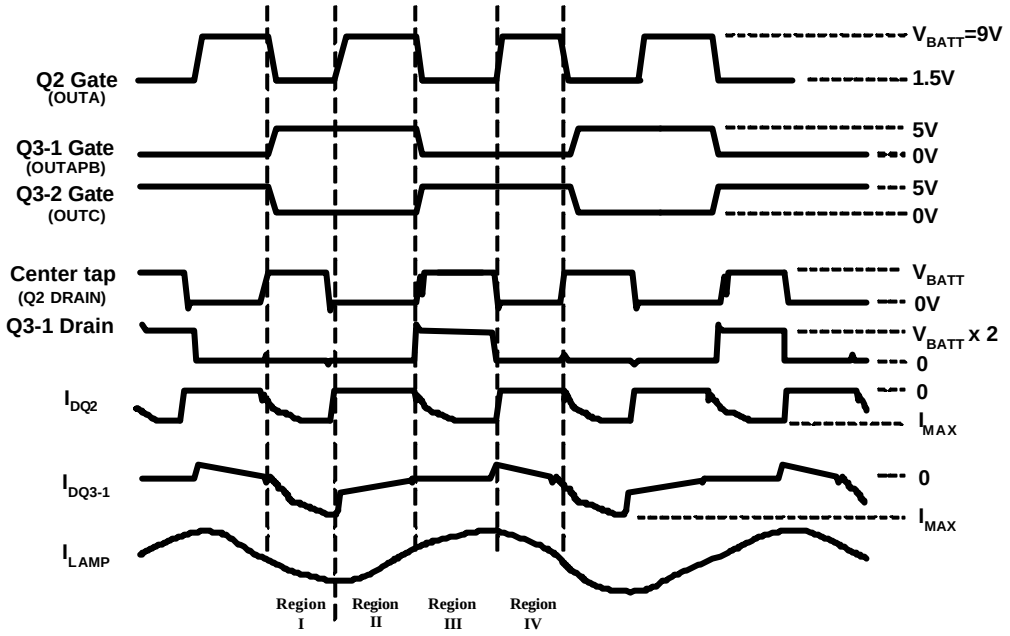


Figure 7. Typical Waveforms V_{BATT}=21V

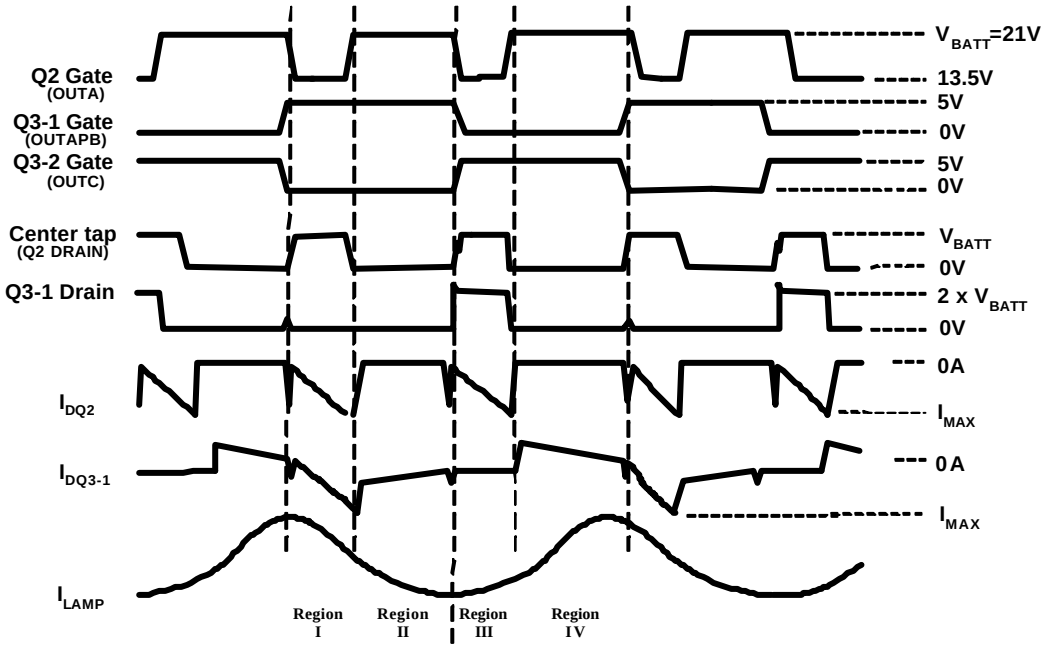


Figure 8-1. Region I

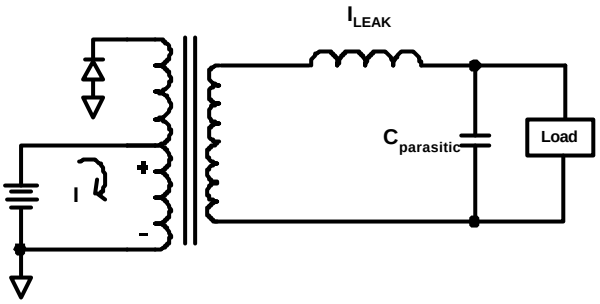


Figure 8-2. Region II

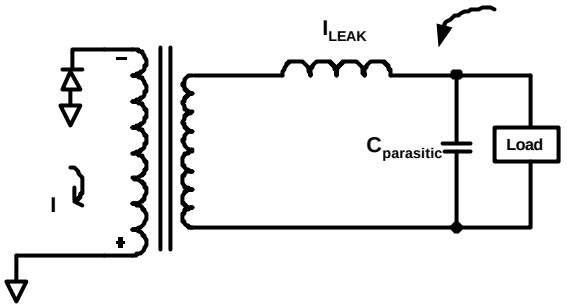


Figure 8-3. Region III

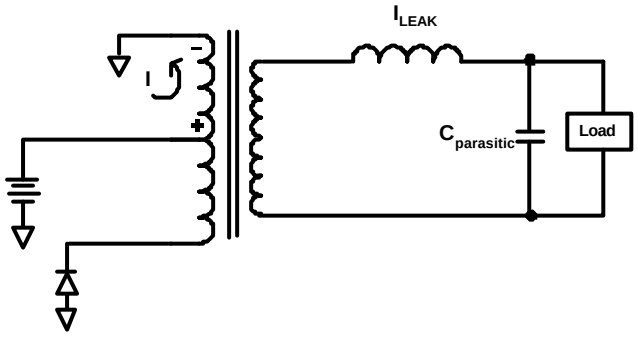


Figure 8-4. Region IV

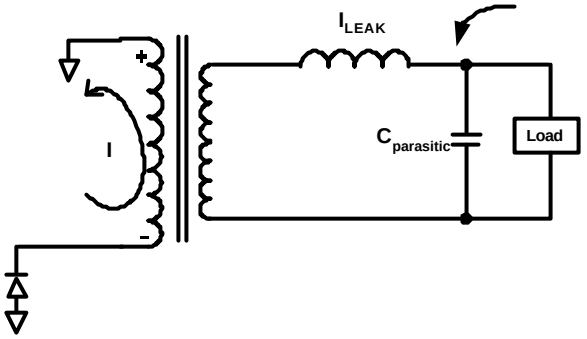
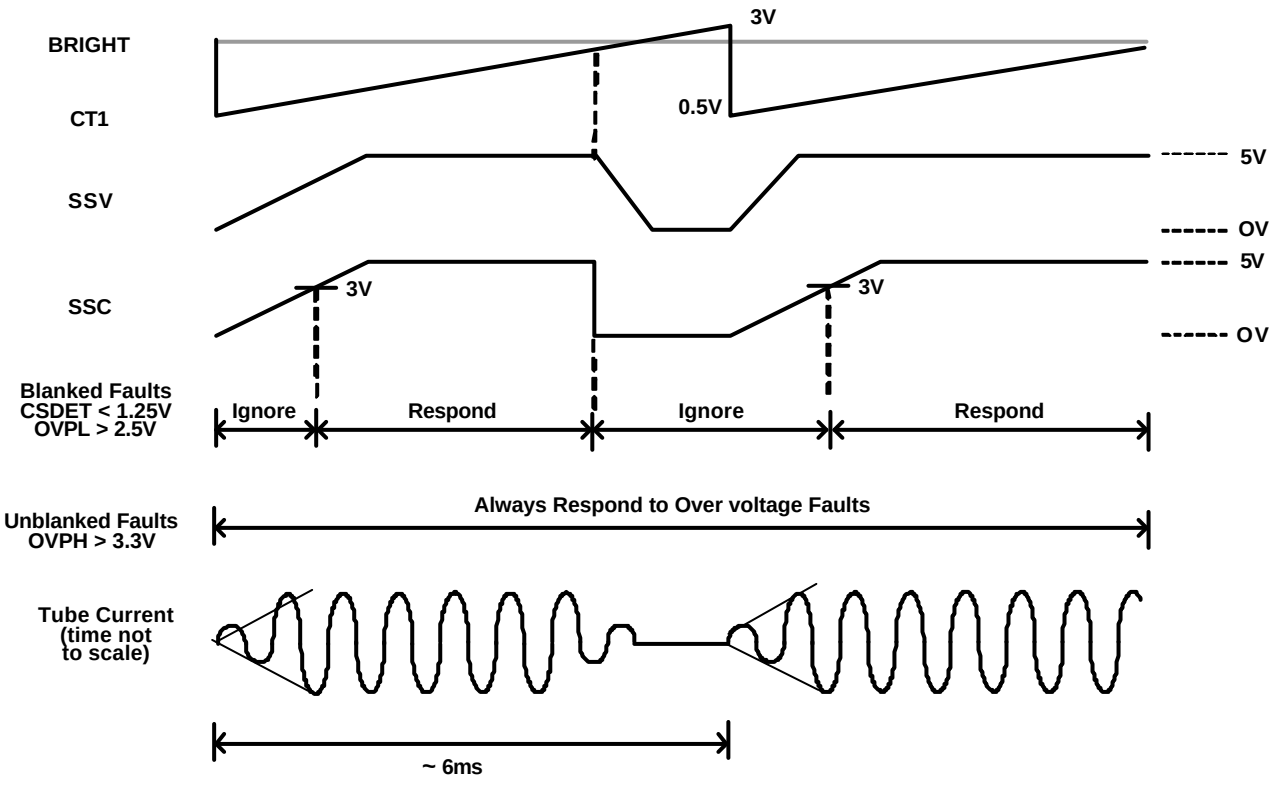


Figure 9. Steady State Dimming Waveforms (after initial start up period)



Driving the CCFL

Unlike modified Royer schemes for driving CCFLs the secondary winding of the AME9003 method is not designed to look like a voltage source to the CCFL lamp. The circuit acts more like a current source (or a power source). The voltage at the transformer secondary is primarily determined by the operating point of the CCFL. The circuit will increase the duty cycle of Q2 thereby dumping more and more energy across to the secondary tank circuit until the CCFL tube current achieves regulation or one of the various fault conditions is met.

There are two major modes of operation of the AME9003. The start up mode consists of the time from intial power up until the tube strikes or 1 second elapses. The steady state mode consists of operation that occurs after the start up mode finishes.

The start up mode is useful for coaxing old or cold tubes into striking. It is believed that as a tube ages it becomes more and more difficult to strike an arc through the gas. Cold temperatures make this problem even worse. The AME9003 will allow higher than normal operating voltages across the CCFL for a period of up to one second in order to facilitate strking. This feature should extend the usable life of the CCFL as well as simplifying start up for "problem" applications.

Start Up Mode

When the circuit is first powered up or the CE pin transitions from a low to a high state a special mode of operation, known as the "start up mode", is initiated that will last for a maximum of one second. The exact duration of the start up period is determined by capacitor C3 and C31 on the SSC pin. Figure 10 shows a flow chart of the CCFL ignition sequence described here. The start up mode will end when one of two conditions is met:

a) The CCFL strikes and the current sense voltage at the CSDET pin rises above 1.25V.

b) The one second time period ends without the tube being struck, in this case the circuit will shut down.

On the first cycle after power on (or a low to high transition on CE) the SSC1ST pin is internally shorted to VSS so C3 and C31 are in parallel. C3 and C31 are initially discharged and the voltage on SSC is zero. C31 and C3 are charged up by a 1.5uA current source. When the voltage at SSC reaches 3 volts the start up mode has ended. A value of 0.47uF for C31 nominally yields a one second start up period. C3 is usually a factor of 10 smaller than C31. If the one second time period ends before the CCFL strikes then the circuit is shutdown until the user toggles the power supply or CE transitions from low to high again. In other words, if the CCFL successfully starts up then the start up time period will end before the one second time period is up.

After the initial startup period pin SSC1ST is internally disconnected from SSV allowing capacitor C31 to float. C3 is now the dominant cap on the SSC pin whereas C31 was the dominant cap during the initial startup period. During steady state operation the SSC pin and C3 are used to set the blanking period. This operation is described more completely below.

At the beginning of the start up period capacitor C32, connected to FCOMP, is also discharged and the voltage at FCOMP is zero. The voltage at FCOMP controls the frequency at which the FETs are driven. When FCOMP is zero the frequency is at its maximum value. When FCOMP reaches 5V then the switching frequency is at its minimum value. The exact relation between the voltage at FCOMP and oscillator frequency is described more fully in the detailed description of the oscillator circuitry.

At the beginning of start up mode FCOMP is zero volts so the switching frequency is at its maximum value. It is intended that this maximum frequency is significantly above the resonant frequency of the tank circuit made up of the transformer and CCFL load. In this way the voltage at the CCFL is lower than would be expected if the circuit was driven nearer to its resonant frequency. At this point in the operation of the circuit we assume that the CCFL has not struck an arc and therefore appears as an open circuit to the transformer. After the tube has struck the voltage at the transformer output is controlled by the IV relationship of the CCFL. Without the variable frequency drive available with the AME9003 the user is unable to control the voltage across the CCFL before the CCFL strikes and current starts flowing in the CCFL.

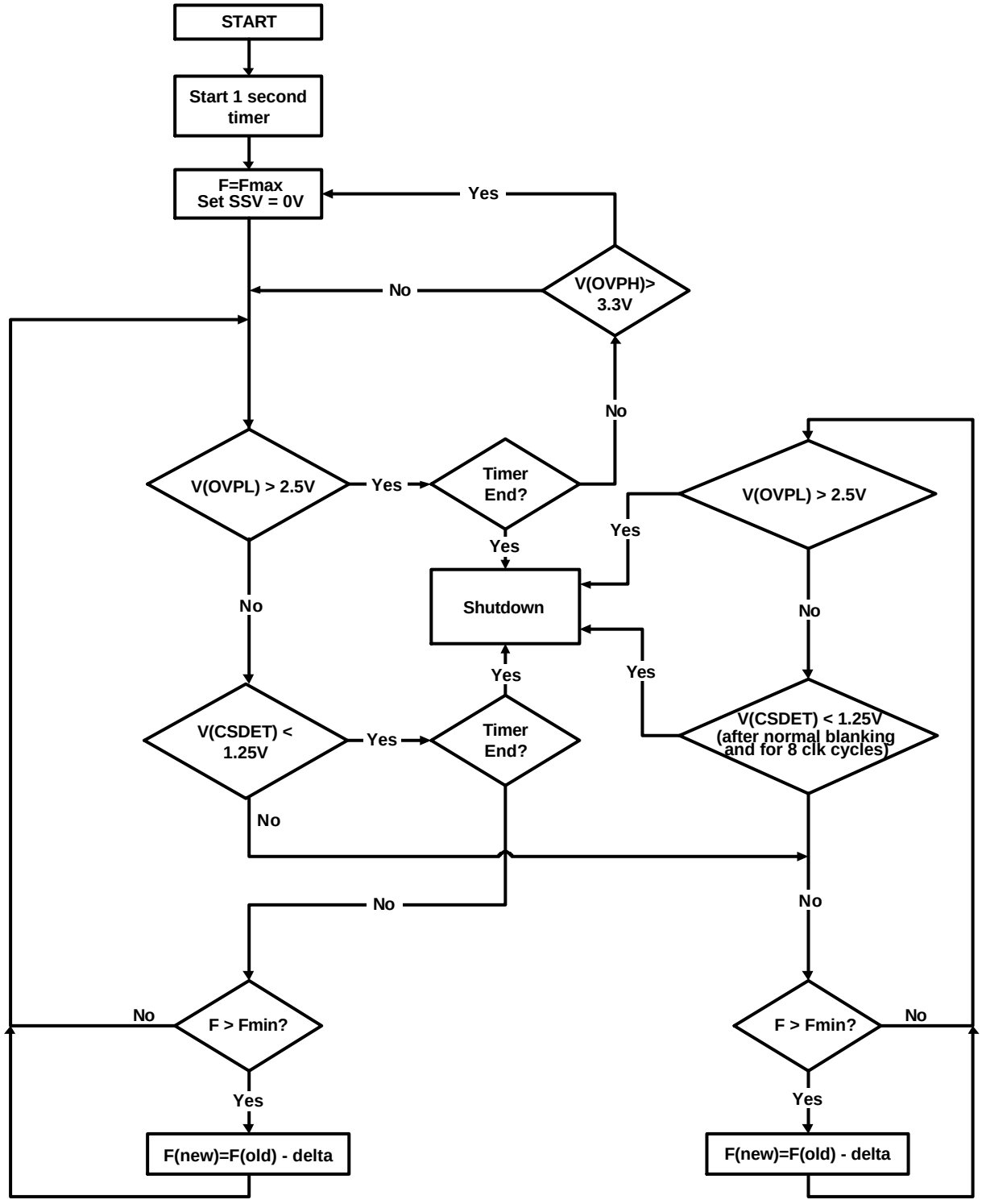
Capacitor C32 is charged by a 1uA current source with the following conditions:

a) If OVPL < 2.5V the charging current is 1uA and the voltage at FCOMP ramps positive.

b) If OVPL > 2.5V and OVPH < 3.3V then the charging current is zero and the voltage at FCOMP remains the same.

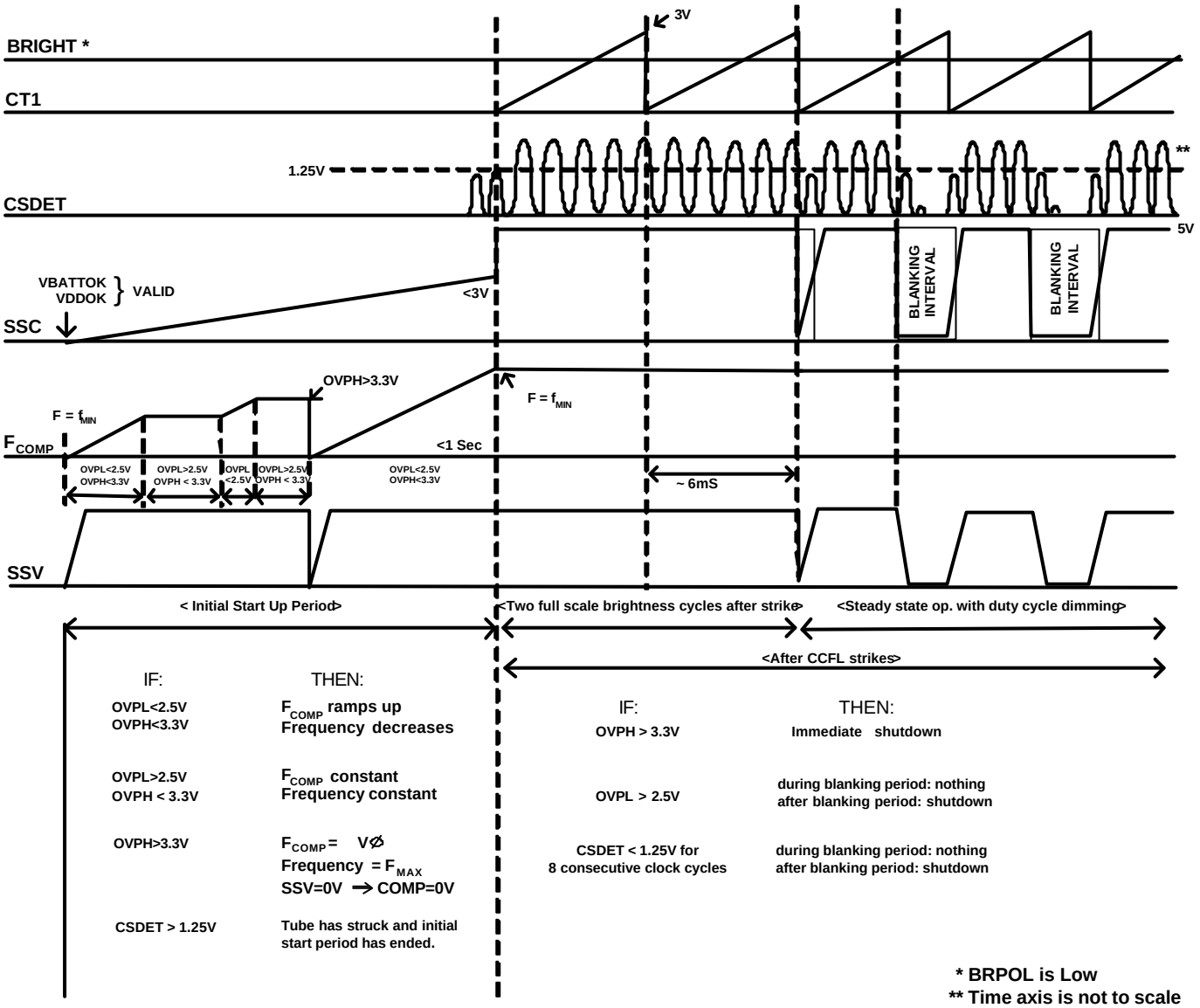
c) If OVPH > 3.3V then FCOMP is discharged to approximately 1V, SSV is also driven to VSS.

Figure 10. Ignition Flow Chart



Start Up Side ------- | ------ Steady State Operation Side

Figure 11. Start Up and Steady State Waveform



* BRPOL is Low
** Time axis is not to scale

These conditions allow the voltage across the CCFL to be controlled during the start up period. The two thresholds available at OVPL and OVPH allow the user to tailor the start behavior for particular tubes.

In Figure 11, initially SSV=SSC=FCOMP= zero volts. The switching duty cycle is zero, the switching frequency is maximum and the one second time period ramp has just started. The SSV ramps positive which allows the switching duty cycle to increase which, in turn, increases the voltage across the CCFL.

At some point later SSV=5 volts, SSC and FCOMP are still ramping up. The tube voltage continues to increase, the switching duty cycle is no longer limited by SSV and is able to go to 100%, if indicated by the error amp loop. The switching frequency continues to decrease forcing the tube voltage higher. If the CCFL voltage is high enough so that OVPL > 2.5V (OVPL senses the CCFL voltage through a resistor or capacitor divider) then FCOMP stops increasing and the frequency remains constant. The frequency will remain constant until:

OVPL < 2.5V

OR....

OVPH > 3.3V (see below)

OR.....

The one second time period runs out and the circuit shuts down.

If the voltage across the tube increases enough so that OVPH > 3.3V (as sensed through a resistor or capacitor divider) then FCOMP is pulled low (~1V), the switching frequency is increased, SSV is pulled low and the switching duty cycle goes to zero. It will remain in this state until:

OVPH < 3.3V

OR....

The one second time period runs out and the circuit shuts down.

Ideally, during one of these states, the CCFL will strike, current will flow in the CCFL and the circuit will move from the start up mode into the steady state mode. Once an arc has struck, as sensed by CSDET > 1.25 volts, then the circuit will drive the CCFL at 100% brightness for approximately two dimming cycles (dimming cycles are on the order of 6mS as determined by the capacitor on CT1) in order to ensure that the CCFL is really "on". After those two full brightness dimming cycles the normal duty brightness control takes over, alternately turning the CCFL on and off at a duty cycle determined by the voltage at the BRIGHT pin.

Remember, the circuit will only "try" to turn on for one second, after that point it gives up and shuts down.

Steady State Mode

At the beginning of each dimming cycle (after the start up mode) there is initially no arc struck in the CCFL. The CCFL load looks like an open circuit. (However an arc has been struck successfully in the start up mode so we assume the gas has "warmed up" and is ready to strike an arc again.) SSV is pulled to zero volts then ramps to 5 volts allowing the duty cycle of the switches to slowly increase to its steady state value. The voltage across the CCFL will increase with each successive clock cycle. Two events may then happen:

1) The gas inside the CCFL will ionize, the voltage across the CCFL will drop, the current through the CCFL will increase, and a stable steady state operating point will be reached.

OR....

2) One of the three fault conditions will be met that shut down the circuit (see Figure 11):
   a) The CCFL tube voltage continues to rise until the OVPH pin is higher than 3.3V at which point the circuit will shut down (immediately).
   b) The CCFL tube voltage continues to rise until the OVPL pin is higher than 2.5V at which point the circuit will shut down (except during the blanking interval).
   c) The CCFL current fails to rise high enough to keep the undercurrent threshold at the CSDET pin from tripping (for 8 consecutive clock cycles).

Note that condition a) can be met at any time while the AME9003 is in steady state operation (after the start up mode). Condition b) can only be met after the SSC pin has risen above 3V (after blanking interval). Condition c) can only be met after the SSC pin has crossed 3V (after blanking interval) AND eight successive undercurrent events occur in a row (CSDET < 1.25V for 8 consecutive clock cycles.).

The SSC pin is pulled to VSS everytime the lamp is turned off, whether for a dimming cycle, user shutdown or fault occurrence. It ramps up slowly depending on the size of capacitor C3 connected to the SSC pin (in steady state mode SSC1ST is high impedance so capacitor C31 has no effect). The period of time when the b) and c) fault checks are disabled is called the blanking? time. The blanking time occurs from the time SSC is pulled to VSS until it reaches 3V. See Figure 9 for some idealized waveforms illustrating the behavior just described.

Control Algorithm

There are 2 major control blocks (loops) within the IC. The first loop controls the duty cycle of the driving waveform. It senses the CCFL current (Figure 1 or 2, resistor R9 and R10) rectifies it, integrates it against an internal reference and adjusts the duty cycle to obtain the desired power. This loop uses error amplifier EA1 whose negative input is pin FB and whose output is COMP. The positive input of EA1 is connected to a 2.5V reference. External components, R7 and C8, set the time constant of the integrator, EA1. In order to slow the response of the integrator increase the value of the product:

(R7 X C8).

The second control block adjusts the brightness by turning the lamp on and off at varying duty cycles. Each time the lamp turns on and off is referred to as a "dimming cycle". At the end of each dimming cycle the SSV pin is pulled low with a 10uA current source, this forces COMP low as well due to the clamping action of Clamp1 shown in Figure 1. At the beginning of a new dimming cycle COMP tries to increase quickly but it is clamped to the voltage at the SSV(soft-start voltage) pin. A capacitor on the SSV pin (C8, Figure 1), which is discharged at the end of every dimming cycle, sets the slew rate of the positive and negative edge of the voltage at the SSV pin, and hence also the maximum positive (and negative) slew rate of the COMP pin. "Dimming cycle" is explained more fully below]

The BRIGHT, CT1 and BRPOL pins

A user-provided voltage at the BRIGHT pin is compared with the ramp voltage at the CT1 pin (See Figure 12). If BRPOL is tied to VSS then as the voltage at BRIGHT increases the duty cycle of the dimming cycle and the brightness of the CCFL increase. If BRPOL is tied to VDD then the brightness of the CCFL diminishes as the BRIGHT voltage increases. The frequency of the dimming cycles is set by the value of the capacitor at pin CT1 (C4 in Figure 1 and 2) and it is also proportional to the current set by resistor R2. Setting C4 equal to 0.047uF and R2 equal to 47.5k yields a dimming cycle frequency of approximately 125Hz. The frequency should vary inversely with the value of C4 according to the relation:

Frequency(Hz) = 1/[4 X R2 X C4]

The brightness may also be controlled by using a variable resistor in place of R10 (See Figure 13). In this case the BRIGHT pin should be pulled to VDD so that the CCFL remains on constantly. This method can lead to flicker at low intensities but it is easy to implement. Harmonic distortion may also increase since the duty cycle of the waveform at the gate of Q2 will vary greatly with brightness. When using burst brightness control the duty cycle of the driving waveforms should not vary because the CCFL is running at 100% power or it is turned off. As long as the battery voltage does not change the duty cycle of the driving waveform also does not change greatly. This means that harmonic distortion can be minimized by optimizing the frequency and transformer characteristics for a particular duty cycle rather than a large range of duty cycle.

Figure 12. Duty Cycle Dimming

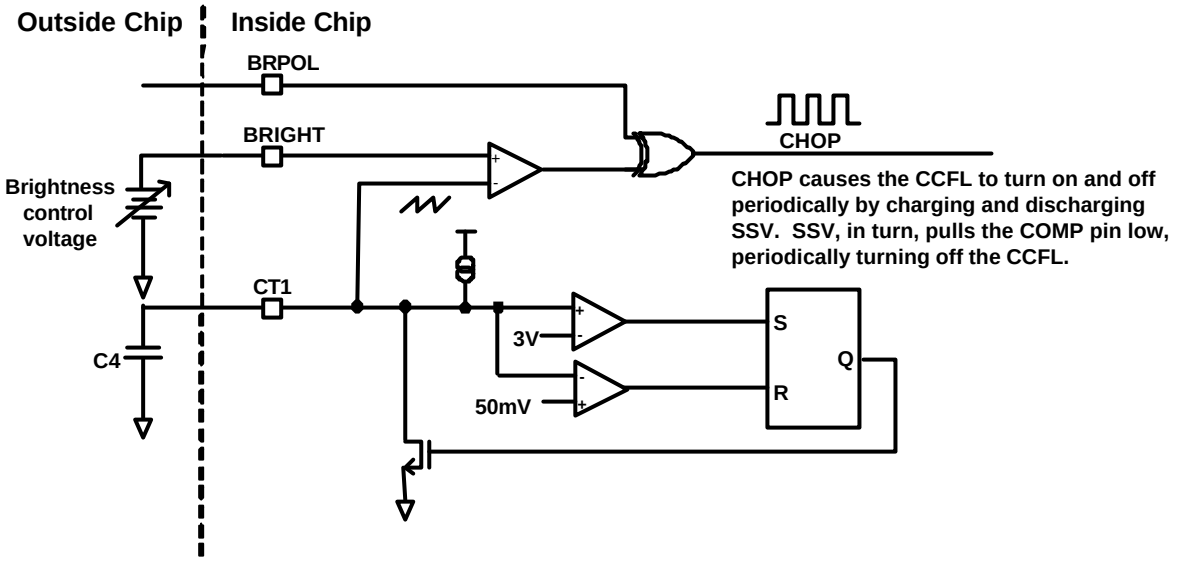
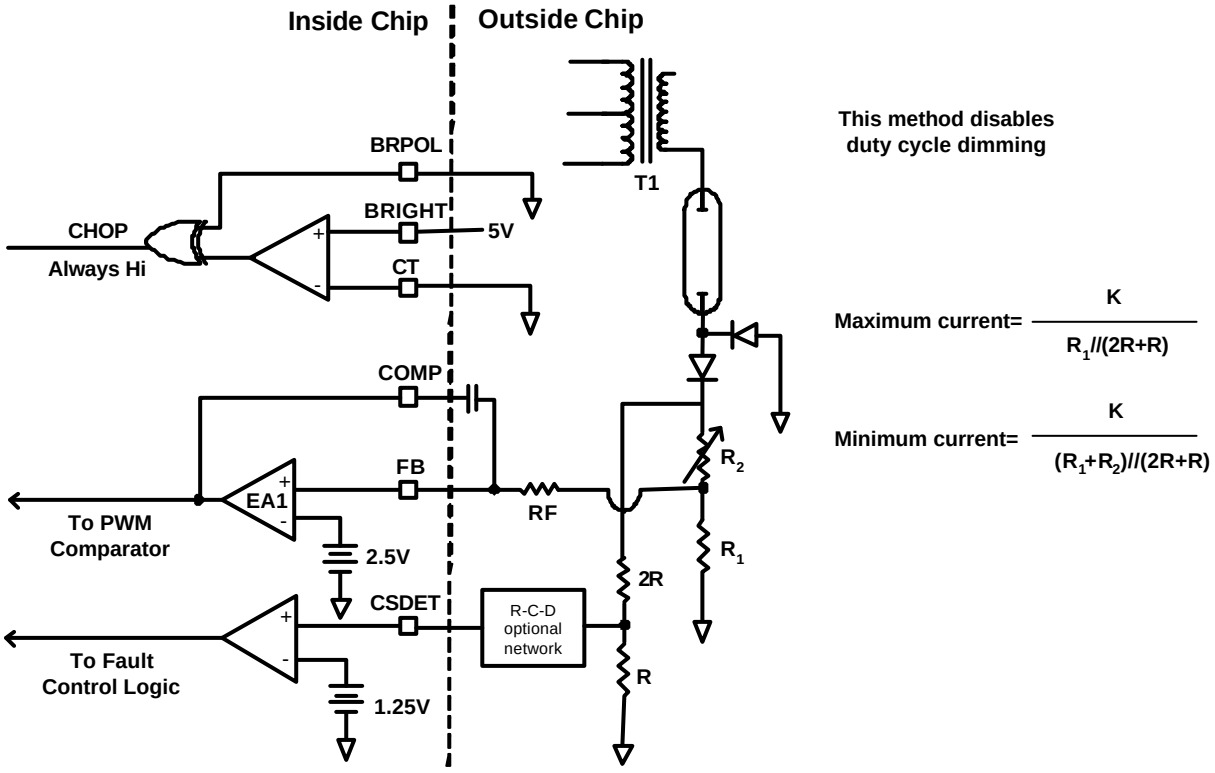


Figure 13. Alternative Brightness Control



RT2, RDELTA pin

The frequency of the drive signal at the gate of Q2 is determined by the VCO shown in Figure1. A detail of the VCO is shown in Figure 14. The user sets the minimum oscillator frequency with the resistor connected to pin RT2 (R2 in the figures). The relation is:

Frequency (Hz) = 2.8E9 / R2 (ohms)

You can see from the formula that as R2 is increased the frequency gets smaller.

Resistor R3 controls how much the oscillator frequency increases as a function of the voltage at FCOMP. The relationship is:

Delta frequency (Hz) = 3.44E8 * (5 - V(FCOMP)) / R3

You can see from the formula that the frequency will decrease as the FCOMP voltage increases. The amount of this increase is set by R3. The current in R3 decreases as the voltage at FCOMP increases and hence decreases the charging current into the timing capacitor of Figure 14 thereby decreasing the oscillator frequency.

Supply voltage pins, VDD and PNP

Most of the circuitry of the AME9003 works at 5V with the exception of one output driver. That driver (OUTA) and its power pad (VBATT) must operate up to 24V although the OUTA pad may never be forced lower than 8 volts away from the VBATT pin. The OUTA pin is internally clamped to approximately 7.5 volts below the Vbatt pin.

The AME9003 uses an external PNP device to provide a regulated 5V supply from the battery voltage (See Figure 15). The battery voltage can range from 7V< VBATT < 24V. The PNP pin drives the base of the external PNP device, Q1. The VDD pin is the 5V supply into the chip. A 4.7uF capacitor, C7, bypasses the 5V supply to ground. If an external 5V supply is available then the external PNP would not be necessary and the PNP pin should float.

When the CE pin is low (<0.4V) the chip goes into a zero current state. The chip puts the PNP pin into a high impedance state which shuts off Q1 and lets the 5V supply collapse to zero volts. When low, the CE pin also immediately turns PMOS transistor Q2 off, however transistors Q3-1 and Q3-2 will continue to switch until the 5V has collapsed to 3.5V. By allowing the Q3 transistors to continue to switch for some time after Q2 is turned off the energy in the tank circuit is dissipated gradually without any large voltage spikes.

The VDD voltage is sensed internally so that the switching circuitry will not turn on unless the VDD voltage is larger than 4.5V and the internal reference is valid. Once the 4.5V threshold has been reached the switching circuitry will run until VDD is less than 3.5V (as mentioned before).

Output drivers (OUTA, OUTAPB, OUTC)

The OUTAPB and OUTC pins are standard 5V CMOS driver outputs (with some added circuitry to prevent shoot through current). The OUTA driver is quite different (See Figure 16). The OUTA driver pulls up to VBATT (max 24V) and pulls down to about 7.5 volts below VBATT. It is internally clamped to within 7.5V of VBATT. On each transition the OUTA pad will sink/source about 500mA for 100nS. After the initial 100ns burst of current the current is scaled back to 1mA(sinking) and 12mA(sourcing). This technique allows for fast edge transitions yet low overall power dissipation.

Fault Protection, the OVPH, OVPL and CSDET pins

During the startup mode the AME9003 does not actually sense for fault conditions, instead it uses the voltages at OVPL and OVPH to adjust the operating frequency for a smooth start up. The startup itself (or "strike") is detected when the voltage at CSDET rises above 1.25V. There are no voltages at OVPL, OVPH or CSDET that can cause a fault during the start up mode.

During steady state operation the AME9003 checks for 3 different fault conditions. There are two overvoltage conditions and one undercurrent condition that can cause a fault. When any one of the fault conditions is met then the circuit is latched off. Only a power on reset or toggling the CE pin will restore the circuit to normal operation. (See Figure 17 for a schematic of the FAULT circuitry.)

The first fault condition check can be used to detect overvoltages at the CCFL. Specifically, if the OVPH pin is above 3V then this fault condition is detected. The first fault condition is always enabled, there is no blanking period (except, of course, during the start up period when fault detection is disabled).

The second fault condition checks that the voltage at OVPL is below 2.5V. This protection is disabled while the SSC ramp is below 3V such as during the beginning of every dimming cycle. Again, this check is disabled during the start up period like all the fault checks.

In order to enable the first two fault condition checks then the OVP pin must, indirectly, sense the high voltage at the input of the CCFL. The actual CCFL voltage must be reduced by using either a resistor or capacitor divider such that in normal operation the voltage at OVPL is lower than 2.5V and the voltage at OVPH is lower than 3.3V.

The third fault condition check can be used to monitor the CCFL current. Specifically, it checks whether the voltage at the CSDET pin is higher than 1.25V. If CSDET does not cross its 1.25V threshold once during 8 successive clock cycles then this fault will be triggered. (Remember that the clock frequency is twice as fast as the driving frequency of the CCFL). This protection is disabled while the SSC ramp is below 3V, such as at the beginning of every dimming cycle. This fault check is disabled during the start up mode, as are all the fault checks. This fault condition is used to check that a reasonable minimum amount of current is flowing in the tube.

Figure 17 is a simplified schematic of the fault protection circuitry used in the AME9003. Most of the signals have been previously defined however some need a little explanation. The VDDOK signal is a power OK signal that goes high when the 5V supply (VDD) is valid. The CHOP signal stops the operation of the switching circuitry once every dimming cycle for burst mode brightness control. The output signal, FIRST, is high during the start up mode then is low during subsequent cycles. It causes the SSC pin to initially source 1000 times less current than on subsequent dimming cycles in order to provide the 1 second initial start up period. The NORM signal is an enable signal to the switching circuitry. When it is high the circuit works normally. When it is low the switching circuitry stops.

SSC, SSC1ST and SSV pins

Besides defining the initial 1 second start up period the SSC pin s primary role is to define a time period in which the 2nd and 3rd fault conditions (previously described) are disabled. This period of time is called the blanking interval. During the initial start up period after a power on reset or just after a low to high transition on the CE pin the SSC pin sources 1.5uA into external capacitors, C3 and C31. At this time the SSC1ST pin is connected to VSS through an internal switch so the charging current out of SSC must charge the parallel combination of C3 and C31. For subsequent dimming cycles, after the initial startup period, the SSC pin sources 140uA and the SSC1ST pin is open circuited which means that the 140uA charging current is only being used to charge C3, not C31 resulting in a faster ramp at the SSC pin..

During steady state operation the blanking interval is defined as the time during which V(SSC) < 3V. Once the voltage at SSC crosses 3V the blanking interval is finished and all three fault condition checks are enabled. (The OVPH > 3.3V fault check is always enabled after the initial start up period.) At the beginning of the next dimming cycle the SSC pin is pulled to VSS then allowed to ramp upwards again.

During steady state operation the SSV pin is pulled to ground with a 10uA current source before the beginning of every dimming cycle. As the dimming cycle starts the SSV pin sources 10uA into external capacitor, C14. This creates a 0 to 5 volt ramp at the SSV pin. This ramp is used to limit the duty cycle of the PWM gate drive signal available at the OUTA pin. The SSV pin accomplishes duty cycle limiting by clamping the COMP voltage to no higher than the SSV voltage. Because the magnitude of the COMP voltage is proportional to the duty cycle of the PWM signal at OUTA the duty cycle starts each dimming cycle at zero and slowly increases to its steady state value as the voltage at SSV increases. At the end of the dimming cycle the SSV pin sinks 10uA out of cap C14 which causes the SSV pin to ramp towards zero, which in turn causes COMP to ramp to zero, which limits the duty cycle and ultimately turns off the lamp for that dimming cycle. (Figure 9 shows this operation.)

During the initial start up mode the SSV pin starts at zero volts and ramps up to 5V just as in steady state operation. However, during the start up mode, if OVPH > 3.3V then SSV is pulled to VSS and only allowed to ramp up when OVPH < 3.3V. This action sets the duty cycle back to 0 volts then allows the duty cycle to increase as the SSV voltage increases.

This type of duty cycle limiting is commonly called "soft-start" operation. Soft start operation lessens overshoot on start up because the power increases gradually rather than immediately. Besides ramping up slowly, the SSV pin also ramps down slowly too. This allows for a "soft-finish" as well as a "soft_start". A "soft-finish" is very useful for minimizing audible vibrations that may occur when using duty cycle dimming.

Unlike the SSC pin the current sourced or sunk by the SSV pin remains approximately 10uA during ALL dimming cycles.

BATTFB

The BATTFB pin is designed to sense the battery voltage and enable the pin OUTA. When the voltage at BATTFB is below 1.25 volts then OUTA is disabled, when the voltage at BATTFB is larger than 1.5V then OUTA is enabled. There is 250mV of hysteresis between the turn on and the turnoff thresholds. This pin does not disable any other portion of the circuit except the OUTA pin. Notably, the other two drivers, OUTAPB and OUTC continue to switch when the voltage at BATTFB is below 1.25V.

Ringing

Due to the leakage inductances of transformer T1 voltages at the drains of Q3 can potentially ring to values substantially higher than the ideal value (which is twice the battery voltage). The application schematic in Figure 17 uses a snubbing circuit to limit the extent of the ringing voltage. Components C9,R8,D2 and D3 make up the snubbing circuit. The nominal voltage at the common node is approximately twice the battery voltage. If either of the drains of Q3 ring above that voltage then diodes D2 or D3 forward bias and allow the ringing energy to charge capacitor C9. Resistor R8 bleeds off the extra ringing energy preventing the voltage at the common node from increasing substantially higher than twice the battery voltage. The extra power dissipation is:

$$P(\text{dissipated}) = Vbatt^2 / R8$$

For the example, in Figure 17, the power dissipation of the snubber circuit with Vbatt=15V is 58mW or approximately 1% of the total input power. The value of R8 can be optimized for a particular application in order to minimize dissipated power.

Excessive ringing is usually a sign that the driving frequency is not well matched to the resonant characteristics of the tank circuit. In a well designed application a snubber circuit will not be necessary.

Layout Considerations

Due to the switching nature of this circuit and the high voltages that it produces this application can be sensitive to board parasitics. In fact, one of the advantages, of this design is that the circuit uses the parasitic elements of the application as resonant components, thus eliminating the need for more added components.

Particular care must be taken with the different gounding loops. The best performance has been obtained by using a "star" ground technique. The star technique returns all significant ground paths back to the center of the "star". Ideally we would place the center of the star directly on the VSS pin of the AME9003. The bypass capacitors would, ideally, be connected as close to the center of the star as possible. The schematic in Figure 18 attemps to show this star ground configuration by bringing all the ground returns back to the same point on the drawing. Separate ground returns back to the star are especially important for higher current switching paths.

Figure 14. VCO Detail

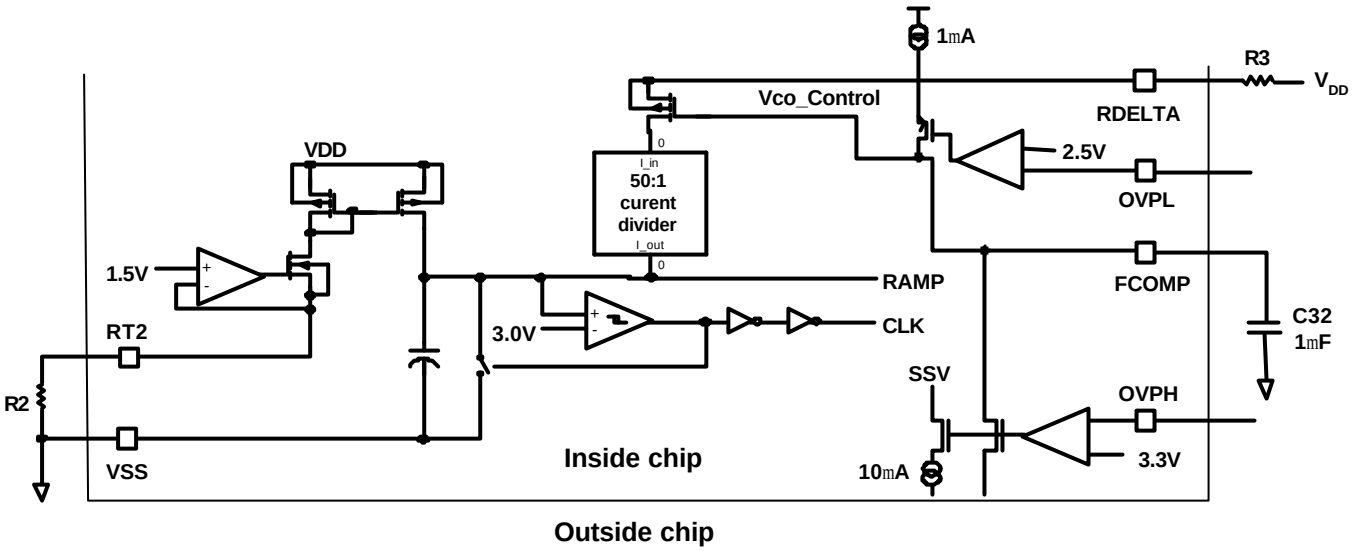


Figure 15. LDO Detail

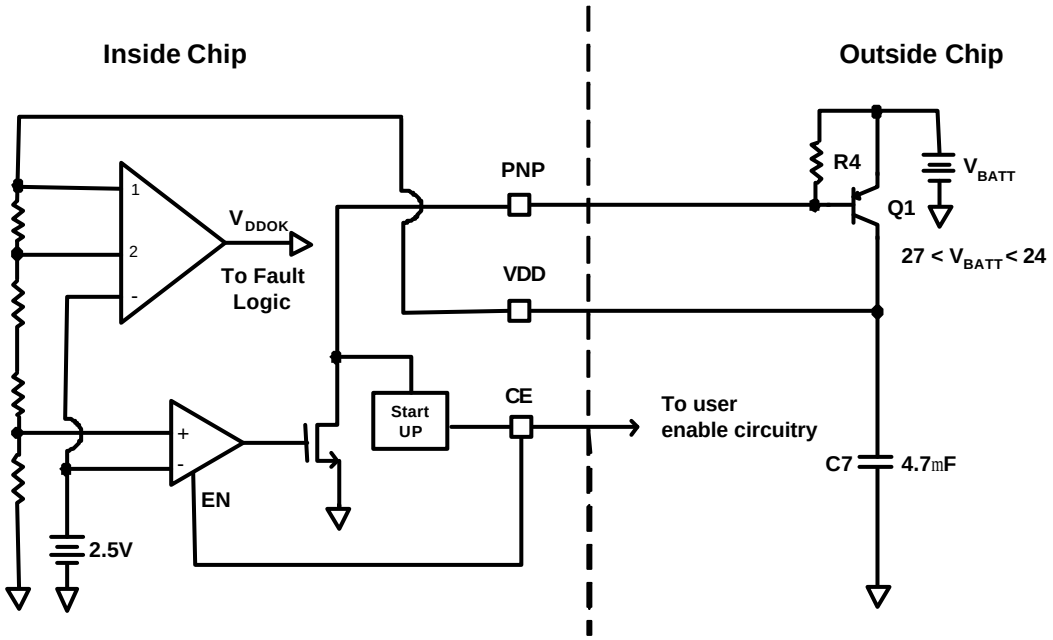


Figure 16. OUTA Driver Circuitry

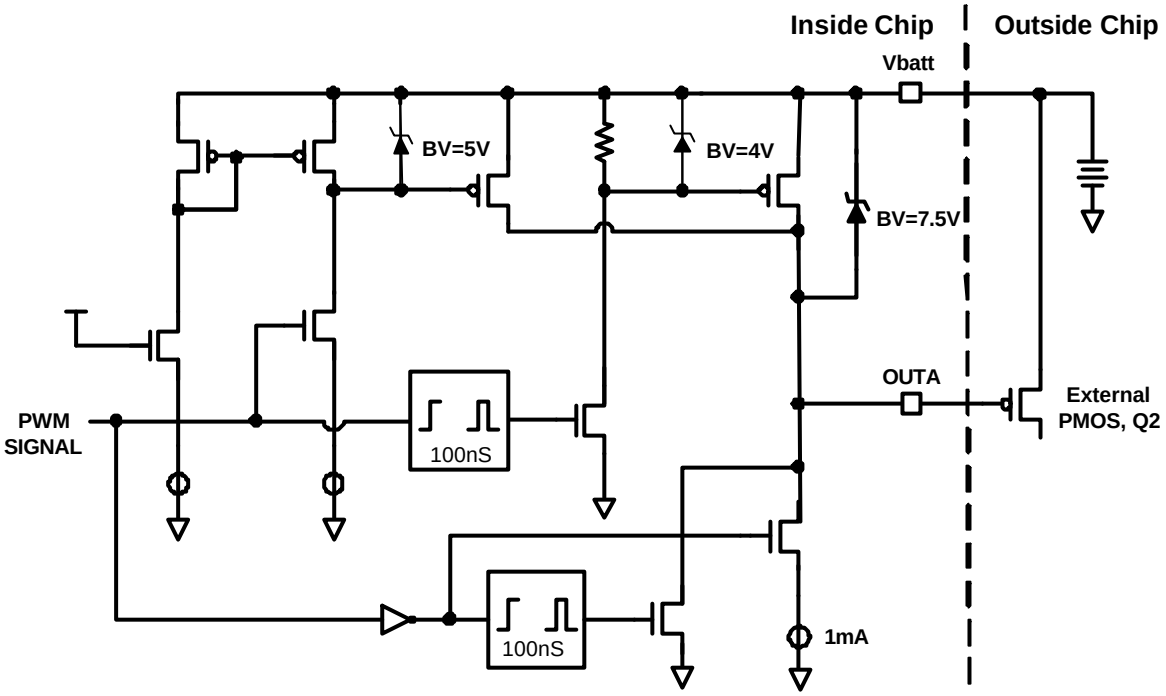
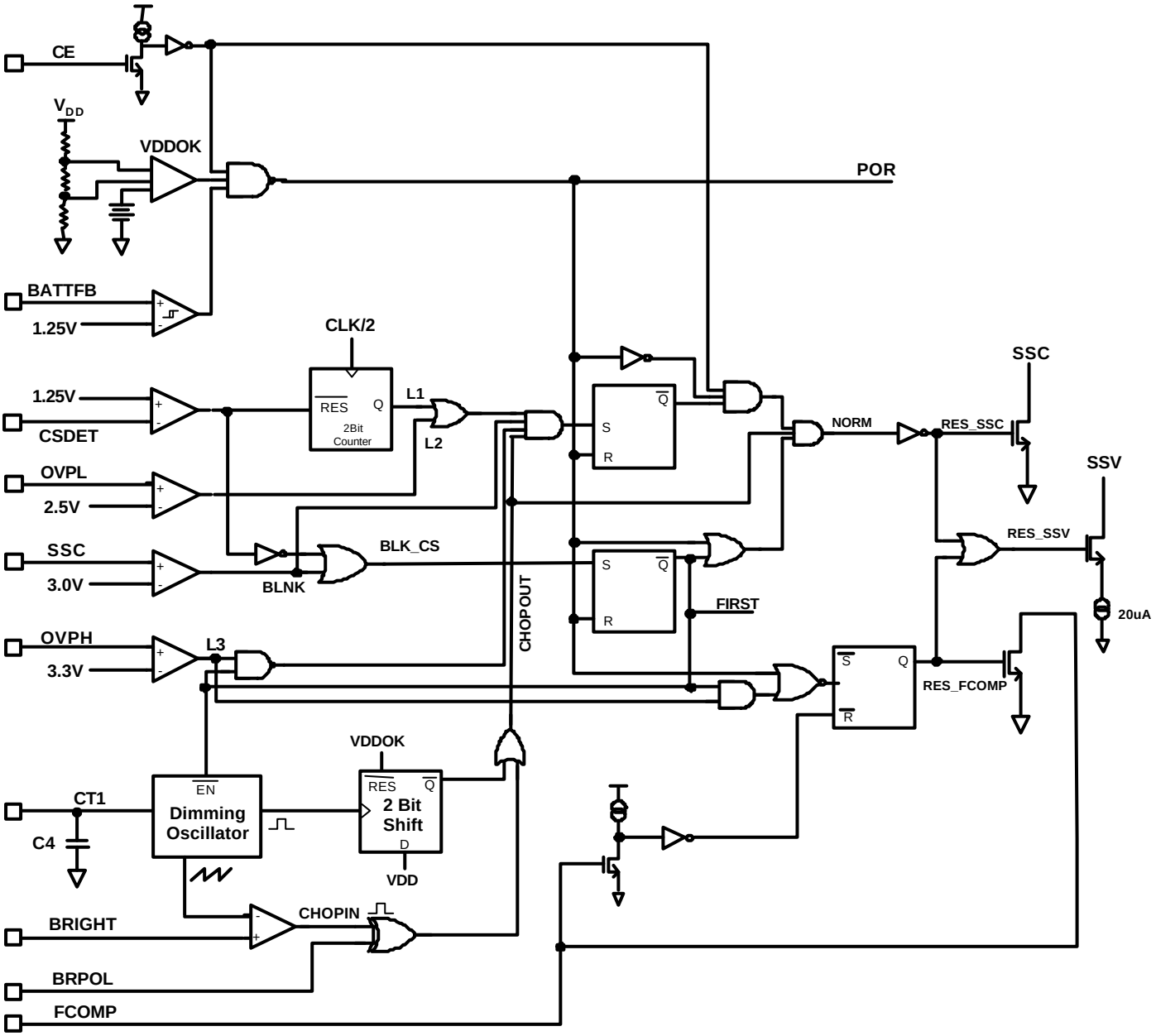


Figure 17. Fault Logic



Application Component Description

Figure 18 shows one typical application circuit for driving 4 tubes. Similar component designations are used on similar components both in figure 2 and Figure 18 as well as throughout this application note.

R1 - Weak pull up for the chip enable (CE) pin. The voltage at CE will normally rise to 5 volts for a 12V supply. Pull down on the CE node to disable the chip and put it into a zero Idd mode. If the user wishes to drive node CE with 3.3 or 5.5 volt logic then R1 is not necessary

C1 - This capacitor acts to de-bounce the CE pin and to slow the turn on time when using R1 to pull up CE. This can be useful when the battery power is disconnected from the circuit in order to turn the circuit off, when the battery is reconnected the chip does not immediately turn on which allows the battery voltage to stabilize before switching starts. If the user is actively driving the CE pin then the C1 capacitor may not be necessary.

R3 - This resistor connected to the RDELTA pin determines how much the oscillator frequency will change with battery voltage. The relation, which is found earlier in the text, is:

Delta frequency (Hz) = 3.44e8 * (5 - V(FCOMP)) / R3

C2 - This 1uF capacitor bypasses and stabilizes the internal reference

C3, C31 - These two capacitors determine the length of the blanking interval at the beginning of every dimming cycle. At the end of every dimming cycle these capacitors are discharged to VSS then allowed to charge up at a rate controlled by its internal current source and the values of C3 and C31. When the voltage on pin SSC crosses 3 volts the blanking interval is over and all fault checks are enabled. The charging current out of pin SSC is normally 140uA but for the very first cycle after the chip is enabled the current is only 1.5uA. During the first cycle of operation one side of C31 is tied to VSS through the SSC1ST pin. This means that during the first cycle the effective capacitance on the SSC pin is C3 + C31. For subsequent cycles the SSC1ST pin reverts to a high impedance state that effectively removes C31 from the circuit. The larger effective capacitor value plus the lower charging current (1.5uA) determines the duration of the intial start up period (nominally 1 second) and is given by the relation:

T(seconds) =(C3+C31) * (3volts) / (1.5e-6amps)

And for subsequent dimming cycles the blanking interval is:

T(seconds) = (C3) * (3volts) / (140e-6amps)

R2 - R2 sets the frequency of the oscillator that drives the FETs. The relation between R2 and frequency, that was found previously in the text, is:

Frequency (Hz) = 2.8e9/R2

R2 = 56K yields approximately 50khz

Note: that this is the frequency of the NMOS(Q3) gate drive. The PMOS(Q2) gate drive is exactly twice this value.

R4 - This resistors pulls the base of Q1 up to Vbatt. Coupled with Q1 and C7 it is part of the 5V regulator that supplies the working power to the AME9003. When the PNP pin is turned off the base of Q1 is pulled high through R4, turning off Q1 and allowing the voltage at the VDD node (VSUPPLY) to decay towards zero.

Q1 - This common PNP transistor (2n3906 is adequate) forms part of the 5V linear regulator which supplies power to most of the AME9003.

R6 - This resistor, together with adjustable resistor R20, form a resistor divider that divides the regulated 5V down to some lower voltage. That lower voltage is used to drive the BRIGHT pin which, in turn, determines the duty cycle of the the dimming cycles and therefore the brightness of the lamps. If the user is driving the BRIGHT pin with his/her own voltage source then R6 and R20 are not necessary.

C6 - This capacitor bypasses the BRIGHT pin. A noisy BRIGHT pin can cause unwanted flicker.

R20 - see description of R6

C14 - Note that the 9003 has a "soft finish" as well as a "soft start" feature. This capacitor sets the slope of the soft-start (soft-finish) ramp on pin SSV. The voltage at SSV limits the duty cycle of the Q2 gate drive signal available at pin OUTA. The voltage at the COMP node is internally clamped to the SSV node. Therefore the C14 cap limits how fast SSV, and hence, COMP can increase (and decrease). Limiting COMP's increase (decrease) will limit the rate of increase (or decrease) of the switching duty cycle thereby creating a "soft start (soft finish)" effect. The charging/discharging current out of SSV is approximately 10uA so the rate of change of the SSV voltage is:

SSV(Volts/sec) = (10e-6amps) / C14

C5 - This is the main battery bypass capacitor.

C4 - This capacitor sets the frequency of the dimming cycles according to the relation:

Dim Cycle Freq(Hz) = 1 / [(4) * (R2) * (C4)]

Note that the frequency is also a function of R2. So the frequency of the main oscillator and the frequency of the dimming oscillator are not independent.

C7 - This capacitor is the load capacitor for the 5V linear regulator. As such it also bypasses the 5V supply and should be laid out as close to the AME9003 as possible.

C8 - This capacitor, in combination with resistor R7, determines the time constant for the error amplifier (integrator) EA1. The integrator is the primary loop stabilizing element of the circuit. In general this application is tolerant of a large range of integrator time constants. Increase the (C8 X R7) product to slow down the loop response.

R7 - see C8

D6 - This diode can catch any negative going spikes on the drain of Q2. This diode is NOT strictly necessary. This is NOT a freewheeling diode such as in a buck regulator. Since the primary windings are tightly coupled to each other the body diodes of Q3-1 and Q3-2 keep their own drains clamped to VSS as well as the drain of Q2. The spikes that diode D6 may catch are of short duration and small energy.

Q2 - This is a PMOS device. By modulating its gate drive duty cycle the power into the transformer, and then into the load, can be controlled. The breakdown of this device must be higher than the highest battery voltage that the application will use. The peak current load is roughly twice the average current load.

Q3-1, Q3-2 - These are NMOS devices. They are driven alternately with 50% duty cycle gate drive. The frequency of the gate drive is one half of the gate drive frequency of Q2. The gate drive is from 0 to 5 volts. The breakdown voltage of these devices must be at least twice the highest battery voltage. Peak current is roughly twice the average supply current.

C9,R8,D2,D3 - These devices form a snubber circuit that can dissipate ringing energy. The snubber circuit is not strictly necessary. In fact a well designed circuit should not require these devices. (These elements were described in more detail earlier.)

R9A, R10 - The sum of R9A and R10 sets the current in one CCFL tube. As the sum of R9A and R10 decreases the tube current goes up, as the sum of R9A and R10 increase the tube current goes down. The RMS tube current is roughly:

Irms = 6V / (R9A + R10)

R9A and R10 also form a voltage divider that drives the CSDET pin. The purpose of the voltage divider is to keep the maximum voltage at CSDET under 5 volts under all conditions. The CSDET pin checks to see if there is any current in the CCFL. If the voltage at CSDET is larger than 1.25V once every clock cycle then the AME9003 assumes there is current in the CCFL and allows operation to continue. CSDET is also used to detect when the CCFL first strikes during the initial start up period.

D4,D5 - These diodes rectify the current through the CCFL to provide a positive voltage for regulation by the error amplifier, EA1.

The following components are only used for multiple tube operation:

Q4,Q5 - These bipolar devices buffer the gate of Q2. That allows Q2 to be made much bigger without dissipating more power or increasing the cost of the AME9003. Q4 is an NPN transistor and Q5 is a PNP transistor.

R35,R36,D16 etc. - These devices form a voltage divider and rectifier combination to sense higher than normal CCFL operating voltages. (This operation is explained in more detail below.) You can diode "OR" as many of these divider/rectifier circuits as you have different CCFLs. Each time you add another double output transformer you must add another set of these resistors and diode networks. (This operation is explained in more detail in the next section.)

D20, D21, R42, R40 and C34 etc. - These devices are not strictly necessary for single tube operation. In single tube operation the junction of R9A and R10 can be directly fed into the CSDET pin. However for multiple tube operation these devices are necessary to allow for any one of the different tubes to be able to pull CSDET below 1.25V and allow a fault to be detected. Figure 1, a single tube application, has these devices included in order to facilitate the transition to multiple tube design as well as working quite well for the single tube application.

Multiple Tube Operation

The AME9003 is particularly well suited for multiple tube applications. Figure19 shows the power section of a two tube application. The major difference between this application and the single tube application is the addition of another secondary winding on the transformer. The primary side of the transformer and its associated FETs are exactly the same as the single tube case although the FETs may need to be resized due to the increased current in two tube applications.

The secondaries are wound so that the outputs to the CCFL are of opposite phase (see Figure 20) although this is not strictly necessary. When the voltage at one secondary output is high (+600 volts) the other secondary output should be low (-600 volts). The other secondary terminals are connected to each other. In a balanced circuit the voltage at the connection of the two secondaries will, ideally, be zero. Of course in a real application the voltage at the connection of the two secondaries will deviate somewhat from zero.

The multi-tube configuration is modular. Since each double transformer can drive two CCFLs it is possible to construct 2, 4, 6..... tube solutions using the basic architecture. Of course the FETs must be properly sized to handle the increased current. Figure 21 shows a 4 tube application. In this configuration the common secondary connection (the node NOT connected to the lamp) is made with the opposite transformer. In this way the secondary current from the winding on the first transformer should be equal to the secondary current of its companion winding on the second transformer. In the case of 4 lamps driven by two transformers there are two sets of common secondary nodes.

Sensing the current in the multiple tube case requires some extra circuitry. Normally the CSDET pin checks for the existence (or absence) of current in the CCFL. If current is detected then the initial start mode terminates and steady state operation begins. During steady state operation if no current is detected for 8 consecutive clock cycles then the circuit is shutdown. Since there is only one CSDET pin yet there are multiple tubes extra circuitry is required.

Take the two tube case of Figure 19 for example. The current through the tube on the right hand side is regulated by the integrator made of R7, C8 and EA1. However, for purposes of fault detection and strike detection it is beneficial to monitor the current through both tubes. In this case R9B senses the current in the left tube in the same way R9A senses the current in the right hand tube. If the current through either tube is zero then R9A or R9B will try to pull node A or B to zero. Resistors R42 and R43 attempt to pull node A and B up but the value of R42 and R43 (nominally 10K) is much larger than the values of resistors R9A and R9B (nominally 221ohms) allowing node A and B to pull close to VSS when there is zero current in their respective CCFL tubes. The absence of current in either tube essentially pulls node A or B to VSS.

In normal operation the voltage at nodes A and B should look like alternating, positive half sinusoids. (See figure 22.) If, however, there is no current flowing in one of the tubes then one half of the sinusoids would be missing and the voltage at CSDET would drop compared to its normal value. The values of the RC network made up of R4 and C34 are chosen so that the voltage at CSDET is always larger than 1.25 volts when both half sinusoids are present but is less than 1.25V when only one sinusoid is present. The concept can be applied to any even multiple of tubes. The tube without the current will dominate the voltage at CSDET so a failure in any single tube will cause the circuit to shutdown. In a similar manner, during start up all tubes must have current flowing in them before CSDET will rise above 1.25V and signal that the tubes have struck and that the initial start up mode is over.

For every 2 extra tubes that need to be added the user must add one more transformer, and two resistor divider networks plus two diodes (R35, R36, R37, R38, D16, D17) to sense the CCFL voltage as well as two more diodes and two more resistors to sense the tube current (R9A, R9B, D20, D22). Resistors R42, R43, R40, diodes D21, D23 and capacitor C34 do not need to be replicated every time more CCFLs are added because they are shared in common on the CSDET node.

Figure 18 shows a complete four tube schematic. Figure 21 shows a detail of the current and voltage sensing circuitry for the four tube application. Analogous components have been given the same numbers as in the single tube schematic. There is really very little difference between the the single tube configuration and the multi-tube version. Transistors Q4 and Q5 are added to buffer the high side drive OUTA. This may be necessary because the PMOS devices for larger current applications have larger gate drive requirements.

The MOS transistors are sized bigger for the 4 tube application as would be expected. The peak currents are much higher so the Vbatt bypassing capacitor must be increased as well. The schematic shows C5 as a 100uF capacitor but higher values such as 220uF are not uncommon in order to minimize ripple on Vbatt.

Figure 18. Four Tube Application Schematic

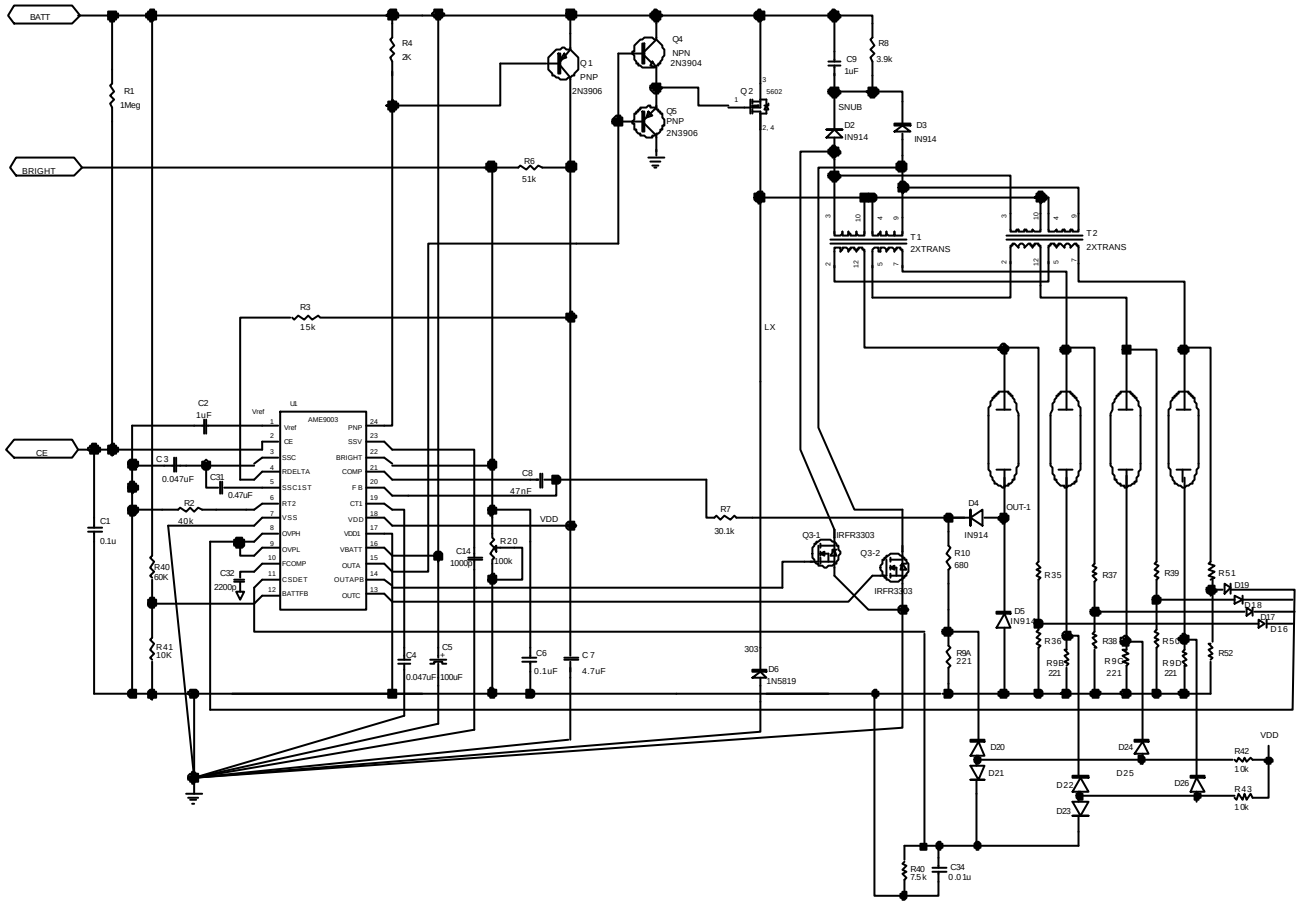


Figure 19. Double CCFL Power Section

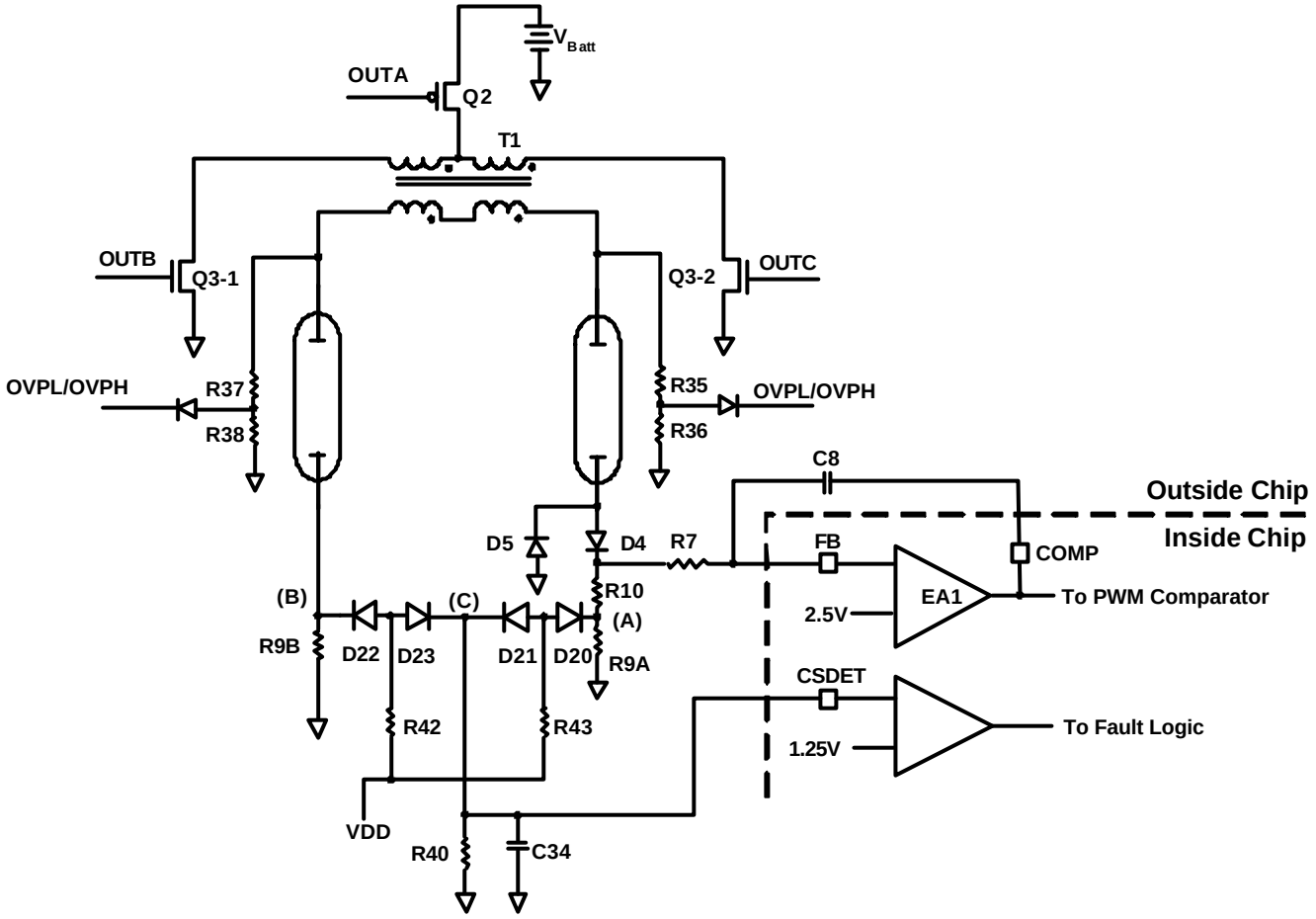


Figure 20. Double transformer construction detail

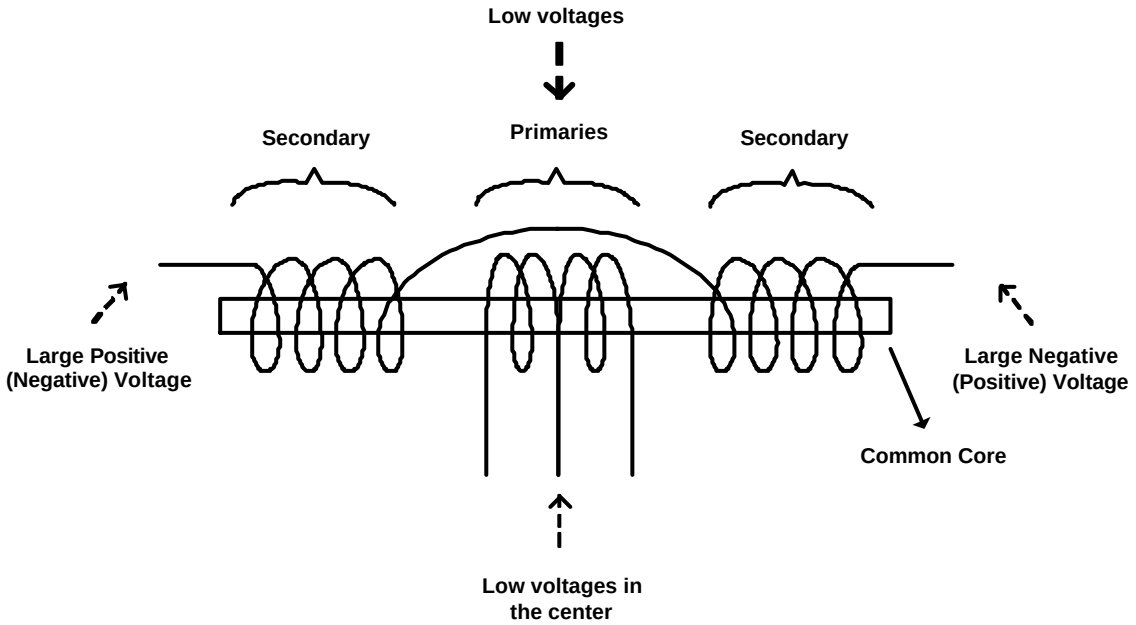


Figure 21. Four Tube Power Section

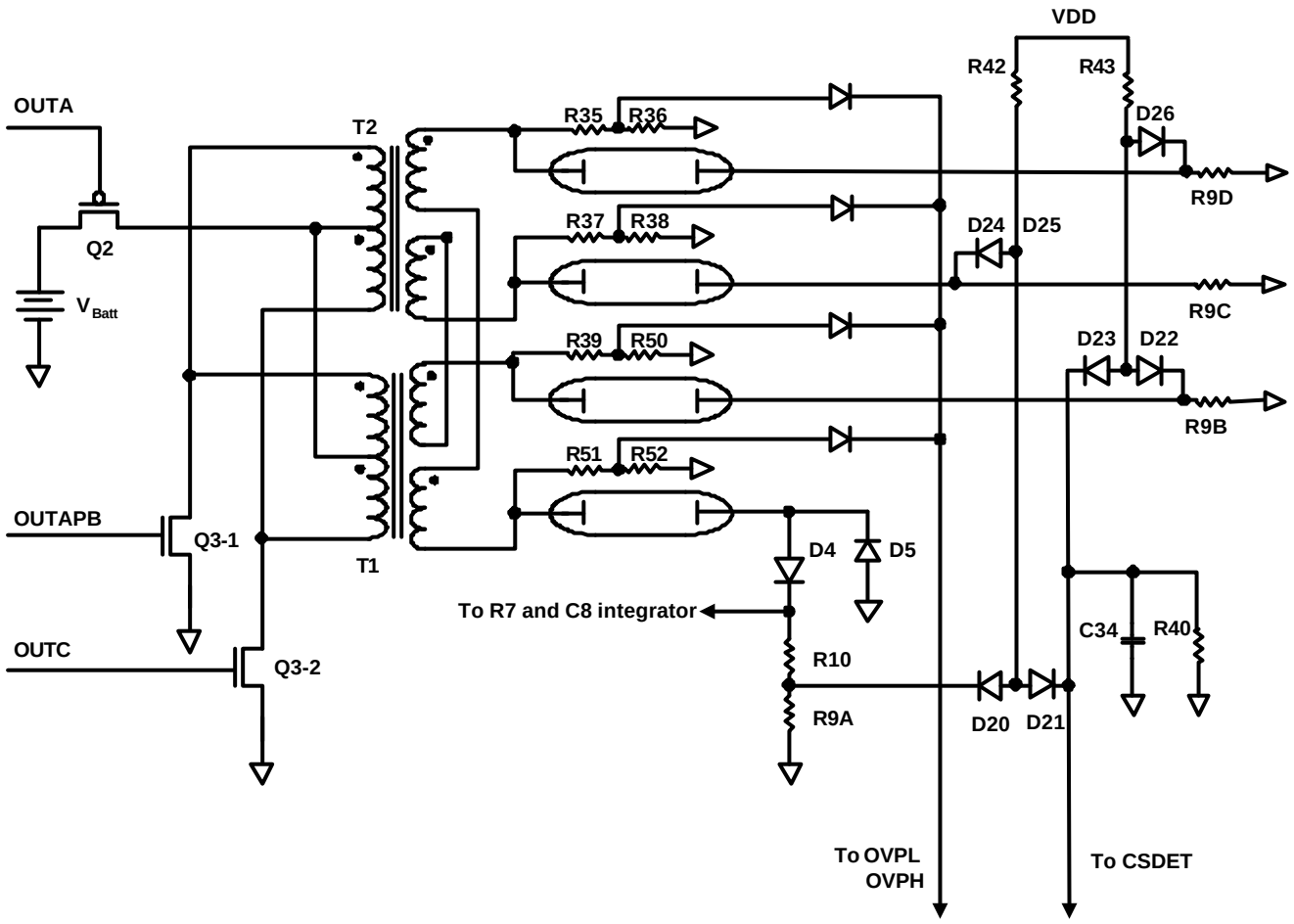
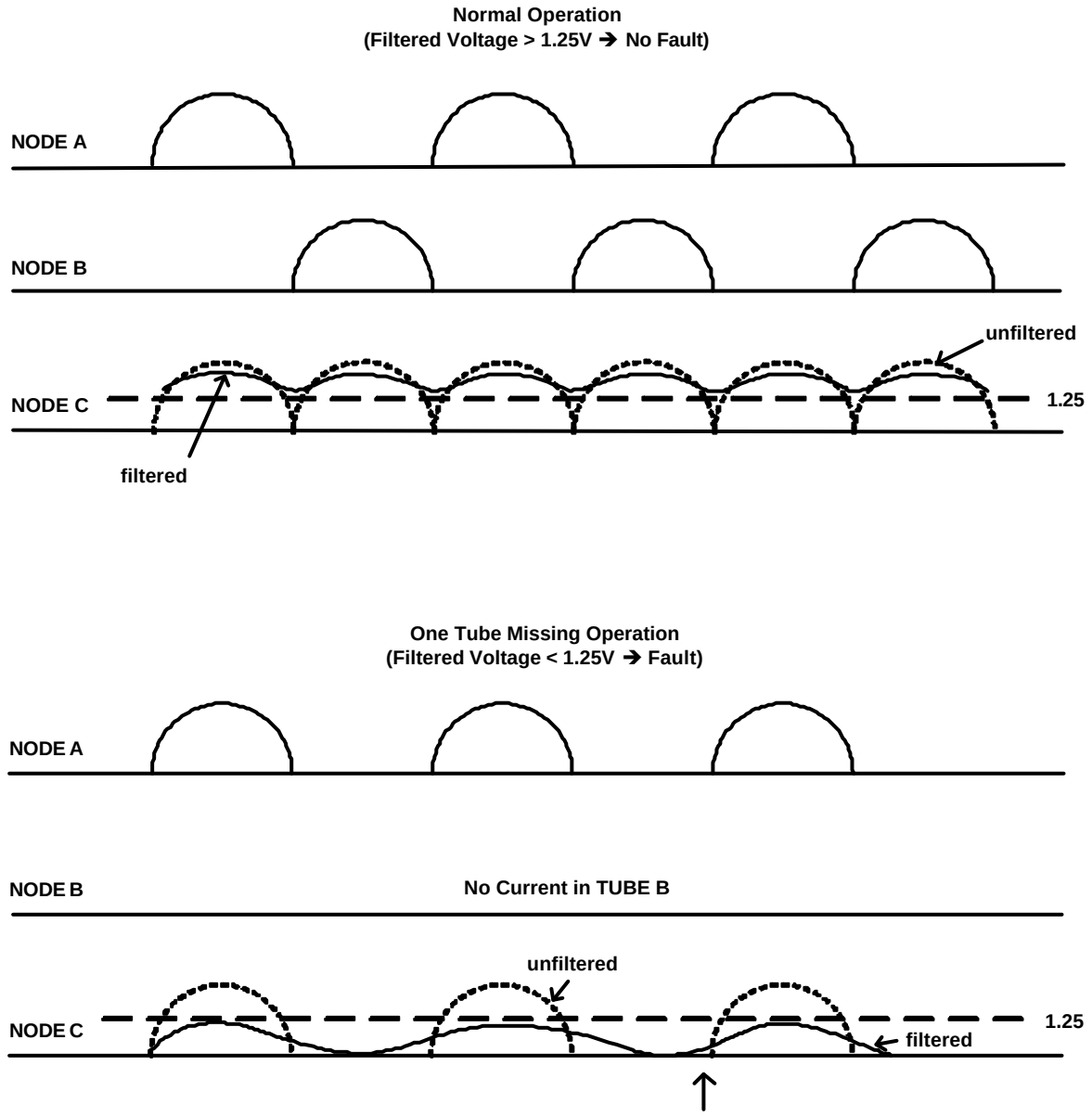


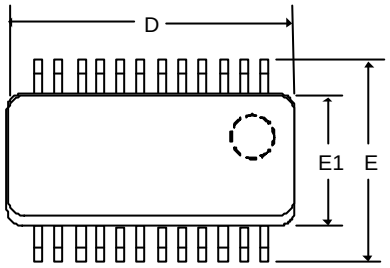
Figure 22.



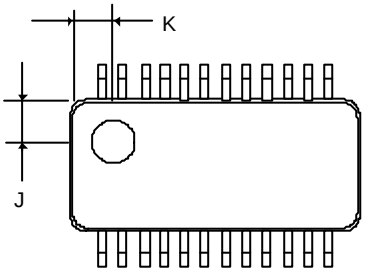
■ Package Dimension

QSOP24

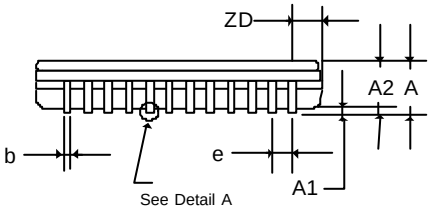
Top View



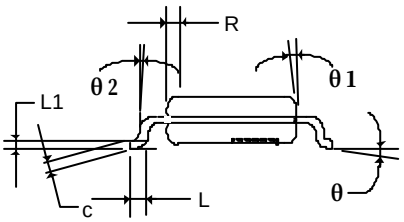
Bottom View



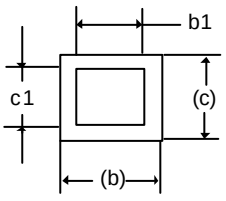
Side View



End View



Detail A

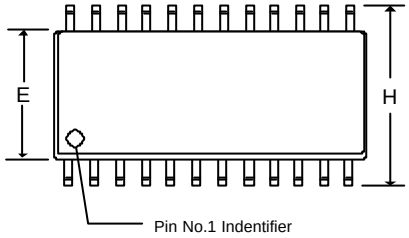


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.524	1.752	0.060	0.069
A1	0.101	0.228	0.004	0.009
A2	1.473REF		0.058REF	
b	0.203	0.304	0.008	0.012
b1	0.203	0.279	0.008	0.011
c	0.177	0.254	0.007	0.010
c1	0.177	0.228	0.007	0.009
D	8.559	8.737	0.337	0.344
ZD	0.838REF		0.033REF	
E	5.791	6.197	0.228	0.244
E1	3.810	3.987	0.150	0.157
L	0.406	1.270	0.016	0.050
L1	0.254BSC		0.010BSC	
e	0.635BSC		0.025BSC	
J	1.27REF		0.050REF	
K	1.27REF		0.050REF	
q	0^o	8^o	0^o	8^o
q1	5^o	15^o	5^o	15^o
q2	0^o	-	0^o	-
R	0.33 x 45^o		0.013 x 45^o	

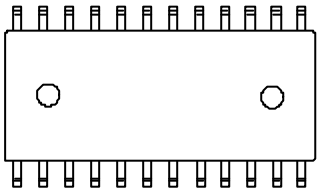
■ Package Dimension

SOIC24

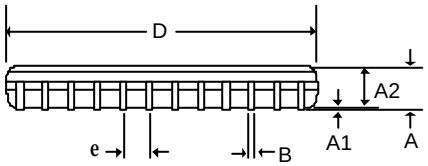
Top View



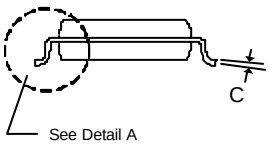
Bottom View



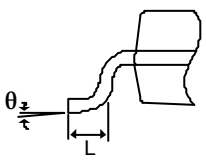
Side View



End View



Detail A

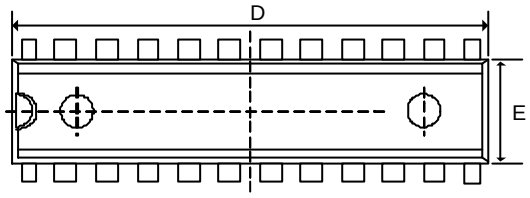


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.092	0.104
A1	0.10	0.30	0.004	0.012
A2	2.25	2.31	0.089	0.091
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.009	0.013
D	15.20	15.60	0.598	0.614
E	7.40	7.60	0.291	0.299
e	1.27BSC		0.050BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
q	0^o	8^o	0^o	8^o

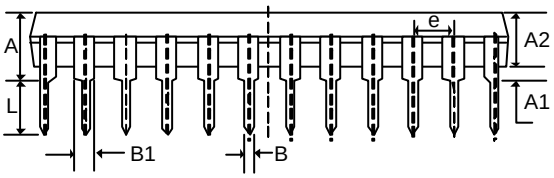
■ Package Dimension

PDIP24 (300mil)

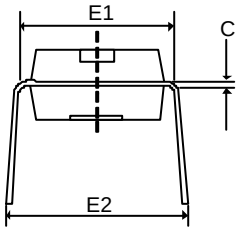
Top View



Side View



End View



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.71	4.31	0.146	0.170
A1	0.51	-	0.020	-
A2	3.20	3.60	0.126	0.142
B	0.36	0.56	0.014	0.022
B1	1.27 TYP		0.050 TYP	
C	0.204	0.36	0.008	0.014
D	29.25	29.85	1.152	1.175
E	6.20	6.60	0.244	0.260
E1	7.62 TYP		0.300 TYP	
e	2.54 TYP		0.100 TYP	
L	3.00	3.60	0.118	0.142
E2	8.20	9.40	0.323	0.370

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