

## Dual N-Channel 20-V (D-S) MOSFET

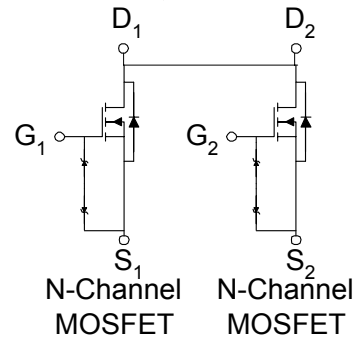
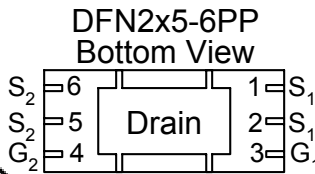
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2x5-6PP saves board space
- Fast switching speed
- High performance trench technology



ESD Protected  
2000V

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
20	22 @ $V_{GS} = 4.5V$	11
	28 @ $V_{GS} = 2.5V$	9.2



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	11	A
	$T_A = 70^\circ\text{C}$		8.5	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 40$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	3.1	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	3.5	W
	$T_A = 70^\circ\text{C}$		1.8	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	36	$^\circ\text{C/W}$
	Steady State		76	$^\circ\text{C/W}$

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	0.5			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			±10	uA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>j</sub> = 55°C			30	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	20			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.5 A			22	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> =0.5 A			28	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 6 A		22		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0 V		0.7		V
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6 A		9.2		nC
Gate-Source Charge	Q <sub>gs</sub>			1.9		
Gate-Drain Charge	Q <sub>gd</sub>			2.8		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 15 Ω , I <sub>d</sub> = 1 A, V <sub>GEN</sub> = 4.5 V		1.7		nS
Rise Time	t <sub>r</sub>			2.3		
Turn-Off Delay Time	t <sub>d(off)</sub>			1.1		
Fall-Time	t <sub>f</sub>			4.4		

## Notes

- Pulse test: PW ≤ 300μs duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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