

1.0 General Description

The AMIS-30663 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12V and 24V systems. The digital interface level is powered from a 3.3V supply providing true I/O voltage levels for 3.3V CAN controllers.

The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller. Due to the wide common-mode voltage range of the receiver inputs, the AMIS-30663 is able to reach outstanding levels of electromagnetic susceptibility. Similarly, extremely low electromagnetic emission is achieved by the excellent matching of the output signals.

2.0 Key Features

- Fully compatible with the "ISO 11898-2" standard
- Certified "Authentication on CAN Transceiver Conformance (d1.1)"
- High speed (up to 1Mbit/s)
- Ideally suited for 12V and 24V industrial and automotive applications
- Low electromagnetic mission (EME) common-mode-choke is no longer required
- Differential receiver with wide common-mode range (+/- 35V) for high electro magnetic susceptibility (EMS)
- No disturbance of the bus lines with an un-powered node
- Transmit data (TxD) dominant time-out function
- Thermal protection
- Bus pins protected against transients in an automotive environment
- Short circuit proof to supply voltage and ground
- Logic level inputs compatible with 3.3V devices
- ESD protection level for CAN bus up to $\pm 8\text{kV}$

3.0 Technical Characteristics

Table 1: Technical Characteristics

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------------------|---|--|------|------|------|
| V_{CANH} | DC voltage at pin CANH | $0 < V_{CC} < 5.25\text{V}$; no time limit | -45 | +45 | V |
| V_{CANL} | DC voltage at pin CANL | $0 < V_{CC} < 5.25\text{V}$; no time limit | -45 | +45 | V |
| $V_{(diff)(bus_dom)}$ | Differential bus output voltage in dominant state | $42.5\Omega < R_{LT} < 60\Omega$ | 1.5 | 3 | V |
| $t_{pd(rec-dom)}$ | Propagation delay TxD to RxD | See Figure 7 | 100 | 230 | ns |
| $t_{pd(dom-rec)}$ | Propagation delay TxD to RxD | See Figure 7 | 100 | 245 | ns |
| CM-range | Input common-mode range for comparator | Guaranteed differential receiver threshold and leakage current | -35 | +35 | V |
| $V_{CM-peak}$ | Common-mode peak | See Figure 8 and 9 (Note) | -500 | 500 | mV |
| $V_{CM-step}$ | Common-mode step | See Figure 8 and 9 (Note) | -150 | 150 | mV |

Note: The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low EME.

4.0 Ordering Information

| Marketing Name | Package | Temp. Range |
|----------------|--------------|---------------|
| AMIS 30663NGA | SOIC-8 GREEN | -40°C...125°C |

5.0 Block Diagram

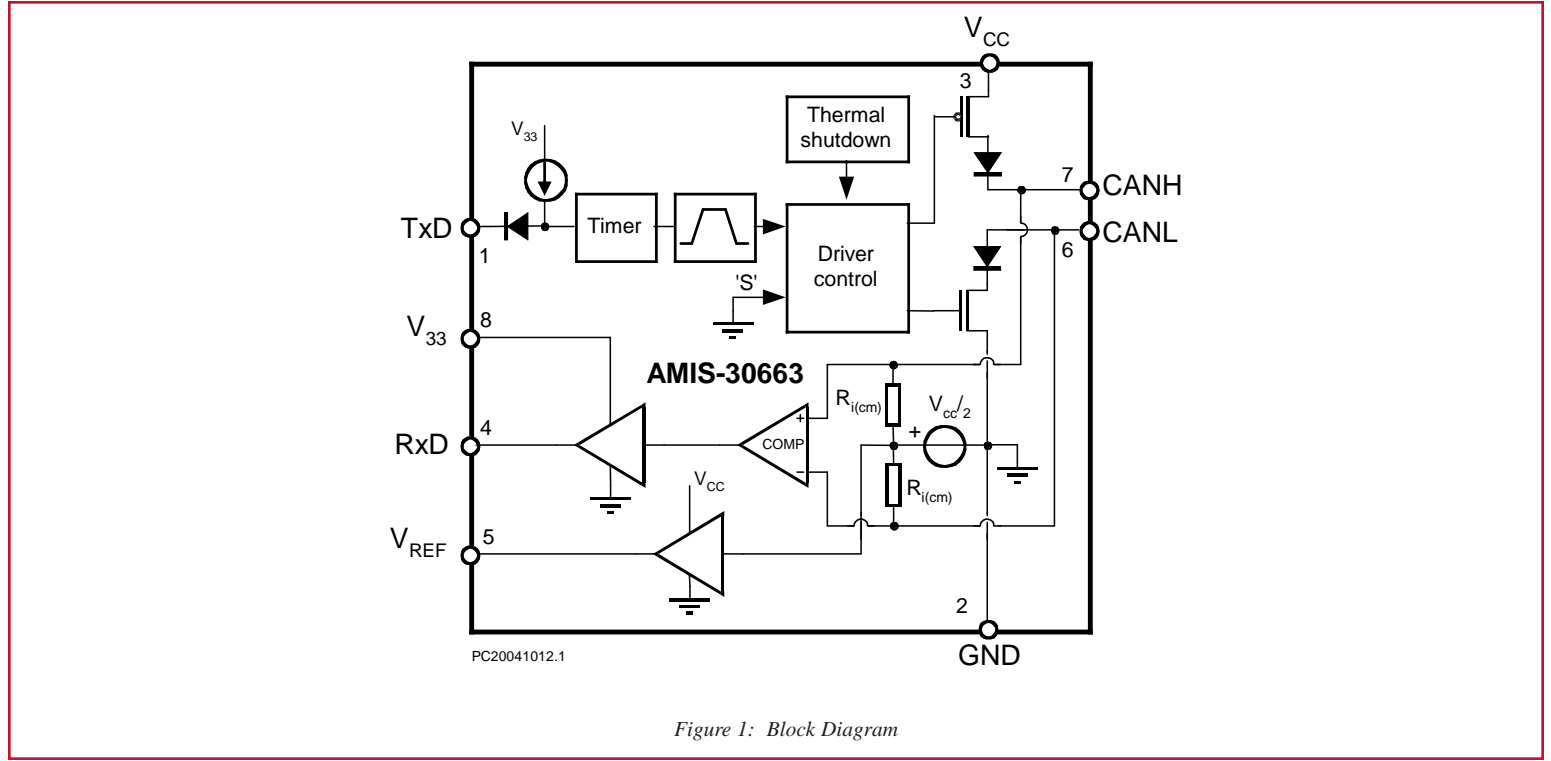


Figure 1: Block Diagram

6.0 Typical Application

6.1 Application Schematic

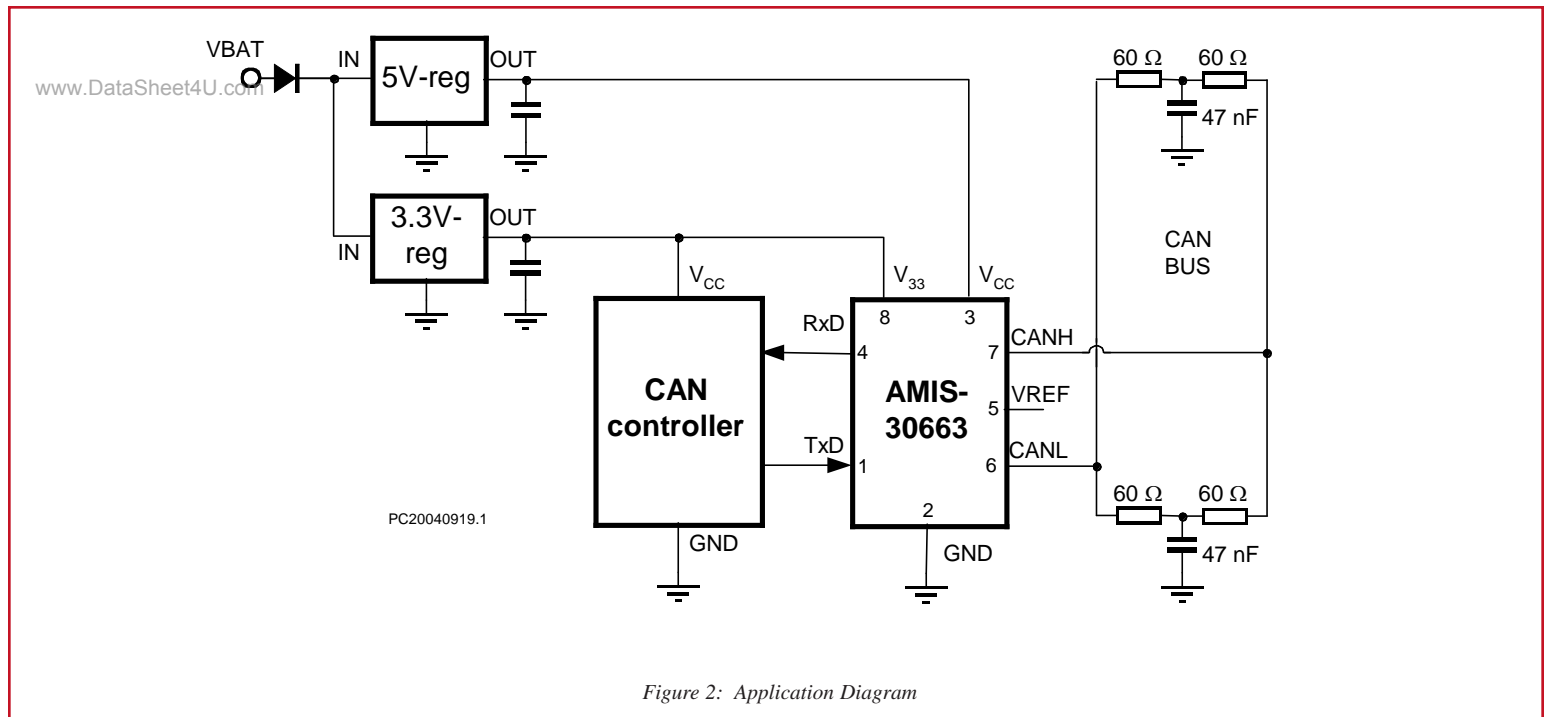


Figure 2: Application Diagram

6.2 Pin Description

6.2.1 Pin Out (top view)

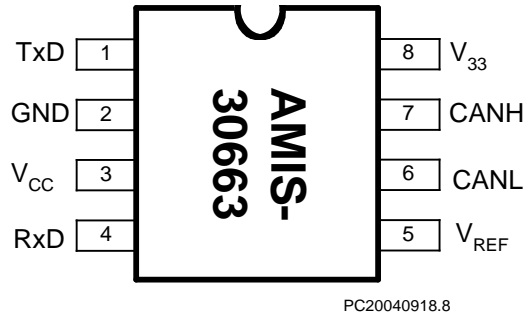


Figure 3: Pin Configuration

6.2.2 Pin Description

Table 2: Pin Out

| Pin | Name | Description |
|-----|------------------|--|
| 1 | TxD | Transmit data input; low input → dominant driver; internal pull-up current |
| 2 | GND | Ground |
| 3 | V _{cc} | Supply voltage |
| 4 | RxD | Receive data output; dominant transmitter → low output |
| 5 | V _{REF} | Reference voltage output |
| 6 | CANL | LOW-level CAN bus line (low in dominant mode) |
| 7 | CANH | HIGH-level CAN bus line (high in dominant mode) |
| 8 | V ₃₃ | 3.3V supply for digital I/O |

7.0 Functional Description

7.1 General

The AMIS-30663 is the interface between the CAN protocol controller and the physical bus. It is intended for use in automotive and industrial applications requiring baud rates up to 1Mbaud. It provides differential transmit capability to the bus and differential receiver capability to the CAN protocol controller. It is fully compatible to the "ISO 11898-2" standard.

7.2 Operating Modes

AMIS-30663 only operates in high-speed mode as illustrated in Table 3.

The transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimised to give extremely low EME.

Table 3: Function Table (X = don't care)

4.75 < V_{CC} < 5.25V

| Mode | Pin | | Bus | | |
|------------|-----|-----|-----------|---------------------|---------------------|
| | TxD | RxD | STATE | CANH | CANL |
| High Speed | 0 | 0 | Dominant | High | Low |
| | 1 | 1 | Recessive | 0.5 V _{CC} | 0.5 V _{CC} |

V_{CC} < PORL

| Mode | Pin | | Bus | | |
|------|-----|-----|-----------|---|---|
| | TxD | RxD | STATE | CANH | CANL |
| - | X | 1 | Recessive | 0 < V _{CANH} < V _{CC} | 0 < V _{CANL} < V _{CC} |

PORL < V_{CC} < 4.75V

| Mode | Pin | | Bus | | |
|------|-------------------|-----|-----------|---|---|
| | TxD | RxD | STATE | CANH | CANL |
| - | > V _{IH} | 1 | Recessive | 0 < V _{CANH} < V _{CC} | 0 < V _{CANL} < V _{CC} |

7.3 Over-temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TxD goes HIGH. The thermal protection circuit is particularly needed when a bus line short circuits.

7.4 TxD Dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the LOW-level on pin TxD exceeds the internal timer value t_{dom} , the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

7.5 Fail-safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage - although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to "ISO 7637"; see Figure 4). Should TxD become disconnected, this pin is pulled high internally. When the V_{CC} supply is removed, pins TxD and RxD will be floating. This prevents the AMIS-30663 from being supplied by the CAN controller through the I/O pins.

7.6 3.3V Interface

AMIS-30663 may be used to interface with 3.3V or 5V controllers by use of the V₃₃ pin. This pin may be supplied with 3.3V or 5V to have the corresponding digital interface voltage levels.

When the V₃₃ pin is supplied at 2.5V, even interfacing with 2.5V CAN controllers is possible. See also Digital Output Characteristics @ V₃₃ = 2.5V, Table 7. In this case a pull resistor from TxD to V₃₃ is necessary.

8.0 Electrical Characteristics

8.1 Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

8.2 Absolute Maximum Ratings

Stresses above those listed in Table 4 may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|-----------------------------|--|--|------|-----------------------|------|
| V _{CC} | Supply voltage | | -0.3 | +7 | V |
| V ₃₃ | I/O interface voltage | | -0.3 | +7 | V |
| V _{CANH} | DC voltage at pin CANH | 0 < V _{CC} < 5.25V; no time limit | -45 | +45 | V |
| V _{CANL} | DC voltage at pin CANL | 0 < V _{CC} < 5.25V; no time limit | -45 | +45 | V |
| V _{TxD} | DC voltage at pin TxD | | -0.3 | V _{CC} + 0.3 | V |
| V _{RxD} | DC voltage at pin RxD | | -0.3 | V _{CC} + 0.3 | V |
| V _{REF} | DC voltage at pin VREF | | -0.3 | V _{CC} + 0.3 | V |
| V _{tran(CANH)} | Transient voltage at pin CANH | Note 1 | -150 | +150 | V |
| V _{tran(CANL)} | Transient voltage at pin CANL | Note 1 | -150 | +150 | V |
| V _{tran(VREF)} | Transient voltage at pin VREF | Note 1 | -150 | +150 | V |
| V _{esd(CANL/CANH)} | Electrostatic discharge voltage at CANH and CANL pin | Note 2 | -8 | +8 | kV |
| | | Note 5 | -500 | +500 | V |
| V _{esd} | Electrostatic discharge voltage at all other pins | Note 3 | -4 | +4 | kV |
| | | Note 5 | -250 | +250 | V |
| Latch-up | Static latch-up at all pins | Note 4 | | 100 | mA |
| T _{stg} | Storage temperature | | -55 | +155 | °C |
| T _{amb} | Ambient temperature | | -40 | +125 | °C |
| T _{junc} | Maximum junction temperature | | -40 | +150 | °C |

Notes

- 1) Applied transient waveforms in accordance with "ISO 7637 part 3", test pulses 1, 2, 3a, and 3b (see Figure 4).
- 2) Standardized human body model system ESD pulses in accordance to IEC 1000.4.2
- 3) Standardized human body model ESD pulses in accordance to MIL883 method 3015. Supply pin 8 is ±4kV
- 4) Static latch-up immunity: static latch-up protection level when tested according to EIA/JESD78.
- 5) Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

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8.3 Thermal Characteristics

Table 5: Thermal Characteristics

| Symbol | Parameter | Conditions | Value | Unit |
|----------------------|--|-------------|-------|------|
| R _{th(j-a)} | Thermal resistance from junction to ambient in SO8 package | In free air | 145 | K/W |
| R _{th(j-s)} | Thermal resistance from junction to substrate of bare die | In free air | 45 | K/W |

8.4 DC Characteristics

Table 6: Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|------------------------|------------------------|------------------------|------|
| Supply (pin V_{CC} and pin V₃₃) | | | | | | |
| I _{CC} | Supply current | Dominant; V _{TxD} = 0V | | 45 | 65 | mA |
| | | Recessive; V _{TxD} = V _{CC} | | 4 | 8 | mA |
| I ₃₃ | I/O interface current | V ₃₃ = 3.3V; C _L = 20pF; recessive | | | 1 | μA |
| I ₃₃ | I/O interface current ⁽¹⁾ | V ₃₃ = 3.3V; C _L = 20pF; 1Mbps | | | 170 | μA |
| Transmitter Data Input (pin TxD) | | | | | | |
| V _{IH} | HIGH-level input voltage | Output recessive | 2.0 | - | V _{CC} | V |
| V _{IL} | LOW-level input voltage | Output dominant | -1.3 | - | +0.8 | V |
| I _{IH} | HIGH-level input current | V _{TxD} = V ₃₃ | -1 | 0 | +1 | μA |
| I _{IL} | LOW-level input current | V _{TxD} = 0V | -50 | -200 | -300 | μA |
| C | Input capacitance ⁽¹⁾ | | - | 5 | 10 | pF |
| Receiver Data Output (pin RxD) | | | | | | |
| V _{OH} | HIGH-level input voltage | I _{RxD} = -10mA | 0.7 x V ₃₃ | 0.75 x V ₃₃ | | V |
| V _{OL} | LOW-level input voltage | I _{RxD} = 5mA | | 0.18 | 0.35 | V |
| I _{oh} | HIGH-level input voltage ⁽¹⁾ | V _{RxD} = 0.7 x V ₃₃ | -10 | -15 | -20 | mA |
| I _{ol} | LOW-level input voltage ⁽¹⁾ | V _{RxD} = 0.45V | 5 | 10 | 15 | mA |
| Reference Voltage Output (V_{REF}) | | | | | | |
| V _{REF} | Reference output voltage | -50μA < I _{VREF} < +50μA | 0.45 X V _{CC} | 0.50 X V _{CC} | 0.55 X V _{CC} | V |
| V _{REF_CM} | Reference output voltage for full common-mode range | -35V < V _{CANH} < +35V | 0.40 X V _{CC} | 0.50 X V _{CC} | 0.60 X V _{CC} | V |
| | | -35V < V _{CANL} < +35V | | | | |
| Bus Lines (pins CANH and CANL) | | | | | | |
| V _{o(reces)(CANH)} | Recessive bus voltage at pin CANH | V _{TxD} = V _{CC} ; no load | 2.0 | 2.5 | 3.0 | V |
| V _{o(reces)(CANL)} | Recessive bus voltage at pin CANL | V _{TxD} = V _{CC} ; no load | 2.0 | 2.5 | 3.0 | V |
| I _{o(reces)(CANH)} | Recessive output current at pin CANH | -35V < V _{CANH} < +35V | -2.5 | - | +2.5 | mA |
| | | 0V < V _{CC} < 5.25V | | | | |
| I _{o(reces)(CANL)} | Recessive output current at pin CANL | -35V < V _{CANL} < +35V | -2.5 | - | -2.5 | mA |
| | | 0V < V _{CC} < 5.25V | | | | |
| V _{o(dom)(CANH)} | Dominant output voltage at pin CANH | V _{TxD} = 0V | 3.0 | 3.6 | 4.25 | V |
| V _{o(dom)(CANL)} | Dominant output voltage at pin CANL | V _{TxD} = 0V | 0.5 | 1.4 | 1.75 | V |
| V _{dif(bus)} | Differential bus input voltage (V _{CANH} - V _{CANL}) | V _{TxD} = 0V; dominant; 42.5Ω < R _{LT} < 60Ω | 1.5 | 2.25 | 3.0 | V |
| I _{o(sc)(CANH)} | Short circuit output current at pin CANH | V _{TxD} = V _{CC} ; recessive; no load | -120 | 0 | +50 | mV |
| | | V _{CANH} = 0V; V _{TxD} = 0V | -45 | -70 | -95 | mA |
| I _{o(sc)(CANL)} | Short circuit output current at pin CANL | V _{CANL} = 36V; V _{TxD} = 0V | 45 | 70 | 120 | mA |
| V _{dif(th)} | Differential receiver threshold voltage | -5V < V _{CANL} < +12V; -5V < V _{CANH} < +12V; see Figure 5 | 0.5 | 0.7 | 0.9 | V |
| V _{hcm(dif)(th)} | Differential receiver threshold voltage for high common-mode | -35V < V _{CANL} < +35V; -35V < V _{CANH} < +35V; see Figure 5 | 0.25 | 0.7 | 1.05 | V |
| V _{dif(hys)} | Differential receiver input voltage hysteresis | -35V < V _{CANL} < +35V; -35V < V _{CANH} < +35V; see Figure 5 | 50 | 70 | 100 | mV |
| R _{(cm)(CANH)} | Common-mode input resistance at pin CANH | | 15 | 25 | 37 | kΩ |
| R _{(cm)(CANL)} | Common-mode input resistance at pin CANL | | 15 | 25 | 37 | kΩ |
| R _{(cm)(m)} | Matching between pin CANH and pin CANL common-mode input resistance | V _{CANH} = V _{CANL} | -3 | 0 | +3 | % |
| R _(dif) | Differential input resistance | | 25 | 50 | 75 | kΩ |
| C _(CANH) | Input capacitance at pin CANH | V _{TxD} = V _{CC} ; not tested | | 7.5 | 20 | pF |
| C _(CANL) | Input capacitance at pin CANL | V _{TxD} = V _{CC} ; not tested | | 7.5 | 20 | pF |
| C _(dif) | Differential input capacitance | V _{TxD} = V _{CC} ; not tested | | 3.75 | 10 | pF |
| I _{LI(CANH)} | Input leakage current at pin CANH | V _{CC} = 0V; V _{CANH} = 5V | 10 | 170 | 250 | μA |

Table 6: Characteristics, Cont.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--|--|------|------|------|-------------|
| Bus Lines (pins CANH and CANL) | | | | | | |
| $I_{L(CANL)}$ | Input leakage current at pin CANL | $V_{CC} = 0V; V_{CANL} = 5V$ | 10 | 170 | 250 | μA |
| $V_{CM-peak}$ | Common-mode peak during transition from dom \rightarrow rec or rec \rightarrow dom | See Figure 8 and 9 | -500 | | 500 | mV |
| $V_{CM-step}$ | Difference in common-mode between dominant and recessive state | See Figure 8 and 9 | -150 | | 150 | mV |
| Power-on-Reset | | | | | | |
| PORL | POR level | CANH, CANL, V_{ref} in tri-state below POR level | 2.2 | 3.5 | 4.7 | V |
| Thermal Shutdown | | | | | | |
| $T_{(sd)}$ | Shutdown junction temperature | | 150 | 160 | 180 | $^{\circ}C$ |
| Timing Characteristics (see Figure 6 and 7) | | | | | | |
| $t_{d(TxD-BUSon)}$ | Delay TxD to bus active | | 40 | 85 | 110 | ns |
| $t_{d(TxD-BUSoff)}$ | Delay TxD to bus inactive | | 30 | 60 | 110 | ns |
| $t_{d(BUSon-RxD)}$ | Delay bus active to RxD | | 25 | 55 | 110 | ns |
| $t_{d(BUSoff-RxD)}$ | Delay bus inactive to RxD | | 65 | 100 | 135 | ns |
| $t_{pd(rec-dom)}$ | Propagation delay TxD to RxD from recessive to dominant | | 100 | | 230 | ns |
| $t_{d(dom-rec)}$ | Propagation delay TxD to RxD from dominant to recessive | | 100 | | 245 | ns |
| $t_{dom(TxD)}$ | TxD dominant time for time out | $V_{TxD} = 0V$ | 250 | 450 | 750 | μs |

Notes

1) Not tested on ATE.

Table 7: Digital Output Characteristics @ $V_{33} = 2.5V$

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------|---------------------------|------------------------------|------|------|------|------|
| Receiver Data Output (pin RxD) | | | | | | |
| I_{oh} | HIGH-level output current | $V_{OH} > 0.9 \times V_{33}$ | -2.6 | | | mA |
| I_{ol} | LOW-level output current | $V_{OL} < 0.1 \times V_{33}$ | | | 4 | mA |

$V_{CC} = 4.75$ to $5.25V$; $V_{33} = 2.5V \pm 5\%$; $T_{junc} = -40$ to $+150^{\circ}C$; $R_{LT} = 60\Omega$ unless specified otherwise.

8.5 Measurement Set-ups and Definitions

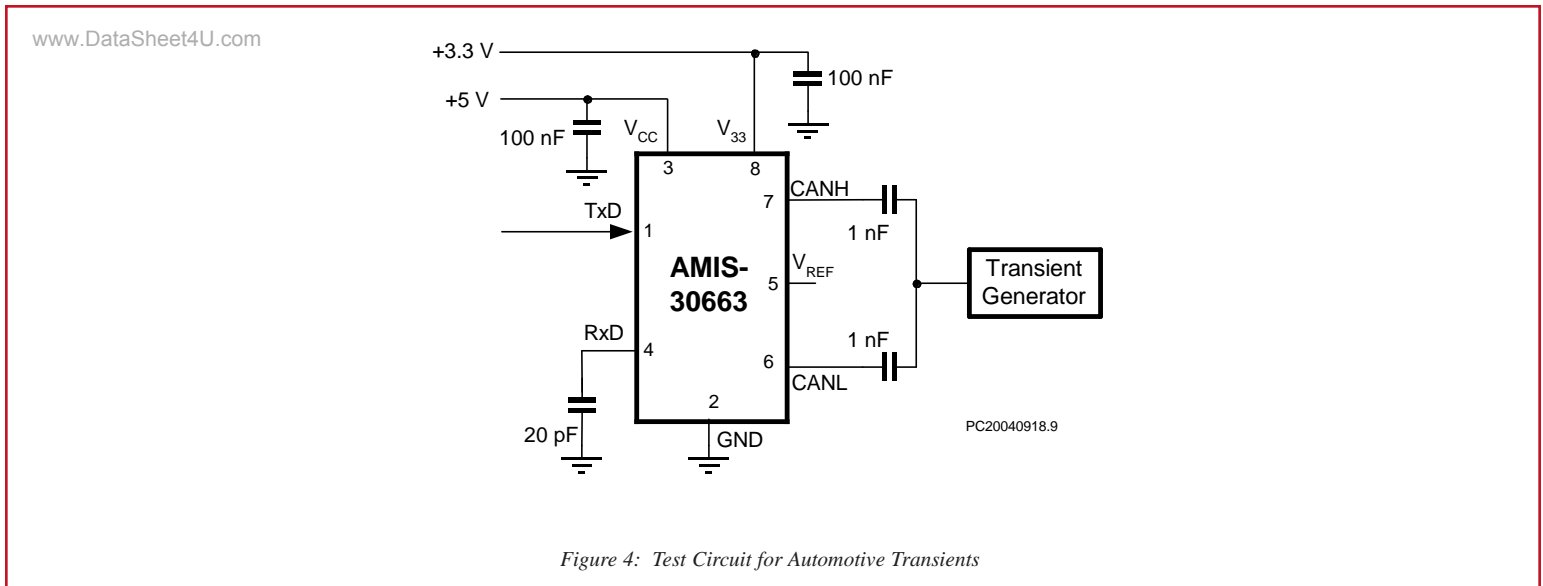


Figure 4: Test Circuit for Automotive Transients

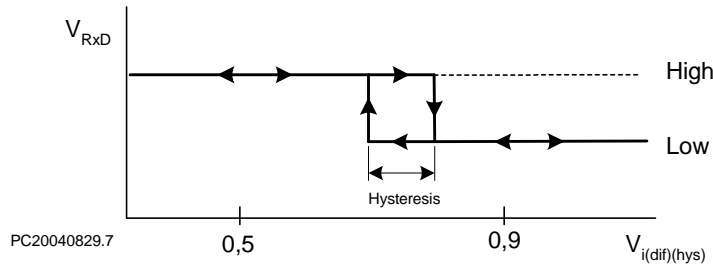


Figure 5: Hysteresis of the Receiver

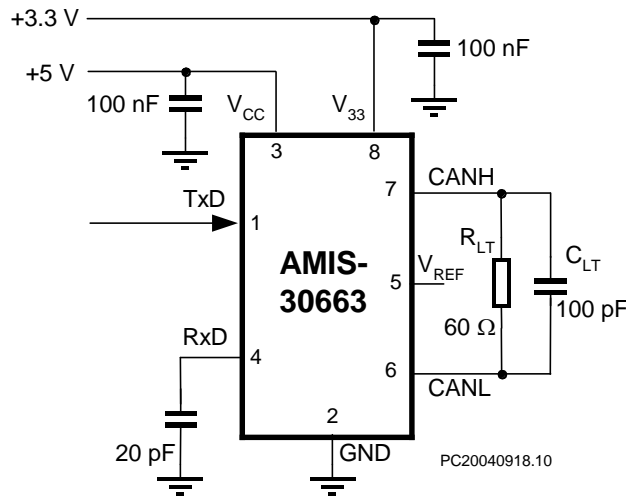


Figure 6: Test Circuit for Timing Characteristics

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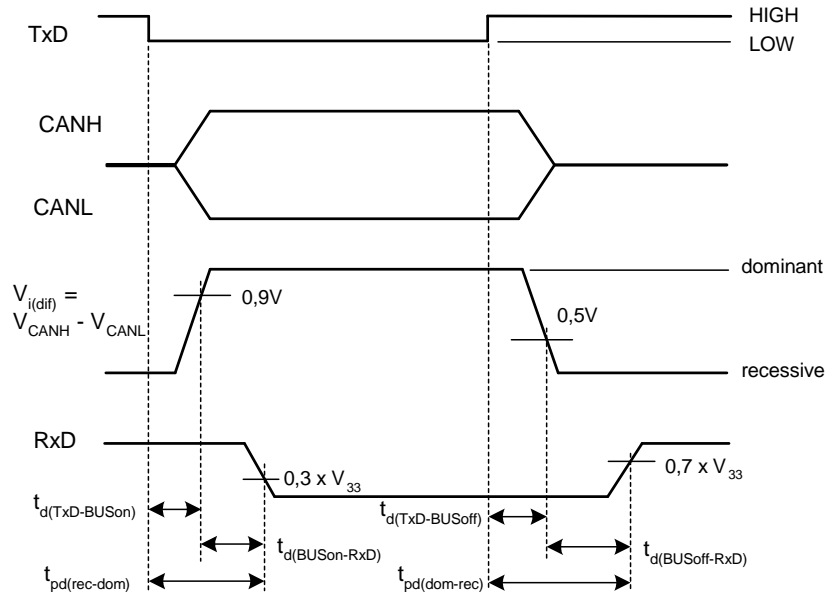
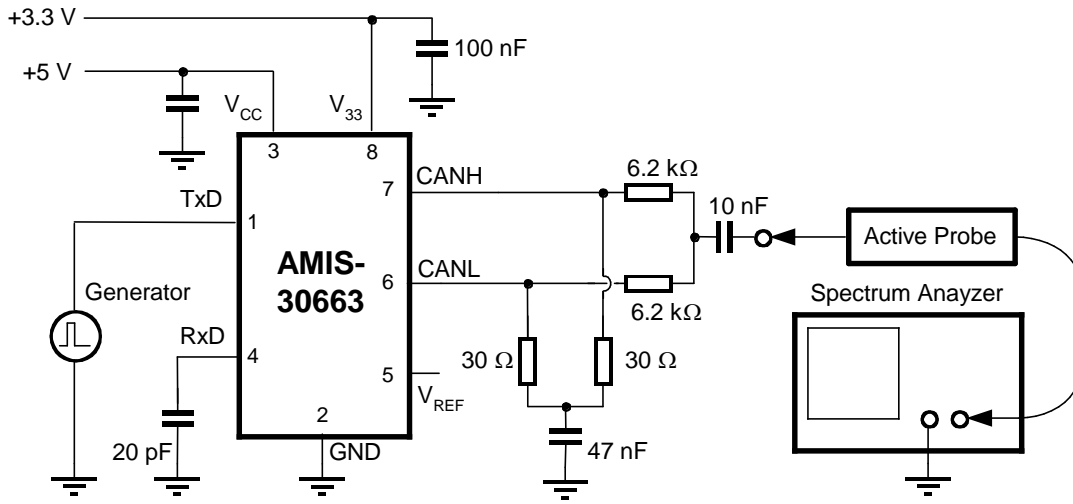
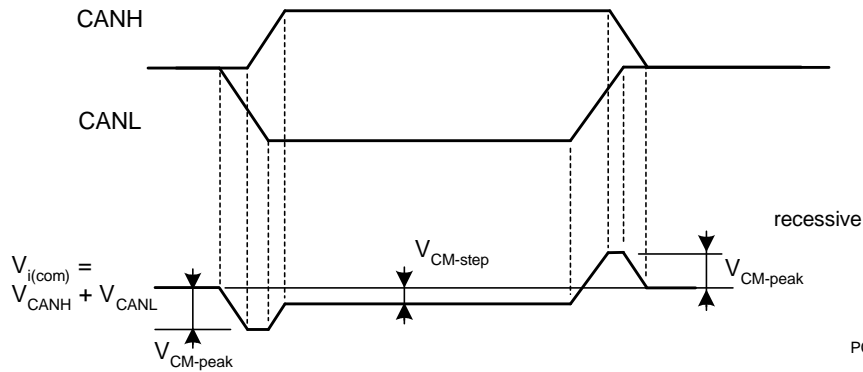


Figure 7: Timing Diagram for AC Characteristics



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Figure 8: Basic Test Set-up for Electromagnetic Measurement

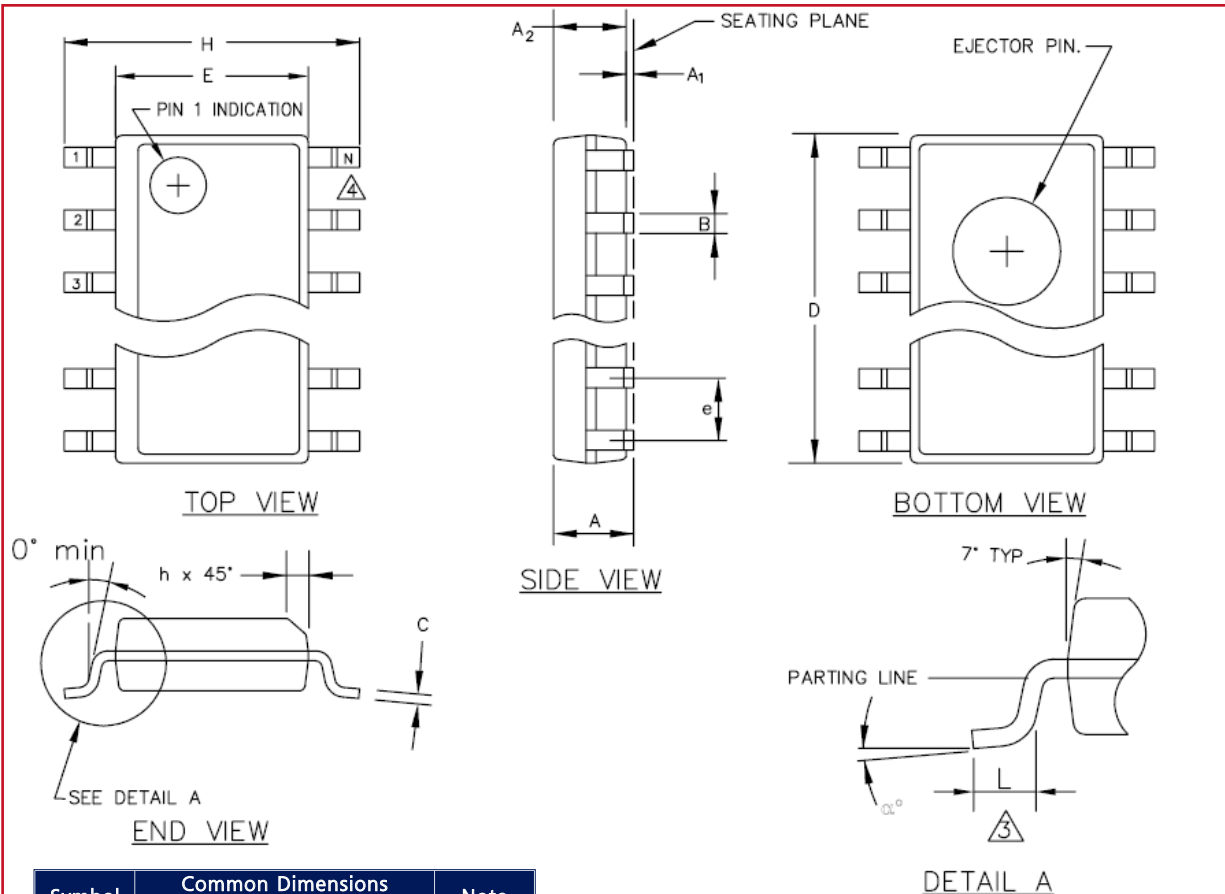


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Figure 9: Common-mode Voltage Peaks (see measurement set-up Figure 8)

9.0 Package Outline

SOIC-8: Plastic small outline; 8 leads; body width 150 mil; JEDEC: MS-012



| Symbol | Common Dimensions | | | Note |
|----------------|-------------------|------|-------|------|
| | Min. | Nom. | Max. | |
| A | .061 | .064 | .068 | |
| A ₁ | .004 | .006 | 0.010 | |
| A ₂ | .055 | .058 | .061 | |
| B | .0138 | .061 | .020 | |
| C | .0075 | .008 | .0098 | |
| D | See Variations | | | 1 |
| E | .150 | .155 | .157 | |
| e | .050 BSC | | | |
| H | .230 | .236 | .244 | |
| h | .010 | .013 | .016 | |
| L | .016 | .025 | .035 | |
| N | See Variations | | | 2 |
| α° | 0° | 5° | 8° | |
| Variations | | | | |
| | 1 | | | 2 |
| | D | | | N |
| Note | Min. | Nom. | Max. | |
| AA | .189 | .194 | .196 | 8 |
| AB | .337 | .342 | .344 | 14 |
| AC | .386 | .391 | .393 | 16 |

NOTES:

1. Maximum die thickness allowable is .015.
2. Dimensioning and tolerances per ANSI.Y14.5M - 1982.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Formed leads shall be planar with respect to one another within .003 inches at seating plane.
6. Country of origin location and ejector pin on package bottom is optional and depend on assembly location.
7. Controlling dimension: inches.

| |
|--------------------------|
| Drawn: PJ 10/28/03 |
| CAD Dwg. No. 6000209.DWG |
| Ref Dwg. No. |
| Drawing Number\CAD File |
| 6000209 |
| Rev. D |
| Scale: |
| Sheet |

SOIC150
8, 14, 16 LEAD



AMI SEMICONDUCTOR, Inc.
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10.0 Soldering

10.1 Introduction to Soldering Surface Mount Package

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed circuit board;
 - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 8: Soldering Process

| Package | Soldering Method | |
|---------------------------------|------------------------|------------|
| | Wave | Reflow (1) |
| BGA, SQFP | Not suitable | Suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | Not suitable (2) | Suitable |
| PLCC (3), SO, SOJ | Suitable | Suitable |
| LQFP, QFP, TQFP | Not recommended (3)(4) | Suitable |
| SSOP, TSSOP, VSO | Not recommended (5) | Suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."
2. These packages are not suitable for wave soldering as a solder joint between the printed circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

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