1.0 General Description

The new AMIS-41682 and AMIS-41683 are interfaces between the protocol controller and the physical wires of the bus lines in a control area network (CAN). AMIS-41683 is identical to the AMIS-41682 but has a true 3.3V digital interface to the CAN controller. The device provides differential transmit capability but will switch in error conditions to a single-wire transmitter and/or receiver. Initially it will be used for low speed applications, up to 125kBaud, in passenger cars.

Both AMIS-41682 and AMIS-41683 are implemented in I2T100 technology enabling both high-voltage analog circuitry and digital functionality to co-exist on the same chip.

These products consolidate the expertise of AMIS for in-car multiplex transceivers and support together with AMIS-30522 (VAN), AMIS-30660 and AMIS-30663 (CAN High Speed) and AMIS-30600 (LIN) another widely used physical layer.

2.0 Key Features

- Fully compatible with ISO11898-3 standard
- Optimized for in-car low-speed communication
  - Baud rate up to 125kBaud
  - Up to 32 nodes can be connected
  - Due to built-in slope control function and a very good matching of the CANL and CANH bus outputs, this device realizes a very low electromagnetic emission (EME)
  - Fully integrated receiver filters
  - Permanent dominant monitoring of transmit data input
  - Differential receiver with wide common-mode range for high electromagnetic susceptibility (EMS) in normal- and low-power modes
  - True 3.3V digital I/O interface to CAN controller for AMIS-41683 only
- Management in case of bus failure
  - In the event of bus failures, automatic switching to single-wire mode, even when the CANH bus wire is short circuited to VCC
  - The device will automatically reset to differential mode if the bus failure is removed
  - During failure modes there is full wake-up capability.
  - Un-powered nodes do not disturb bus lines
  - Bus errors and thermal shutdown activation is flagged on ERRB pin
- Protection issues
  - Short circuit proof to battery and ground
  - Thermal protection
  - The bus lines are protected against transients in an automotive environment
  - An un-powered node does not disturb the bus lines
- Support for low power modes
  - Low current sleep and standby mode with wake-up via the bus lines
  - Power-on flag on the output
  - Two-edge sensitive wake-up input signal via pin WAKEB
- IOs
  - The un-powered chip cannot be parasitically supplied either from digital inputs nor from digital outputs.

3.0 Technical Characteristics

Table 1: Technical Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CANH}	DC voltage at pin CANH, CANL	0 < VCC < 5.25V; no time limit	-40	+40	V
Vbat	Voltage at pin Vbat	Load-dump		+40	V

4.0 Ordering Information

Table 2: Ordering information

Marketing Name	Package	Temp.Range
AMIS41682NGA	SOIC-14 GREEN	-40°C…125°C
AMIS41683NGA	SOIC-14 GREEN	-40°C…125°C

5.0 Block Diagram

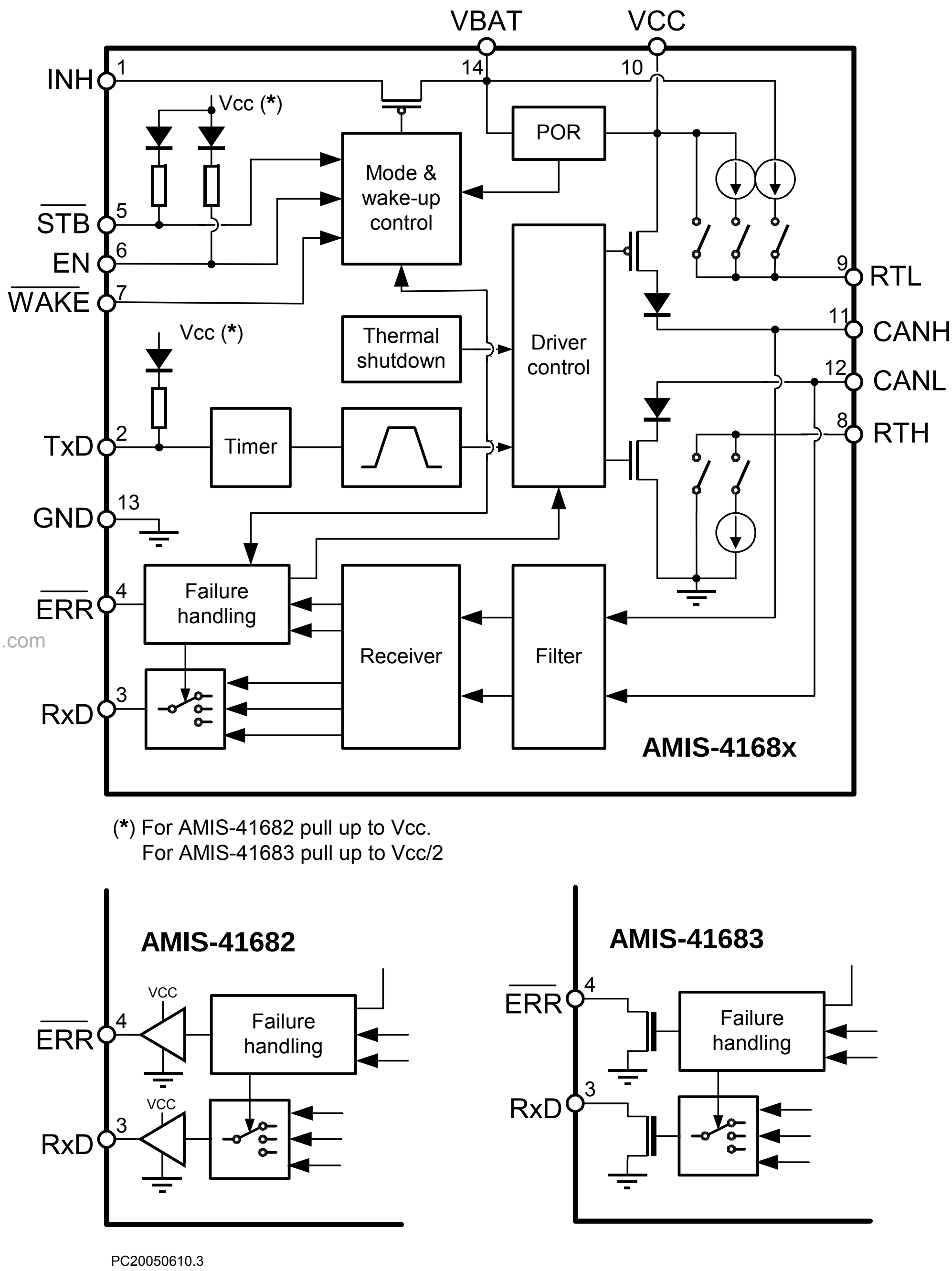


Figure 1: Block Diagram

6.0 Typical Application Schematic

6.1. Application Schematic

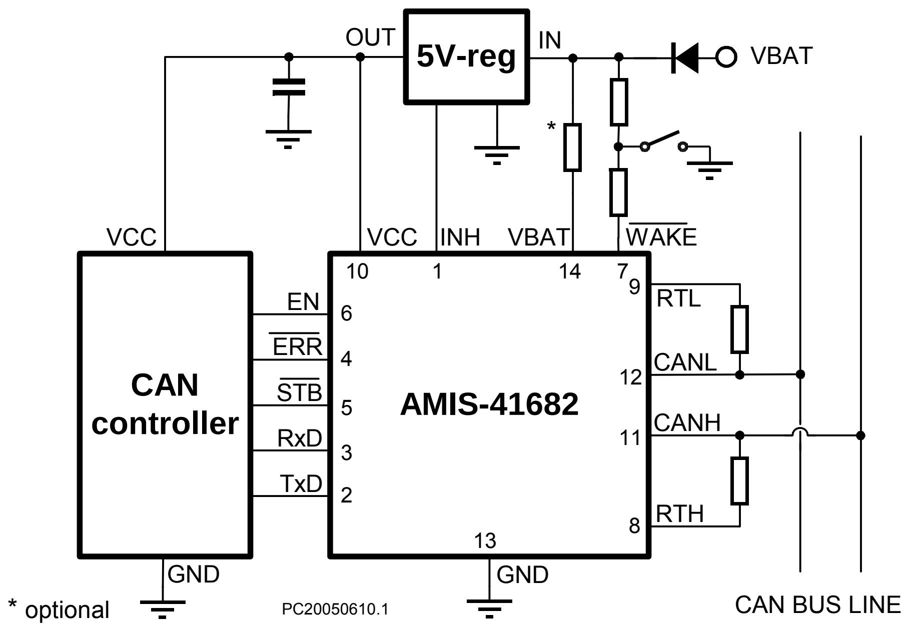


Figure 2: Application Diagram AMIS-41682

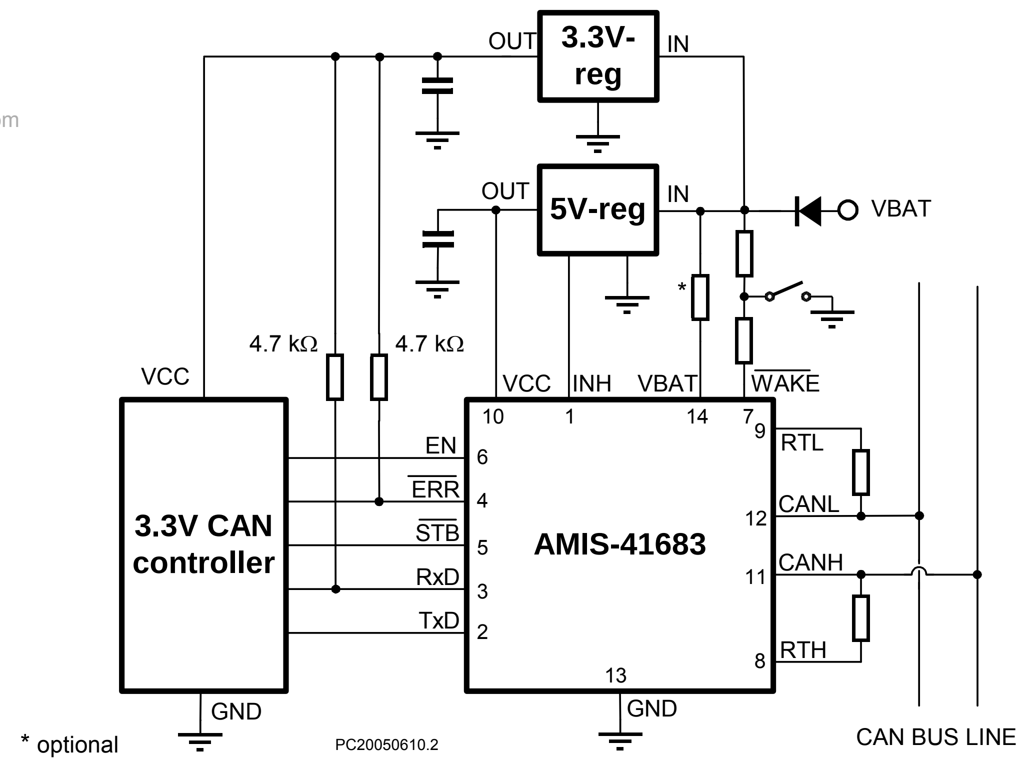


Figure 3: Application Diagram AMIS-41683

6.2. Pin Description

6.2.1. Pin Out (top view)

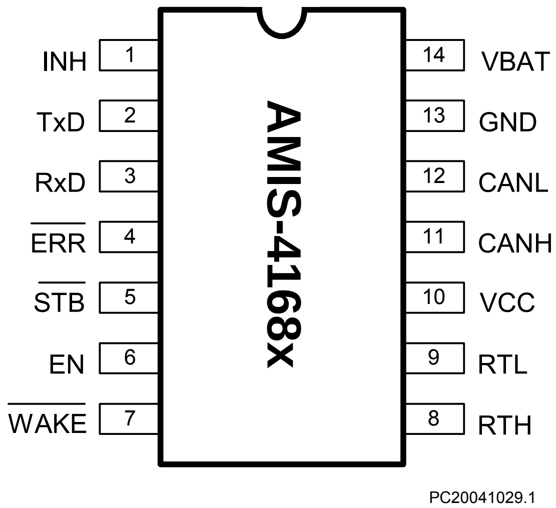


Figure 4: Pin Configuration

6.2.2. Pin Description

Table 3: Pin Description

Pin	Name	Description
1	INH	Inhibit output for external voltage regulator
2	TxD	Transmit data input; internal pull-up current
3	RxD	Receive data output
4	ERR-B	Error; wake-up and power-on flag; active low
5	STB-B	Standby digital control input; active low; pull-down resistor
6	EN	Standby digital control input; active high; pull-down resistor
7	WAKEB	Enable digital control input; falling and rising edges are both detected
8	RTH	Pin for external termination resistor at CANH
9	RTL	Pin for external termination resistor at CANL
10	Vcc	5V supply input
11	CANH	Bus line; high in dominant state
12	CANL	Bus line; low in dominant state
13	GND	Ground
14	BAT	Battery supply

Functional description and characteristics are made for AMIS-41682 but are also valid for AMIS-41683. Differences between the two devices will be explicitly mentioned in text.

7.0 Functional Description

7.1. Description

AMIS-41682 is a fault tolerant CAN transceiver which works as an interface between the CAN protocol controller and the physical wires of the CAN bus (see Figure 2). It is primarily intended for low speed applications, up to 125kBaud, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

The AMIS-41683 has open-drain outputs (RXD and ERR-B pins) that allow the user to use external pull-up resistors to the required supply voltage; this can be 5V or 3.3V.

To reduce EME, the rise and fall slope are limited. Together with matched CANL and CANH output stages, this allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines.

The failure detection logic automatically selects a suitable transmission mode, differential or single-wire transmission. Together with the transmission mode, the failure detector will configure the output stages in such a way that excessive currents are avoided and that the circuit returns to normal operation when the error is removed.

A high common-mode range for the differential receiver guarantees reception under worst case conditions and together with the integrated filter the circuit realizes an excellent immunity against EMS. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode.

A timer has been integrated at pin TXD. This timer prevents the AMIS-41682 from driving the bus lines to a permanent dominant state.

7.2. Failure Detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode. The different wiring failures are depicted in Figure 5. The figure also indicates the effect of the different wiring failures on the transmitter and the receiver. The detection circuit itself is not depicted.

The differential receiver threshold voltage is typically set at 3V (VCC = 5V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 4, and 6a. These failures, or recovery from them, do not destroy ongoing transmissions. During the failure, reception is still done by the differential receiver and the transmitter stays fully active.

To avoid false triggering by external RF influences the single-wire modes are activated after a certain delay time. When the bus failure disappears for another time delay, the transceiver switches back to differential mode. When one of the bus failures 3, 5, 6, 6a, and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and the respective output stage. A wake-up from sleep mode via the bus is possible either via a dominant CANH or CANL line. This ensures that a wake-up is possible even if one of the failures 1 to 7 occurs. If any of the wiring failure occurs, the output signal on pin ERRB will become low. On error recovery, the output signal on pin ERRB will become high again.

During all single-wire transmissions, the EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In the single-wire mode, LF noise cannot be distinguished from the required signal.

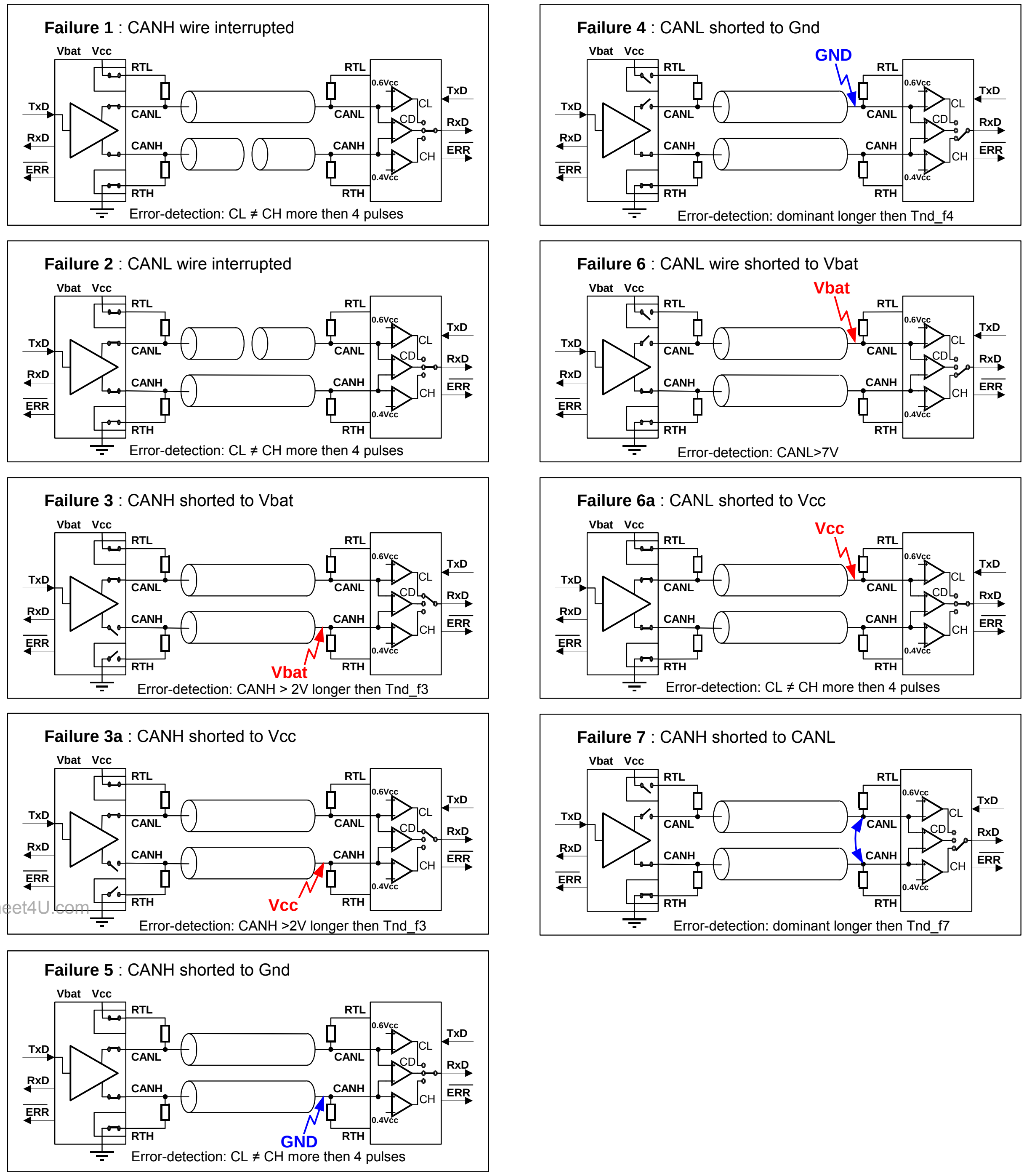


Figure 5: Different Types of Wiring Failure

7.3. Low Power Modes

The transceiver provides three low power modes that can be entered and exited via pins STBB and EN (see Figure 6). (Go-to-sleep mode is only a transition mode.)

The sleep mode is the mode with the lowest power consumption. Pin INH is switched to high-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. If the supply voltage is provided, pins RXD and ERRB will signal the wake-up interrupt signal.

The standby mode will react the same as the sleep mode but with a high-level on pin INH.

The power-on standby mode is the same as the standby mode with the battery power-on flag instead of the wake-up interrupt signal on pin ERRB. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

Wake-up request is detected by the following events:

- Local wake-up: Rising or falling edge on input WAKEB (Levels maintained for a certain period).
- Remote wake-up from CAN bus : A message with five consecutive dominant bits.

On a wake-up request the transceiver will set the output on pin INH high which can be used to activate the external supply voltage regulator. Note: Pin INH is also set similar as an after wake up event by V_{BAT} voltage being below the battery power on flag level. See FLAG_V_{BAT} in Table 6)

If VCC is provided, the wake-up request can be read on the ERR-B or RXD outputs so the external microcontroller can wake-up the transceiver (switch to normal operating mode) via pins STB-B and EN.

In the low power modes the failure detection circuit remains partly active to prevent increased power consumption in the event of failures 3, 3a, 4, and 7.

The go-to-sleep-mode is only a transition mode. The pin INH stays active for a limited time. During this time the circuit can still go to another low-power mode. After this time the circuit goes to the sleep-mode. In case of a wake up request (from BUS or WAKEB pin) during this transition time, the wake up request ha higher priority than go-to-sleep and INH will not be deactivated.

Once VCC is below the threshold level of LAG_Vcc , the signals on pins STB-B and EN will internally be set to low-level to provide fail safe functionality.

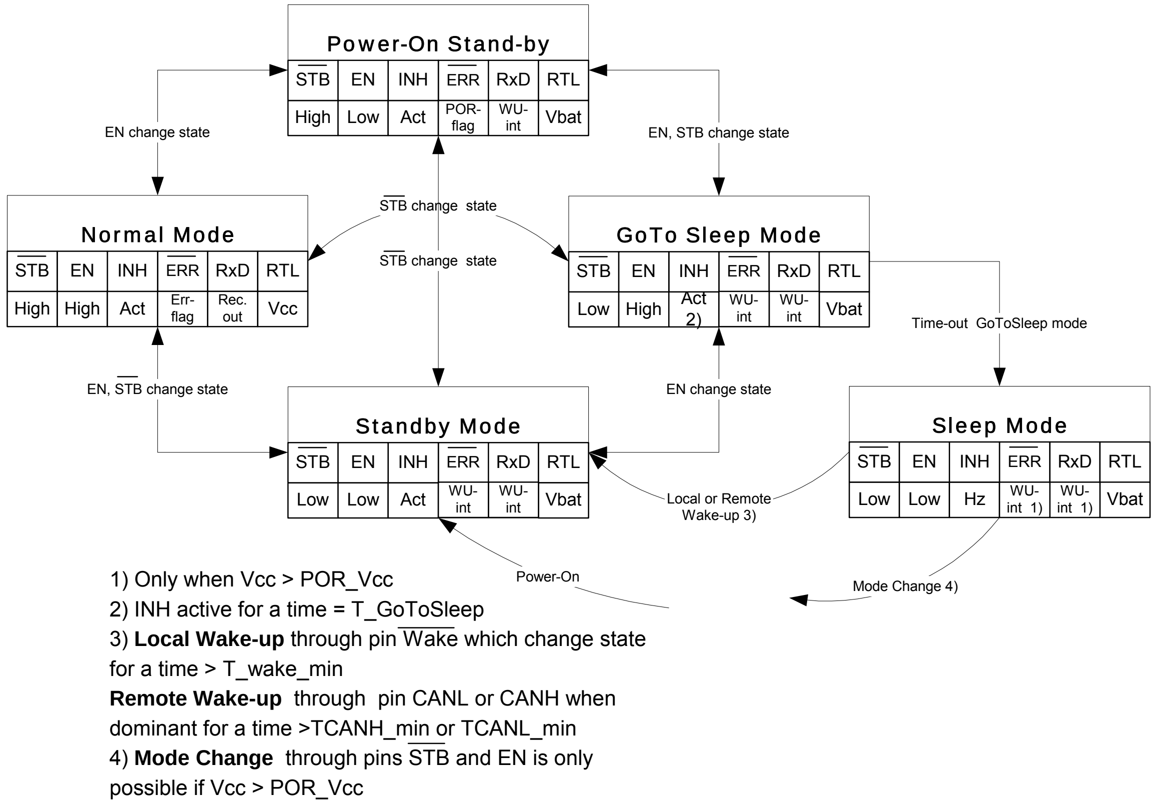


Figure 6: Low Power Modes

7.4. Power-on

After power-on (VBAT switched on) the signal on pin INH will become high and an internal power-on flag will be set. This flag can be read in the power-on standby mode via pin ERRB (STB-B = 1; EN = 0) and will be reset by entering the normal operating mode.

7.5. Protections

A current limiting circuit protects the transmitter output stages against short circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled and flagged on ERRB pin. Because the transmitter is responsible for the major part of the power dissipation, this will result in reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operating.

The pins CANH and CANL are protected against electrical transients that may occur in an automotive environment.

8.0 Electrical Characteristics

8.1. Definitions

All voltages are referenced to GND (pin 13). Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

8.2. Absolute Maximum Ratings

Stresses above those listed in this clause may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage on pin VCC	-0.3	+6	V
VBAT	Battery voltage on pin BAT	-0.3	+40	V
Vdig	DC voltage on pins EN, STB-B, ERR-B, TxD, RxD	-0.3	VCC + 0.3	V
VCANH-L	DC voltage on pin CANH, CANL	-40	+40	V
Vtran-CAN	Transient voltage on pins CANH and CANL (Figure 11) note 1	-350	+350	V
VWAKE	DC input voltage on pin WAKE	-40	+40	V
VINH	DC output voltage on pin INH	-0.3	VBAT + 0.3	V
VRTH-L	DC voltage on pin RTH , RTL	-40	40	V
RRTH	Termination resistance on pin RTH	500	16000	Ω
RRTL	Termination resistance on pin RTL	500	16000	Ω
Tjunc	Maximum junction temperature	-40	+150	ºC
Vesd	Electrostatic discharge voltage (CANH- and CANL pin) HBM; note 2	-6	+6	kV
	Electrostatic discharge voltage (other pins) HBM; note 2	-3.0	+3.0	kV
	Electrostatic discharge voltage; machine model; note 3	-500	+500	V

Notes:
1. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. Class C operation
2. Equivalent to discharging a 100pF capacitor through a 1.5kOhm resistor.
3. Equivalent to discharging a 200pF capacitor through a 10Ohm resistor and a 0.75µH coil.

8.3. Thermal Characteristics

Table 5: Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
Rth(vj-a)	Thermal resistance from junction to ambient in SSOP14 package (2 layer PCB)	In free air	140	K/W
Rth(vj-s)	Thermal resistance from junction to substrate of bare die	In free air	30	K/W

8.4. Characteristics

V_{CC} = 4.75V to 5.25V; V_{BAT} = 5V to 36V; T_{junc} = –40°C to +150°C; unless otherwise specified.

Table 6: Characteristics AMIS-4168x

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies Vcc Vbat						
ICC	Supply current	Normal operating mode; VTXD = VCC (recessive)	1	3.7	6.3	mA
		Normal operating mode; VTXD = 0V (dominant); no load	1	8	12	mA
LAG_Vcc	Forced low power mode	VCC rising VCC falling	 2.45		4.5 	V V
IBAT	Battery current on pin BAT	In all modes of operation; 500Ω between RTL - CANL 500Ω between RTH - CANH VBAT = WAKE = INH = 5 to 36V	10	110	230	µA
ICC+ IBAT	Supply current plus battery current	Low power modes; Vcc = 5V; Tamb = -40°C to 100°C VBAT = WAKE = INH = 5 to 36V		30	60	µA
ICC+ IBAT	Supply current plus battery current	Low power modes; Vcc = 5V; Tamb = 100°C to 150°C VBAT = WAKE = INH = 5 to 36V			80	µA
FLAG_VBAT	Power-on flag-level for pin Vbat	For setting power-on flag For not setting power-on flag	 3.5	2.1 2.4	1 	V V
Pins STB-B, EN and TXD						
R-PD	Pull-down resistor at pin EN and STB-B	1V	190	360	600	KΩ
T_Dis_TxD	Dominant time-out for TxD	Normal mode; VtxD = 0V	0.75		4	ms
T_GoToSleep	Minimum hold-time for Go-To-Sleep mode		5		50	µs
Pin WAKE-B						
IIL	Low-level input current	VWAKE = 0V; VBAT = 27V	-10		-1	µA
Vth(WAKE)	Wake-up threshold voltage	VSTB-B = 0V	2.5	3.2	3.9	V
T_Wake_Min	Minimum time on pin wake (debounce time)	VBAT = 12V; low power mode; for rising and falling edge	7		38	µs
Pin INH						
Delta_VH	High-level voltage drop	IINH = 0.18mA			0.8	V
I_leak	Leakage current	Sleep mode; VINH = 0V			1	µA

Table 7: Characteristics AMIS-41682 (5V version)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pins STB-B, EN and TXD						
VIH	High-level input voltage		0.7 x Vcc		6.0	V
VIL	Low-level input voltage		-0.3		0.3 x Vcc	V
I-PU-H	High-level input current pin TXD	TXD = 0.7 * Vcc	-10		-200	µA
I-PU-L	Low-level input current pin TXD	TXD = 0.3 * Vcc	-80		-800	µA
Pins RXD and ERR-B						
VOH	High-level output voltage	Isource = -1mA	VCC - 0.9		VCC	V
VOL	Low-level output voltage	Isink = 1.6mA Isink = 7.5mA	0 0		0.4 1.5	V V

Table 8: Characteristics AMIS-41683 (3.3V version)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pins STB-B, EN and TXD						
VIH	High-level input voltage		2		6.0	V
VIL	Low-level input voltage		-0.3		0.8	V
I-PU-H	High-level input current pin TXD	TXD = 2V		-10		µA
Pins RXD and ERR-B						
VOL	Low-level output voltage open drain	Isink = 3.2mA			0.4	V
I_leak	Leakage when driver is off	VERR-B = VRXD = 5V			1	µA

Table 9: Characteristics AMIS-4168x continued

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pins CANH and CANL (Receiver)						
Vdiff	Differential receiver threshold voltage	No failures and bus failures 1, 2, 4, and 6a; see Figure 5 VCC = 5V VCC = 4.75V to 5.25V	-3.25 0.65 x Vcc	-3 0.6 x Vcc	-2.75 0.55 x Vcc	V V
VseCANH	Single-ended receiver threshold voltage on pin CANH	Normal operating mode and failures 4, 6 and 7 VCC = 5V VCC = 4.75 to 5.25V	1.6 0.32 x Vcc	1.775 0.355 x Vcc	1.95 0.39 x Vcc	V V
VseCANL	Single-ended receiver threshold voltage on pin CANL	Normal operating mode and failures 3 and 3a VCC = 5V VCC = 4.75 to 5.25V	3 0.61 x Vcc	3.2 0.645 x Vcc	3.4 0.68 x Vcc	V V
Vdet(CANL)	Detection threshold voltage for short circuit to battery voltage on pin CANL	Normal operating mode	6.5	7.3	8	V
Vth(wake)	Wake-up threshold voltage On pin CANL On pin CANH	Low power modes Low power modes	2.5 1.1	3.2 1.8	3. 9 2.25	V V
DVth(wake)	Difference of wake-up Threshold voltages	Low power modes	0.8	1.4		V
Pins CANH and CANL (Transmitter)						
VO(reces)	Recessive output voltage On pin CANH On pin CANL	VTXD = VCC RRTH < 4kΩ RRTL < 4kΩ	Vcc - 0.2		0.2	V V
VO(dom)	Dominant output voltage On pin CANH On pin CANL	VTXD = 0V; VEN = VCC ICANH = -40mA ICANL = 40mA	Vcc - 1.4		1.4	V V
IO(CANH)	Output current on pin CANH	Normal operating mode; VCANH = 0V; VTXD = 0V	-110	-80	-45	mA
		Low power modes; VCANH = 0V; VCC = 5V	-1.6	0.5	1.6	μA
IO(CANL)	Output current on pin CANL	Normal operating mode; VCANL = 14V; VTXD = 0V	45	80	110	mA
		Low power modes; VCANL = 12V; VBAT = 12V	-1	0.5	1	μA
Pins RTH and RTL						
Rsw(RTL)	Switch-on resistance between pin RTL and VCC	Normal operating mode; I(RTL)> -10mA			100	Ω
Rsw(RTH)	Switch-on resistance between pin RTH and ground	Normal operating mode; I(RTH)< 10mA			100	Ω
VO(RTH)	Output voltage on pin RTH	Low power modes; IO = 1mA			1.0	V
IO(RTL)	Output current on pin RTL	Low power modes; VRTL = 0V	-1.25		-0.3	mA
Ipu(RTL)	Pull-up current on pin RTL	Normal operating mode and failures 4, 6 and 7; VRTL= 0V		-75		μA
Ipd(RTH)	Pull-down current on pin RTH	Normal operating mode and failures 3 and 3a		-75		μA
Thermal Shutdown						
Tj	Junction temperature	For shutdown	150		180	°C

8.5. Timing Characteristics

V_{CC} = 4.75V to 5.25V; V_{BAT} = 5V to 27V; V_{STB-B} = V_{CC}; T_{junc} = –40°C to +150°C; unless otherwise specified.

Table 10: Timing Characteristics AMIS-4168x

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tt(r-d)	CANL and CANH output transition time for recessive-to-dominant	10 to 90%; C1 = 10nF; C2 = 0; R1 = 125Ω; see Figure 7	0.35	0.60	1.4	µs
tt(d-r)	CANL and CANH output transition time for dominant-to-recessive	10 to 90%; C1 = 1nF; C2 = 0; R1 = 125Ω; see Figure 7	0.2	0.3	0.7	µs
tPD(L)	Propagation delay TXD to RXD (LOW)	No failures C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 0.75 1.4	 1.5 2.1	 µs µs
		Failures 1, 2, 5, and 6a; see Figure 5, 7 C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 1.2 1.4	 1.9 2.1	 µs µs
		Failures 3, 3a, 4, 6, and 7; see Figure 5, 7 C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 1.2 1.5	 1.9 2.2	 µs µs
tPD(H)	Propagation delay TXD to RXD (HIGH)	No failures C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 0.75 2.5	 1.5 3.0	 µs µs
		Failures 1, 2, 5, and 6a; see Figure 5, 7 C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 1.2 2.5	 1.9 3.0	 µs µs
		Failures 3, 3a, 4, 6, and 7; see Figure 5, 7 C1 = 1nF; C2 = 0; R1 = 125Ω C1 = C2 = 3.3nF; R1 = 125Ω		 1.2 1.5	 1.9 2.2	 µs µs
tCANH(min)	Minimum dominant time for wake-up on pin CANH	Low power modes; VBAT = 12V	7		38	µs
tCANL(min)	Minimum dominant time for wake-up on pin CANL	Low power modes; VBAT = 12V	7		38	µs
tdet	Failure detection time	Normal mode Failure 3 and 3a Failure 4, 6 and 7	 1.6 0.3		 8.0 1.6	 ms ms
		Low power modes; VBAT = 12V Failure 3 and 3a Failure 4 and 7	 1.6 0.1		 8.0 1.6	 ms ms
trec	Failure recovery time	Normal mode Failure 3 and 3a Failure 4 and 7 Failure 6	 0.3 7 125		 1.6 38 750	 ms µs µs
		Low power modes; VBAT = 12V Failures 3, 3a, 4, and 7	 0.3		 1. 6	 ms
Dpc	Pulse-count difference between CANH and CANL	Normal mode and failures 1, 2, 4, and 6a Failure detection (pin ERR-B becomes LOW) Failure recovery (pin ERR-B becomes HIGH)		 4 4		 - -

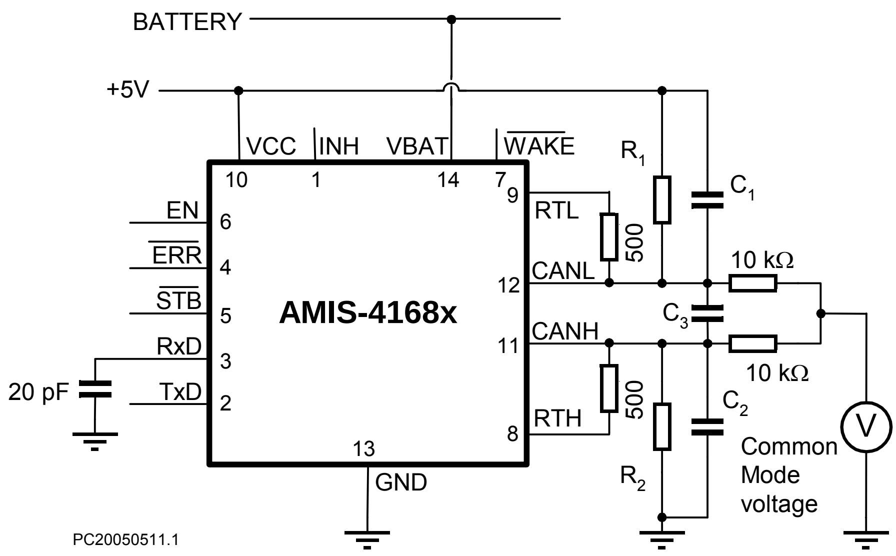


Figure 7: Test Circuit for Dynamic

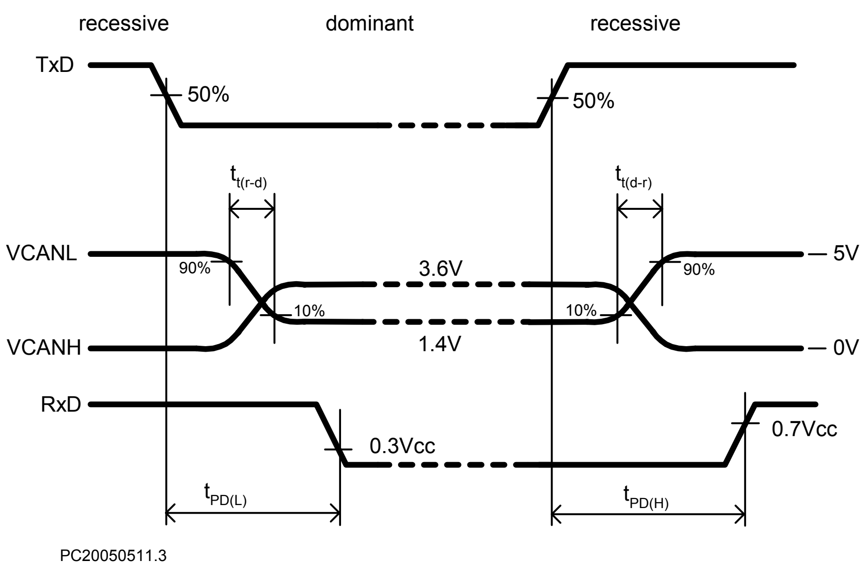


Figure 8: Timing Diagram for AC Characteristics

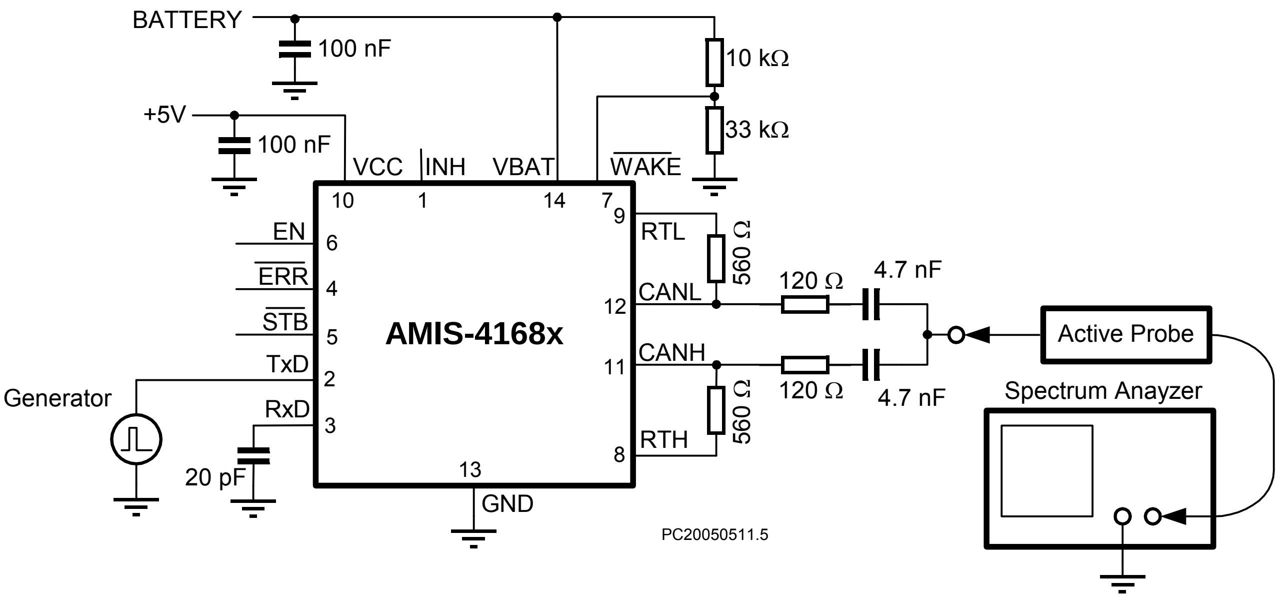


Figure 9: Test Setup EME Measurements

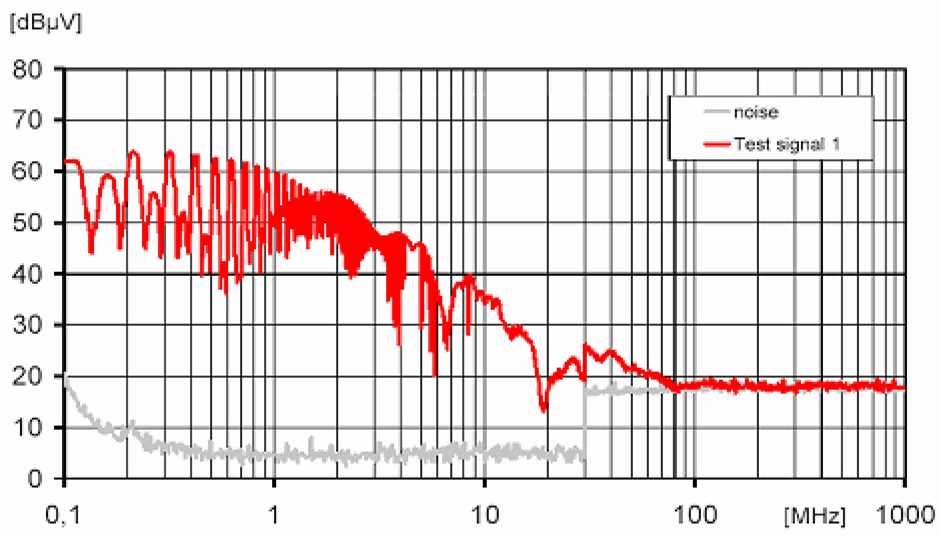


Figure 10: EME Measurements (See Measurement Setup Figure 9)

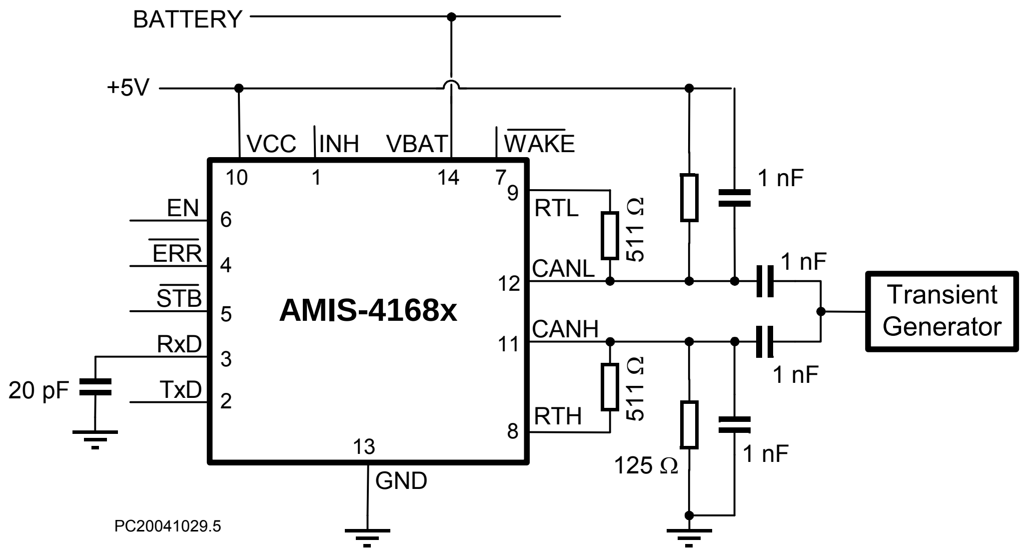
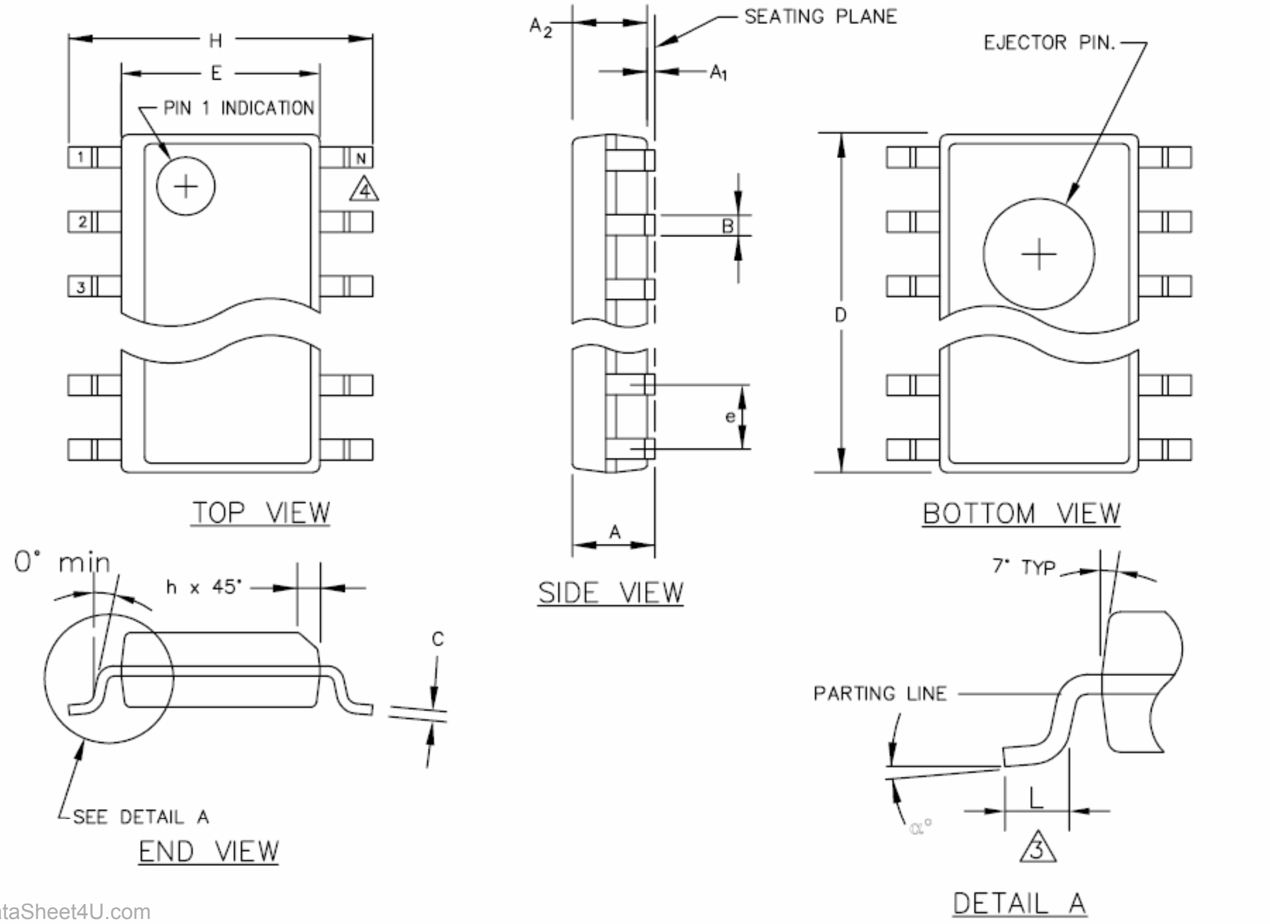


Figure 11: Test Circuit for Schaffner Tests (ISO 7637 part

9.0 Package Outline

SOIC-14: Plastic small outline; 14 leads; body width 150 mil; JEDEC: MS-012 AMIS reference: SOIC150 14 150 G



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS				
	1			2
	D			N
NOTE	MIN.	NOM.	MAX.	
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M – 1982.
3. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
4. "N" IS THE NUMBER OF TERMINAL POSITIONS.
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
6. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
7. CONTROLLING DIMENSION: INCHES.

Drawn:	PJ 10/28/03
CAD Dwg. No.	6000209.DWG
Ref Dwg. No.	
Drawing Number\CAD File	6000209
Rev.	D
Scale:	
Sheet	

SOIC150
8, 14, 16 LEAD

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10.0 Soldering

10.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical re-flow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed.
If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45º angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 11: Soldering Process

Package	Soldering Method	
	Wave	Re-flow(1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:
1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

11.0 Company or Product Inquiries

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