1.0 Introduction

The AMIS-52000 is a low cost, ultra low power ASK/OOK (Amplitude Shift Keying/On-Off Shift Keying) transceiver intended for narrow band RF applications. The device is targeted for applications at 433MHz but can operate from 260 to 700MHz. The adjustable RF output ranges from –26 to +6dBm into a matched 50ohm load. The receiver contains two independent receive channels which can be connected to separate antennas for antenna diversity applications.

On chip trim registers eliminate manual trimming of external components. Using the on chip trimming, transmit and receive frequencies achieve 5ppm accuracy over the entire voltage and temperature range.

2.0 Key Features

- Very low power single-chip transceiver
- Minimal external components
- Low power RC oscillator
- Unique Quick Start, low-noise oscillator (patent pending)
- Extreme low power RF Sniff Mode™, wake on RSSI
- Internal trim functions
- I^2C control interface
- Serial TX/RX data port
- Clock generation for an external microprocessor
- Wake up on RSSI
- Unique antenna diversity dual receiver (patent pending)
- Internal VCO/PLL tuning varactor

3.0 Technical Features

- Operating Frequency: Range 260 to 700MHz
- TX Output Power: +6dBm
- RX Sensitivity:
  - Sniff Mode: -93dBm minimum
  - Receive: -103dBm minimum @ 1Kbps
- Data Rate: 1 to 19.2Kbps, user selectable
- Power Requirements:
  - Receive: 7.5mA (continuous)
  - Transmit: 25mA full power; 50% duty cycle
  - Sniff Mode: 750µA at a 1ms sniff rate (10% duty cycle)
  - Standby: 500nA (RC oscillator running)
- Operating Voltage: 2.4 to 3.6V
- Modulation: ASK/OOK (Amplitude Shift Key/On-Off Shift Key)
- Xtal Start Time: 15µs (Quick Start)
- Sniff Mode Polling: 0.5ms to 16s (0.5ms or 64ms steps)
- PLL Lock Time: <50µs
- Selectable Data Filter: up to 19.2 Kbps
- Internal Trim Function:
  - TX power
  - Antenna for trim or tune (2 inputs are independent)
  - Xtal for frequency and quick start
  - RC for frequency
  - Sniff mode for data threshold
  - Data slice
- I^2C Interface: Control bus
- Serial Interface: Data input/output
- Low Frequency IF
- Internal IF Filtering
- Package: 20-lead, 209 m SSOP

4.0 Operating and Maximum Specifications

Table 1: Operating Conditions

Sym	Parameter	Min	Typ	Max	Units
VDD	Positive Supply	2.4	3.0	3.3	V
Vss	Ground		0.0	0.1	V
Temp	Temperature Range	0	+25	+50	C

Table 2: Absolute Maximum Ratings

Sym	Parameter	Min	Max	Units
VDD	Positive Supply		+3.6	V
RFin	Maximum RF Input RX1/RX2		+10	dBm
Vss	Ground	0.0	0.1	V
Vin	Logic I/P Voltage	-0.3	VDD+0.3	V
Tstrg	Storage Temp	-40	+120	C

Table 3: Electrical Characteristics Supply Current

Idd (Supply Current)	Max	Typ	
Sleep	1µA	500nA	
Receiving	10mA	7.5mA	
Transmitting	25mA	25mA	50% Duty Cycle

Table 4: Electrical Characteristics Digital Inputs

Parameter	Min	Typ	Max	Units
Vih	0.7*VDD			Volts
Vil			0.3*VDD	Volts
Iih			+1.0	µA
Iil	-1.0			µA
I^2C Internal Pullup		15	20	KΩ

Table 5: Electrical Characteristics Digital Outputs

Parameter	Min	Typ	Max	Units
Voh	0.8*VDD			Volts
Vol			0.4	Volts
Ioh			–1.0	mA
Iol	+1.0			mA
I^2C Internal Pullup		15	20	KΩ

Table 6: Electrical Characteristics
Analog TX

Parameter	Min	Typ	Max	Units	Comments
Frequency Range	260	433.92	700	MHz	
Modulation		ASK/OOK			Amplitude shift key on/off shift key
Modulation Frequency	1.2		19.2	KBaud	Approximate allowable data rates
Max Output Power	5	6	7	dBm	Over entire operating temperature and voltage range
On/Off Ratio		60		dB	
VCO Gain, Kvco		75		MHz/V	
PLL Phase Noise		-97		dBc/Hz	10kHz offset, 200kHz loop bandwidth
		-97		dBc/Hz	100kHz offset, 50kHz loop bandwidth
Harmonics		-35		dBc	With typical matching circuits at 433.92MHz
Reference Frequency	8.125	13.56	22.5	MHz	10 PPM Xtal
Crystal Frequency Spurs		-50		dBc	200kHz PLL loop bandwidth
TR Delay			1	ms	Transmit to receive delay

Table 7: Electrical Characteristics
Analog RX

Parameter	Min	Typ	Max	Units	Comments
Frequency Range	260	433.92	700	MHz	
Modulation		ASK/OOK			Amplitude shift key on/off shift key
Input Sensitivity	-103			dBm	10-3 BER, 1.2kbps
RF Detect Time	100			µs	Sniff Mode operation only
TR Delay			1	ms	Receiver to transmit delay

5.0 Pin Definitions

This section describes the pins of the AMIS-52000 package.

Table 8: Pin List

Pin #	Name	Type	Comments
1	RX1	RF	RF Receive Antenna Input 1
2	RX2	RF	RF Receive Antenna Input 2
3	VCO2	Ana	Voltage Controlled oscillator 2
4	VCO1	Ana	Voltage Controlled oscillator 1
5	LPFILT	Ana	Loop Filter
6	RSSI/Bandgap Out	Ana	Analog RSSI Output or Bandgap Output
7	NC		No connection
8	CREF	Ana	Current Bias Precision Resistor
9	GND	Ana	Analog/Digital Ground
10	CLKOUT	Dig	RC or XTAL Output
11	X1	Ana	Xtal Input
12	X2	Ana	Xtal Output
13	IIC Data	Dig	IIC Interface Data I/O
14	NC		No connection
15	IIC Clock	Dig	IIC Interface Clock
16	TX/RX Data	Dig	Data Transmit or Data Receive
17	VDD	Ana	Positive Power Supply
18	RFPWR	Ana	Regulated Voltage Output for RF Transmitter Circuitry
19	RFOUT	RF	RF Transmit Antenna Output
20	RFGND	Ana	RF Ground

Type Codes … Ana – Analog Dig – Digital RF – Radio Frequency

6.0 Package Outline

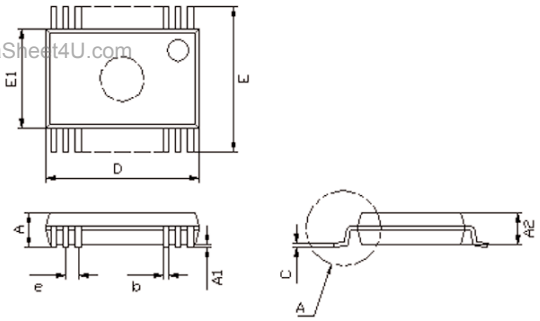

Figure 1 – AMIS-52000 SSOP Package Dimensions

Table 9: Package Dimensions

	Inches		Millimeters	
Dm	Min	Max	Min	Max
A	0.068	0.078	1.73	2.00
A1	0.002	0.20	0.05	
A2	0.065	0.073	1.65	1.85
b	0.009	0.015	0.22	0.38
D	0.271	0.295	6.90	7.50
E	0.291	0.323	7.40	0.820
E1	0.197	0.221	5.00	0.560
e	0.026 BSC		0.65 BSC	

7.0 Pin Descriptions

RX1, RX2, RF Inputs

RX1 and RX2 are RF antenna inputs to the AMIS-52000. The internal design of these circuits is identical. Each internal circuit can be trimmed to compensate for device process tolerances and external component tolerances. The first stage of the RF input is an LNA (Low Noise Amplifier). The receiver uses a low IF frequency and internal filters. The two inputs are "summed" before the data recovery circuit.

The receiver uses an RSSI (Receive Signal Strength Indication) to recover the ASK/OOK (Amplitude Shift Keyed/On Off Shift Keyed) modulated data.

The receiver is controlled by writing to the internal registers of the AMIS-52000:

Table 10: Pin Descriptions

RX1 or RX2 Receiver Control (Registers 0x05, 0x0F and 0x17)				
Register	**Bit**	**Bit Name**	**Bit State**	**Comments**
Register 0x05	0	Antenna #1 Enable	0	Receive circuits (RX1) are off
			1	Receive circuits (RX1) are controlled by Bit 3
	1	Antenna #2 Enable	0	Receive circuits (RX2) are off
			1	Receive circuits (RX2) are controlled by Bit 3
	3	RX Enable	0	Receiver is disabled (off)
			1	Receiver is enabled (on)
Register 0x0F	53	Continuous RX	0	Normal operation
			1	RF receiver is turned on
Register 0x17 & Register 0x05	Register 0x17 Bit 6 & 7	Data Rate Cntl	000	Set Data filter to 1.1kHz
			001	Set Data filter to 2.3kHz
			010	Set Data filter to 5.2kHz
			011	Set Data filter to 10.4kHz
	Register 0x05 Bit 2	BIT Order Bit 7 msb Bit 2 lsb	100	Set Data filter to 1.18kHz
			101	Set Data filter to 2.57kHz
			110	Set Data filter to 7.0kHz
			111	Set Data filter to 20.45kHz

TX/RX, Data Input/Output

The TX/RX pin (in transmit operation) is the digital data input to the AMIS-52000's transmit circuits. The data is used to turn the transmitter on or off. The AMIS-52000 does not perform protocol conversion to the data. It simply transmits when transmission is enabled. The state (low input or high input) that causes the AMIS-52000 to transmit is programmable.

The TX/RX pin (in receive) is the digital data output from the AMIS-52000 receiver. The received data is formed into high and low signals (ones and zeros) in a serial bit stream. The data output state (pin TX/RX) produced by the AMIS-52000 receiver due to the presence of RF energy at the RX input can be programmed to be either a high level or a low level. An external controller must recreate the actual information.

The TX/RX pin (can be programmed to be the oscillator output) is the RC oscillator frequency. An external test system can use this signal in a feedback loop to trim the RC oscillator frequency.

The TX/RX pin (during the Sniff or signal capture period) is an indicator (to a host controller) output that either the AMIS-52000 receiver has detected RF energy when the device is powered down with Sniff Mode enabled or the internal housekeeping timer has expired. When TX/RX is used in this mode the I^2C data line will be high when RF energy is detected or low when the housekeeping timer activates the device. Depending on the bit period time, this acquisition could occur on the first bit of data and still receive the bit or it may require a pre-amble. The following timing chart shows the function of this pin in signal acquisition and Sniff Modes.

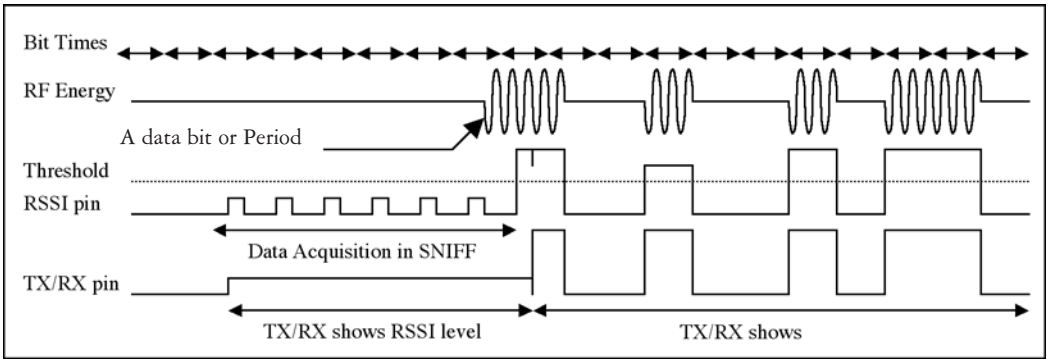

Figure 2: Receiver Data Acquisition Waveforms

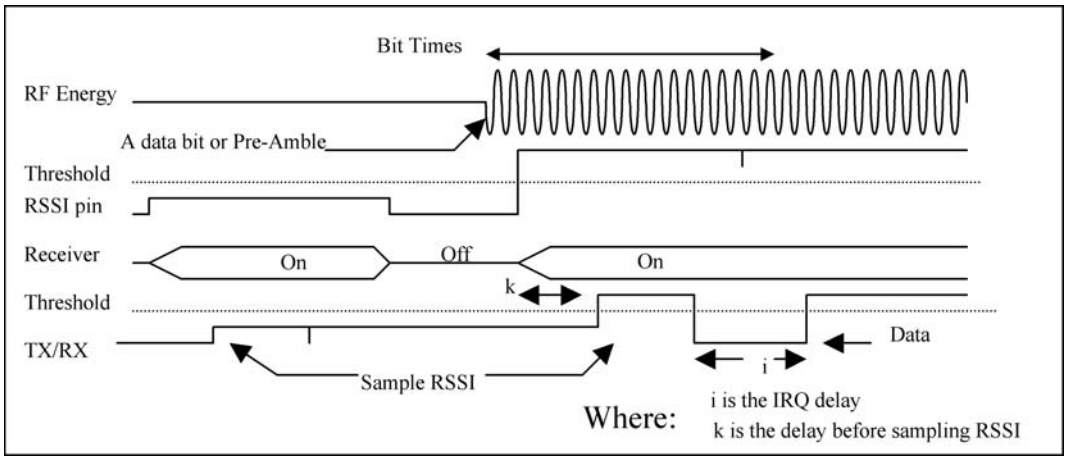

Figure 3: Receiver Acquisition Bit Function Timing
Where: i is a delay allowing pins function to change to signal the HOST controller that a RF caused wakeup occurred. It can be controlled by Reg 0x0E (IRQ Delay).
k (set by Reg 0x0B) is a delay allowing signal levels to settle before sampling RSSI.

The TX/RX pin can be programmed to perform one of these functions by writing to the AMIS-52000 internal registers.

Table 11: TX/RX Pin Definition Control (Registers 0x08, 0x0f and 0x17)

TX/RX Pin Definition Control (Registers 0x08, 0x0f, and 0x17)				
Register	**Bit**	**Bit Name**	**Bit State**	**Comments**
0x08	7	Sniff Out	0	Do not output Sniff on TX/RX pin
			1	Output Sniff comparator results on TX/RX
0x0F	2	RC Osc.	0	TX/RX pin is normal operation (DATA)
		Out	1	RC osc. clock is output on the TX/RX pin
0x17	5	TX/RX Inv	0	TX will output RF energy when TX/RX high
		Transmit	1	TX will output RF energy when TX/RX low
0x17	5	TX/RX Inv	0	RX is a high level when RF energy is received
		Receive	1	RX is a low level when RF energy is received
0x0E	All	IRQ Delay		Delay from TX/RX line signals a wakeup event to when the line returns to its normal function

VDD, Supply Voltage

The VDD pin is the supply voltage for the AMIS-52000 circuits other than the RF output. It is typically 3.0V DC. Please refer to section "Operating and Maximum Specifications" of this specification for operating conditions.

GND, Analog/Digital Ground

The GND pin is a ground connection for all non-RF circuitry.

RFGND, RF Ground

The RFGND pin is a ground connection for all the internal RF circuitry.

X1, X2, Crystal Oscillator

X1 and X2 connect a parallel resonance oscillator crystal and capacitors to the AMIS-52000. The AMIS-52000 is designed with an internal trim function that is controlled by writing to the AMIS-52000 registers.

Table 12: Crystal Divider Control

Reg	Name	Register Function
0x03	TX Crystal Trim	Changing the value of this changes the crystal frequency
0x04	RX Crystal Trim	Changing the value of this changes the crystal frequency

NOTE:
The value of the external crystal load capacitors should be slightly lower than for a typical crystal to allow for capacitor loading in the trim function.

LPFILT, Loop Filter

The LPFILT pin connects the AMIS-52000 internal PLL comparator to the external loop filter. The filter is required to allow the internal PLL to lock to the crystal frequency while producing the desired RF frequency. A simple second order RC loop filter is typically sufficient for this purpose.

VCO1, VCO2, Voltage Controlled Oscillator Tune

The VCO1 and VCO2 pins connect a parallel capacitor and inductor to the AMIS-52000 internal VCO (Voltage Controlled Oscillator). The LC circuit tunes the VCO frequency. The frequency of the VCO is twice the desired TX or RX frequency and the range of the VCO is 520MHz to 1400MHz.

CLKOUT, Internal Clock Output

The CLKOUT pin output is either the internal RC oscillator, the crystal oscillator, or a divided version of the crystal oscillator.

Table 13: Crystal Divider Control TX/RX Pin Definition Control (Registers 0x05 and 0x08)

Register	BIT	Bit Name	Bit State	Comments
Register 0x05	7	CLKOUT Enable	0	CLKOUT is enabled
			1	CLKOUT is disabled
Register 0x08	4 & 5	CLKOUT Output Select	00	Automatic control
			01	RC oscillator is output
			10	Xtal oscillator is output
			11	CLKOUT output is off
Register 0x0F	0 & 1	CLKOUT Frequency Select	00	Divide crystal by 4
			01	Divide crystal by 3
			10	Divide crystal by 2
			11	Divide crystal by 1

CREF, Current Reference Bias

The CREF pin requires a resistor to ground to set the bandgap BIAS CURRENT. IT IS CRITICAL THAT THE RESISTOR BE 33.2K OHMS, 1% or better tolerance.

R(Bias) = 33.2 KΩ (1%)

I^2CDATA, I^2CCLK, I^2C Control Interface Bus

The AMIS-52000 implements an I^2C serial 8 bit bi-directional interface with the pins I^2CDATA and I^2CCLK. The I^2C bus handshaking and protocol is implemented for a SLAVE device. Because only a minimal configuration is supported, clock stretching for slow peripherals, general call addressing, and ten-bit extended addressing are not implemented. The interface will support either normal (0 - 100 Kbits/second) or fast (0 - 400 Kbits/second) data modes. The interface conforms to the Phillips specification for the I^2C bus.

Pin	Function	Resistor	Units
I²CDATA	Internal Pullup	15	K ohms
I²CCLK	Internal Pullup	15	K ohms

Device	Address	Hex	Function
AMIS-52000	0110100X		Device address
AMIS-52000	01101000	68	Device write
AMIS-52000	01101001	69	Read device

The I²C pins are also used as part of the wake-up function of the AMIS-52000. When the AMIS-52000 is in power down or sleep mode, the I²CCLK line can be driven to a low state to wake the AMIS-52000. Then an external controller can interrogate the state of the I²CDATA line to determine whether a Sniff function detected RF (data high) or a HOUSEKEEPING timer timeout (data low).

RSSI/BG, Analog Output

The RSSI/BG pin outputs the analog RSSI signal. This signal is filtered by an internal parallel connection of a resistor and capacitor to ground.

The RSSI/BG pin (when programmed to be) outputs the voltage of the internal Bandgap voltage reference.

Each of these functions for the RSSI/BG pin can be selected by writing to the AMIS-52000 registers.

Table 14: RSSI/BG Analog Pin Definition Control (Registers 0x0F and 0x17)

Register	Bit	Bit Name	Bit State	Comments
0x0F	3	RSSI or Bandgap	0	RSSI signal output (Pre Data Filter)
		Output	1	Bandgap voltage is output

8.0 Functional Design Description

The AMIS-52000 is a dual receiver and a transmitter in a single device. Data is transmitted at data rates up to 19.6Kbps. The AMIS-52000 can be used in half-duplex mode, or simplex mode. Control is provided by an external microprocessor. Power output adjust, frequency trim, filter bandwidth selection, antenna or receiver diversity selection and crystal divider values can be changed to compensate for device tolerances. The transmit section of the AMIS-52000 generates the output carrier signal when the TX/RX pin is toggled to enable the RF carrier. RF output power is controlled by setting register TXPOWER (0x02) to some value, setting a DC voltage level on the pin RFPWR (0x00 is the lowest setting and 0xFF is the highest setting). The receive section of the AMIS-52000 is configured to accept the input signals from either or both of the two antennas. The detected signals are summed inside the receiver, providing the received digital signal output. The receiver operates as a very low IF superheterodyne receiver with internal filtering.

AMIS-52000 Block Diagram

This section shows a typical design with external components for 433.92MHz operation. The following sections will describe each external circuit.

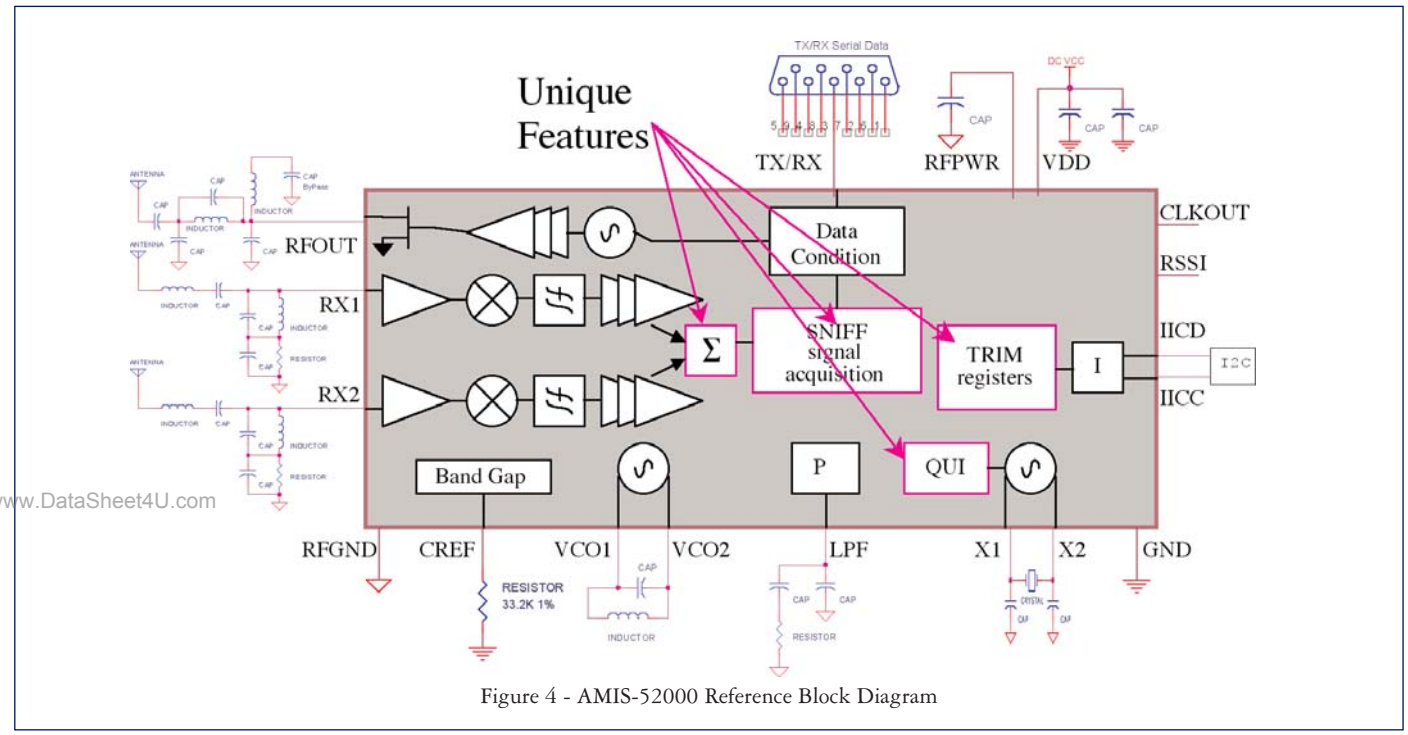

Figure 4 - AMIS-52000 Reference Block Diagram

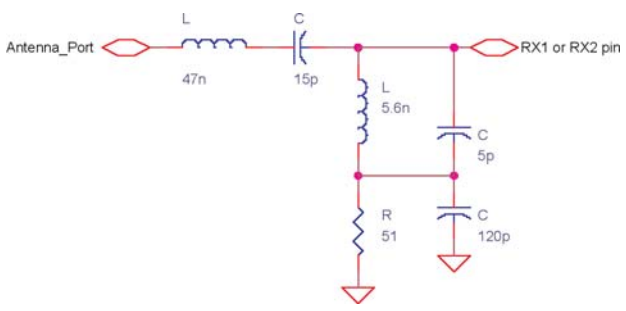

Figure 5 - 433.92MHz Typical Match to 50 Ohms

RX1, RX2, RF Input Impedance

There are two identical RF input circuits (AMIS-52000 pins RX1 and RX2). The LNA for these inputs requires a DC voltage path to ground. The following circuit diagram shows a suggested circuit for 433.92MHz.

Table 15: RFIN Characteristics

Specification	Settings	Conditions	Min	Typ	Max	Units
Input Resistance	RX trim 0x00	Trim set minimum		2K		Ω
Input Capacitance	RX trim 0x00	Trim set minimum		3		pF
Input Resistance	RX trim 0xff	Trim set maximum		2K		Ω
Input Capacitance	RX trim 0xff	Trim set maximum		6		pF
Input Sensitivity				-103		dBm
Input Noise Figure			3	3	6	dB
Freq Range			260	433	700	MHz
RF Input		Max RF signal input			-10	dBm
IP3				+8		dBm
IP2				+66		dBm

RFOUT, RF Output Impedance

The RF transmitter output pin is RFOUT. This is an open drain output. It requires a DC signal path to RFPWR, which is the output of the internal power supply to the transmitter. The transmitter output requires a tuned resonant circuit externally to form the desired waveform. This resonant circuit should be resonant at the desired output frequency. The transmitter output also requires filtering to reduce the harmonics to acceptable levels. The following circuit is a suggestion for matching the output to 50Ω at 433.92MHz. The circuit includes a tuned parallel LC tank at the 433.92MHz (including internal capacitance) and an LC notch filter at the third harmonic.

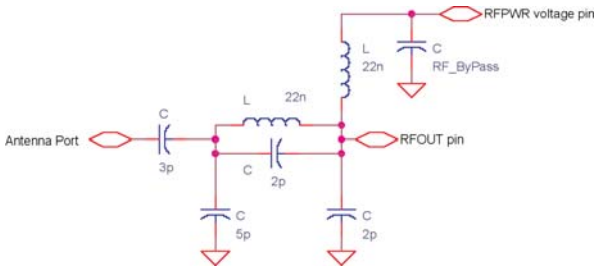

Figure 6 – 433.92MHz Typical Match to 50Ω

Table 16: RFOUT Characteristics

Specification	Settings	Conditions	Min	Typ	Max	Units
Output Resistance	TX PC 0x00			22		Ω
Output Capacitance	TX PC 0x00			3		pF
Output Resistance	TX PC 0xff			TBD		Ω
Output Capacitance	TX PC 0xff			TBD		pF
Harmonics	TX PC 0xff	With typical match circuit		-35		dBc
Freq Range	Transmit		260	433.92	700	MHz
Freq Range	Transmit	Fast start crystal circuit	350	433.92	480	MHz
Modulation				ASK/OOK		
On/Off Ratio				60		dB
Output Power	TX PC 0x00	With typical match circuit		-24		dBm
Output Power	TX PC 0xff	With typical match circuit		6		dBm

VCO1, VCO2, VCO Tuning

The AMIS-52000 has an internal Voltage Controlled Oscillator (VCO). A parallel LC circuit (tuned to twice the desired RF frequency) is connected between the VCO1 and VCO2 pins to set the frequency of the VCO.

There is a secondary requirement in the selection of the components for this function. When the component values meet the above resonant requirements, the loop filter voltage should be about in the mid range of the supply voltage (Vloopfilter = (1/2) the VCC supply). Different combinations of the L and C should be tried until this secondary requirement is also met.

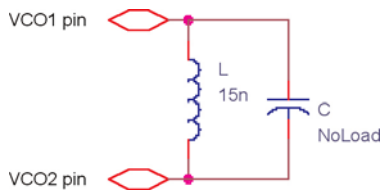

Figure 6 – Frequency Tuning Components for 433.92MHz

This circuit is sensitive to the PCB board layout. The components should be located as close as possible to the AMIS-52000 part.

The parallel LC circuit tunes the internal VCO frequency. The frequency is determined by the following:

Frequency = (2) * (Rxfreq) MHz

ctot = CAP + 2.25 pF

INDUCTOR = 1/((Ctot) * ((2πF)^2)))

More detailed information on this function is found in the AMIS application note, "AMIS-52000 Extending the AMIS-52000 Frequency Range Beyond the 433MHz Target."

LPFFILT

The AMIS-52000 uses a Phase Locked Loop to set the frequency stability of the oscillators. This circuit requires an external LOOP FILTER connected to pin LPF. The following second order loop filter is suggested. The components for this filter should be located as close to the AMIS-52000 part as possible in the PCB layout. More detailed information on the design of this filter is found in the AMIS application note, "AMIS-52000 Extending the AMIS-52000 Frequency Range Beyond the 433MHz Target."

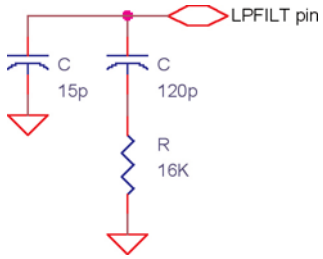

Figure 7 – Typical Loop Filter Design

Table 17: PLL Design Parameters

Items	Description	Min	Typ	Max	Units
Ref Freq.	433.93MHz external reference frequency		13.56		MHz
ζ	Damping factor		0.866		
Fn	Natural frequency		115		kHz
Icp	Charge pump current		50		µA
Kvco	VCO sensitivity		80		MHz/V

CREF, Current Bias Resistor

To insure proper operation of the AMIS-52000, this can only be a precision resistor with a value of 33.2KΩ. Use a 1% or better resistor tolerance.

I²CDATA, I²CCLK, Control Interface 2-wire Bus

The AMIS-52000 implements an I²C serial 8 bit bi-directional interface with the pins I²CDATA and I²CCLK. The I²C bus handshaking and protocol is implemented for a SLAVE device. The interface can connect directly to a host or controller I²C interface. There are internal pullup resistors on both the I²CDATA and I²CCLK lines of the AMIS-52000. The interface can handle data rates as defined in the I²C specification up to 400Kbps.

Pin	Function	Resistor	Units
I2CDATA	Internal pullup	15	KΩ
I2CCLK	Internal pullup	15	KΩ

Device	Address	Hex	Function
AMIS-52000	0110100X		Device address
AMIS-52000	01101000	68	Device write
AMIS-52000	01101001	69	Read device

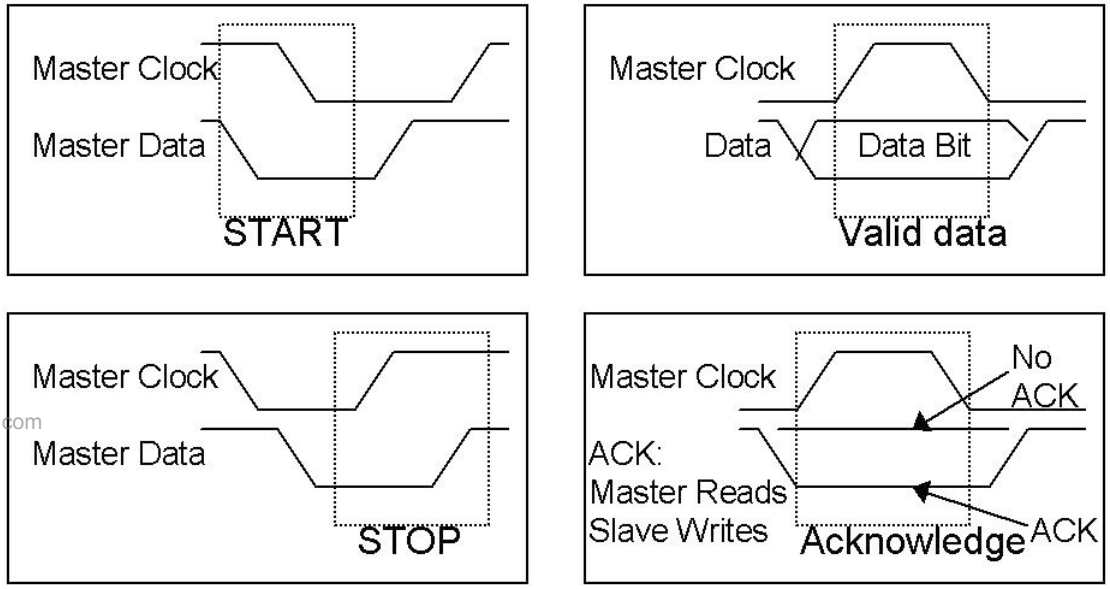

Figure 8 – I²C Waveforms Showing Message START and STOP Conditions

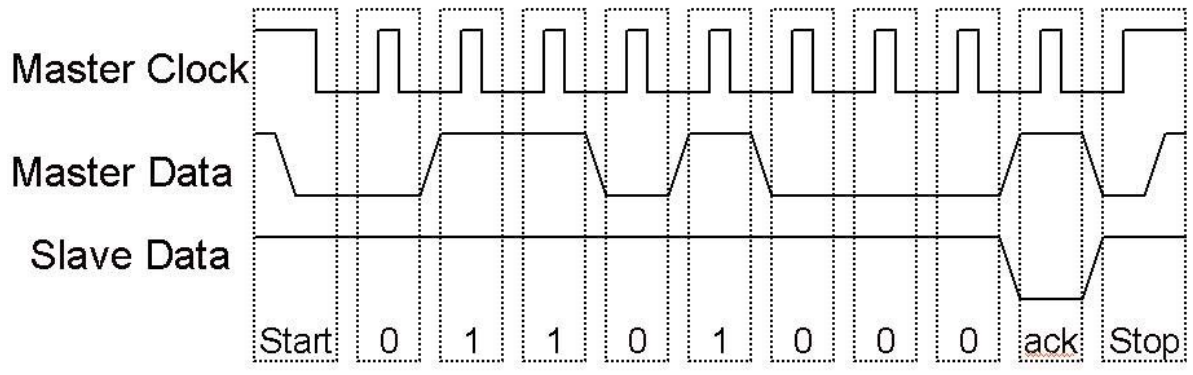

Figure 9 – I²C Waveforms Showing 8 BITs of Message and Acknowledge

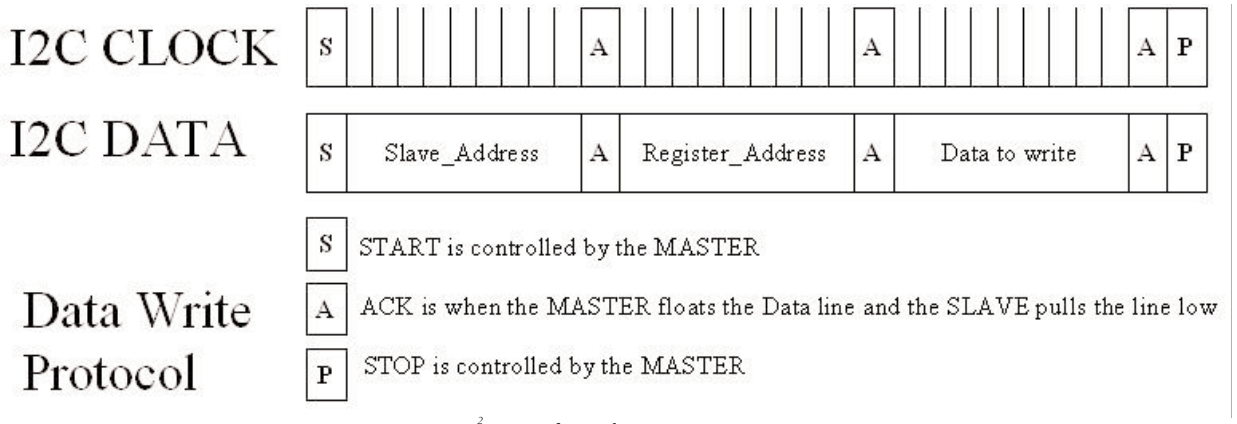

Figure 10 – I²C Waveforms Showing Write Message Format

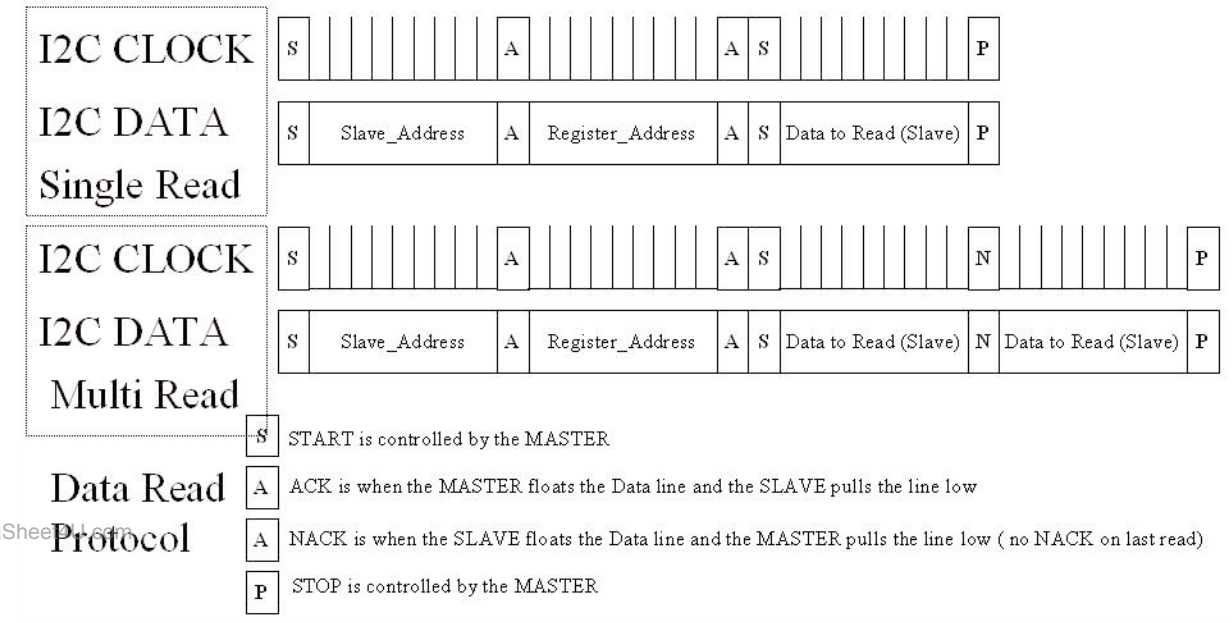

Figure 11 – I²C Waveforms Showing Read Message Format

The protocol of the I²C bus is as follows:
Clock is always from the MASTER
Device Address is different for a WRITE (0x68) than for a READ (0x69)
The SLAVE or MASTER when not outputting data leaves the data line high
The SLAVE acknowledges each BYTE written to it
The MASTER has the option of acknowledging the last READ BYTE of data
Each message begins with a START and ends with a STOP
Each message has DEVICE ADDRESS, REGISTER ADDRESS, and then DATA
MASTER can write incrementing registers by just adding DATA BYTES to message
When writing multi Data BYTES, add data to end of single DEVICE, REGISTER ADDRESS

X1, X2, Crystal Oscillator

The AMIS-52000 requires a parallel resonant crystal. The frequency of this crystal can be in the frequency range of 12.5MHz to 14.5MHz. The AMIS-52000 will form an RF frequency for transmit and receive from this crystal frequency. The transmit frequency is 32 times the crystal frequency. The receive frequency is the same, but the AMIS-52000 will pull the frequency to form an LO (local oscillator) frequency about 50kHz different than the signal frequency.

A typical value for the 2 parallel load capacitors is 15pF. This may be less than the suggested values for a crystal due to the internal trim capacitance of the AMIS-52000.

The AMIS-52000 contains a QUICK START function. For the frequencies that this circuit can operate (350 to 480MHz), the circuit can be used to stabilize the crystal frequency much faster than the normal crystal oscillator circuit. This function is explained in detail in AMIS application note, "AMIS-52000 Quick Start Crystal Oscillator Circuit Operation and Setup."

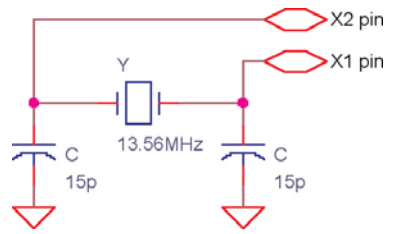

Figure 12 – Typical Crystal Oscillator Circuit

Power-On-Reset/Brownout Detection

The POR/Brownout Detection circuit ensures that the AMIS-52000 will be in a reset state when VDD drops below certain threshold voltage, and remains in this state until VDD rises above another threshold voltage. The POR circuit characteristics are illustrated in Figure 13.

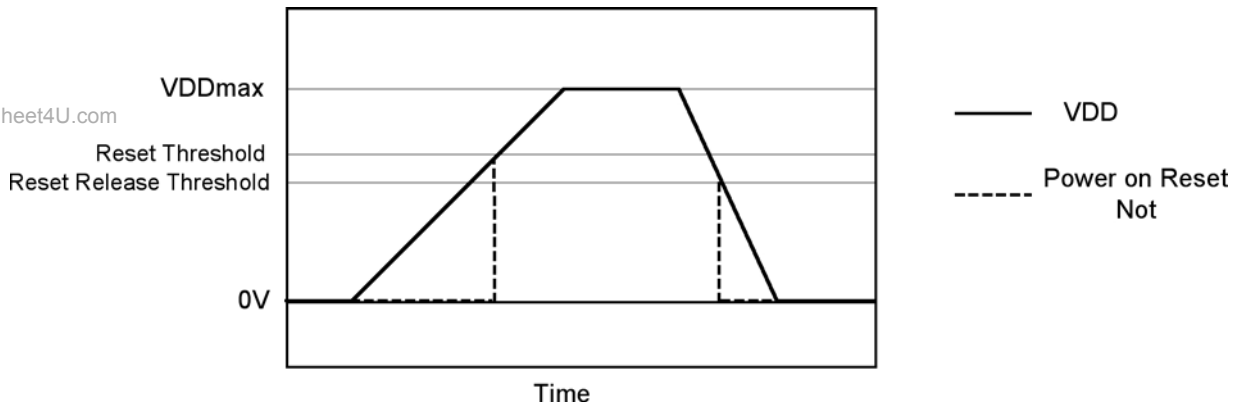

Figure 13 – Power On Reset Characteristics

Sniff Signal Acquisition

The AMIS-52000 is designed with a very low power mode. This mode shuts down the RF sections and CLKOUT circuitry. This mode has the RC oscillator and wake up divider circuits still running.

To take full advantage of the low power state, the AMIS-52000 has a Sniff Mode. In this mode, the AMIS-52000 will periodically wake the receiver to look for incoming RF energy. When the AMIS-52000 detects RF energy, it will start the receive mode, while setting the I^2CDATA and I^2CCLK lines to indicate to the host or controller that a wake up was generated by received signal. The minimum power use by the AMIS-52000 can be achieved by using the Sniff Mode to detect an incoming signal, while using the QUICK START function to start the crystal oscillator in a minimum time.

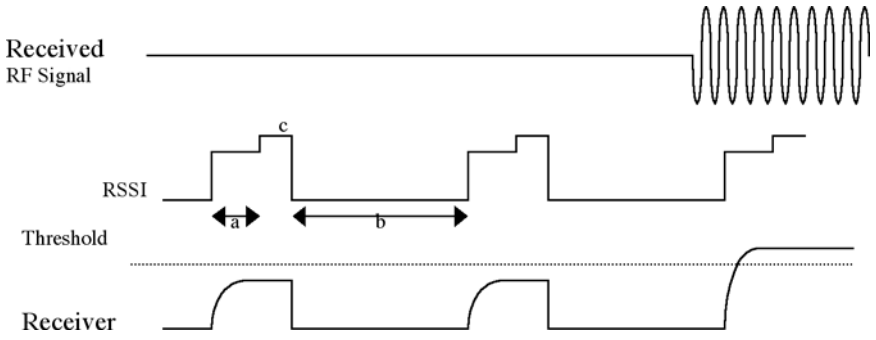

Figure 14 - Sniff (Data Acquisition) Timing
where: a: Delay (0x0B) before checking RSSI
b: Time between Sniff functions (0x0A)
c: Receiver on and sampling input signal

Alternative Wake-Up

The AMIS-52000 will wake from a low power mode upon the reception of RF energy. There is a second method for the AMIS-52000 to wake from its very low power mode. This low power mode is when the RF circuits and the CLKOUT circuits are shut off and the RC oscillator and wakeup divider chain are running. The AMIS-52000 can be programmed to wake up from time to time for housekeeping tasks. When the housekeeping timer occurs, the AMIS-52000 will set the I^2CDATA and I^2CCLK lines to indicate to the host or controller that a housekeeping cycle is requested.