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1.0 Introduction

The AMIS-52100 is a low-cost, ultra-low power single chip transceiver. It combines the proven amplitude shift key/on-off key (ASK/OOK) modulation technology of the AMIS-52000 with data clock recovery. The AMIS-52100 is targeted at narrow band applications in the 402 to 405MHz range.

Features such as dual independent receive channels, quick start crystal oscillator start up, Sniff Mode™ signal acquisition, and data clock recovery make the AMIS-52100 ideally suited for a wide range of customer applications. Applications that the AMIS-52100 can be used for are point-to-point wireless data links, low cost wireless monitors, very low power remote wireless sensors, and many other uses.

2.0 Key Features

- Data clock recovery
- Auto slicing of data
- Very low-power single-chip transceiver
- Minimal external components
- Low-power RC oscillator
- Quick Start for the crystal oscillator
- Extreme low-power RF Sniff Mode™, wakes on RSSI
- Internal trim functions reduce external component requirements
- I^2C control interface
- Serial TX/RX data port
- Clock generation for an external microprocessor
- Wake up on RSSI
- Antenna diversity dual receiver
- Internal VCO/PLL tuning varactor
- Application wakeup interrupt to external controller

3.0 Technical Features

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- Operating Frequency:
  - Quick Start range 350 to 448MHz
  - Non-Quick Start range 300 to 768MHz
  - Targeted range 402 to 405MHz
- TX Output Power: +12dBm
- RX Sensitivity:
  - Sniff Mode: -93dBm minimum
  - Receive: -117dBm minimum @ 1Kbps with CDR
- Data Rate:
  - 1 to 8Kbps with Manchester Coding
  - 1 to 16Kbps with NRZ data
- Power Requirements:
  - Receive: 7.5mA (continuous)
  - Transmit: 25mA full power; 50 percent duty cycle
  - Sniff Mode: 75uA (one percent duty cycle)
  - Standby: 500nA (RC oscillator running)
- Operating Voltage: 2.3 to 3.6V
- Modulation: ASK/OOK
- Xtal Start Time: 15us (Quick Start)
- Sniff Mode Polling: 0.5ms to 16s (0.5ms or 64ms steps)

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- PLL Lock Time: <50us
- Selectable Data Filter: up to 20kHz
- Internal Trim Function:
    - TX power (-3 to +12dBm)
    - Antenna impedance match (two independent channels)
    - Xtal for frequency and Quick Start
    - RC oscillator frequency
    - Sniff Mode for data threshold
    - Data slice
- Clock and Data Recovery (reduced Data jitter)
- I^2C Interface: Control bus
- Serial Interface: Data input/output
- Low Frequency IF
- Internal IF Filtering
- Package: 20-lead, 209mm SSOP

4.0 Functional Block Diagram

The AMIS-52100 is a dual channel receiver and a transmitter in a single small outline package. The receiver provides two independent receive channels with the signals combined in the data detection circuit. Summing the signals allows the two channels to be used for antenna diversity without complex protocols to select the strongest channel. The AMIS-52100 can be programmed to be a single channel or a dual channel receiver. There are internal trim functions for the RF receiver frequency, tuning each input port, setting the internal filters to match the data rate, and to set the threshold level for acquiring an incoming signal. The receiver converts the received RF signal to a low frequency IF. An RSSI circuit determines the strength of the received signal. A level detector samples the RSSI signal level and compares that level to the slice threshold to recover data. The slice threshold can either be set to a fixed level or the AMIS-52100 can determine the threshold level from the incoming data.

The transmitter is a high efficiency PA that is simply turned on or off by the serial data. The output power level is adjustable. The frequency of the RF output can be tuned with an internal crystal trim function that allows the AMIS-52100 to abide component and manufacturing tolerances. There are a number of unique circuit features. The AMIS-52100 can be placed in a very low power state with the crystal oscillator off and a low power RC oscillator maintaining operations. There is an application wakeup mode where the AMIS-52100 “sleeps” until either the application wakeup timer wakes the device or an external controller wakes the device. The receiver can be used in a low power Sniff Mode where the AMIS-52100 is programmed to wake at times to “sniff” for received RF signals and then return to “sleep” if a signal is not detected. The AMIS-52100 contains a Quick Start circuit that allows the crystal oscillator to return to full operation in an extremely short time which allows the AMIS-52100 to consume much less power than comparable products. The AMIS-52100 uses a programmable PLL to synchronize a data clock to the received data. This circuit can remove much of the jitter on the data signal.

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These functions will be described in more detail later in this document.

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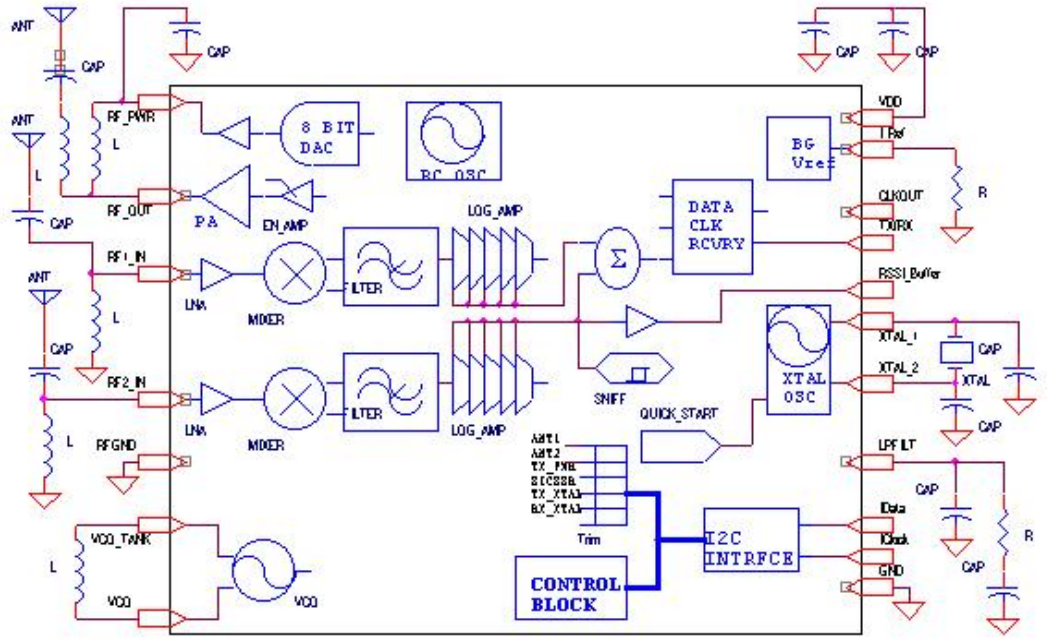

Figure 1: AMIS-52100 Block Diagram

5.0 Operating and Maximum Specifications

Table 1: Operating Conditions

Sym	Parameter	Min.	Typ.	Max.	Units
VDD	Positive Supply	2.3	3	3.6	V
VSS	Ground		0.0	0.1	V
Temp	Temperature Range	0	+25	+50	°C

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Table 2: Absolute Maximum Ratings

Sym	Parameter	Min.	Max.	Units
VDD	Positive Supply		+4	V
RFin	Max RF Input RX1/RX2		+10	dBm
VSS	Ground	0.0	0.1	V
Vin	Logical I/P Voltage	-0.3	VDD+0.3	V
Tstrg	Storage Temperature	-40	+120	°C

Table 3: Absolute Maximum Ratings

Idd (Supply Current)	Typ.	Max.	Units	Conditions
Transmitting	20	25	mA	50% duty cycle
Receiving	7.5	10	mA	
Sniff Mode	75		uA	1% sniff cycle
Off		500	nA	RC OSC off

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Table 4: Electrical Characteristics Digital Inputs

Parameter	Min.	Typ.	Max.	Units
Vih	0.7*VDD			V
Vil			0.3*VDD	V
Iih			+1.0	uA
Iil	-1.0			uA
I^2C Internal Pull-up		15	20	KΩ

Table 5: Electrical Characteristics Digital Outputs

Parameter	Min.	Typ.	Max.	Units
Voh	0.8*VDD			V
Vol			0.4	V
Ioh			-1.0	mA
Iol	+1.0			mA
I^2C Internal Pull-up		15	20	KΩ

Table 6: Electrical Characteristics Analog TX

Parameter	Min.	Typ.	Max.	Units	Comments
Frequency Range	402	403.5	405	MHz	Targeted
	300		768	MHz	Non Quick Start
	350		448	MHz	Using Quick Start
Modulation	1		8	Kbps	Manchester coded data
	1		16	Kbps	NRZ data
Max Output Power	11	12	13	dBm	
On/Off Ratio		70		dB	Transmit
VCO Gain		75		MHz/V	Kvco
PLL Phase Noise		-95		dBc/Hz	10kHz
		-97		dBc/Hz	100kHz
Harmonics		-35		dBc	With typical matching components
Crystal Freq Spurs		-50		dBc	50kHz PLL loop bandwidth
Time TX to RX			1	mS	

Table 7: Electrical Characteristics Analog RX

Parameter	Min.	Typ.	Max.	Units	Comments
Frequency Range	402	403.5	405	MHz	Targeted
	300		768	MHz	Non Quick Start
	350		448	MHz	Using Quick Start
Modulation	1		8	Kbps	Manchester coded data
	1		16	Kbps	NRZ data
RF Input	-117		-10	dBm	
Noise Figure		4.5			
RF Detect Time	100			uS	In Sniff Mode
Time RX to TX			1	mS	

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6.0 Pin Definitions

This section describes the pins of the AMIS-52000 package.

Table 8: Pin List

Pin#	Name	Type	Comments
1	RX1 RF	RF	Receive RF input 1
2	RX2 RF	RF	Receive RF input 2
3	VCO2	Ana	Voltage controlled oscillator 2
4	VCO1	Ana	Voltage controlled oscillator 1
5	LPFILT	Ana	Loop filter
6	RSSI/ Bandgap Out	Ana	Analog RSSI output or bandgap output
7	NC		No electrical connection
8	CREF	Ana	Current bias precision resistor
9	GND	Ana	Analog/digital ground
10	CLKOUT	Dig	RC, XTAL, or data clock output
11	X1	Ana	Xtal input
12	X2	Ana	Xtal output
13	IIC Data	Dig	IIC interface data I/O
14	NC		No electrical connection
15	IIC Clock	Dig	IIC interface clock
16	TX/RX DATA	Dig	Data transmit, data receive or recovered data
17	VDD	Ana	Positive power supply
18	RFPWR	Ana	Regulated voltage Output for RF transmitter circuitry
19	RFOUT RF	RF	Transmit RF output
20	RFGND	Ana	RF ground

7.0 Package Outline

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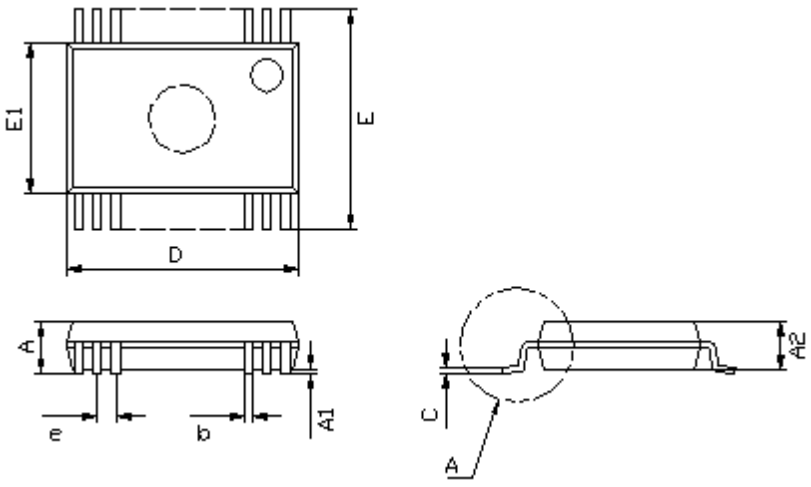

Figure 2: Package Outline

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Table 9: Package Dimensions: 209mil SSOP

	Inches		Millimeters	
Dm	Min.	Max.	Min.	Max.
A	0.068	0.078	1.73	2.00
A1	0.002	.20	0.05	
A2	0.065	0.073	1.65`	1.85
b	0.009	0.015	0.22	0.38
D	0.271	0.295	6.90	7.5
E	0.291	0.323	7.40	0.820
E1	0.197	0.221	5.00	0.560
e	0.026 BSC		0.65 BSC	

8.0 Pin Descriptions

8.1 RX1, RX2, RF Inputs

RX1 and RX2 are RF antenna inputs to the AMIS-52100. The internal circuit designs are identical between these inputs. The AMIS-52100 receiver inputs, RX1 and RX2, require external components to match the low noise amplifier (LNA) to external devices such as antennas. The external components must provide a DC voltage path to the RF ground. Figure 3 suggests an external circuit for the receiver inputs at 403MHz. Each circuit's input impedance can be trimmed internally to compensate for device manufacture and external component tolerances. The circuits employ an LNA, internal filters, a low frequency, intermediate frequency (IF), and an received signal strength indication (RSSI) circuit to recover the ASK/OOK modulated data. The signals in the two input channels are "summed" before the data recovery circuit.

The functions of the receive circuits are controlled by writing to the registers shown in Table 10.

Table 10: Receiver Control Register Description

RX1 or RX2 Receiver Register Control				
Register (HEX)	Name	Bits	States	Comments
0x00	ANT1 Trim	All		Inverse relationship register value to internal capacitance
0x01	ANT2 Trim	All		Inverse relationship register value to internal capacitance
0x0c	ANT1 Enable	0	0	Antenna port is off
			1	Antenna port is on
	ANT2 Enable	1	0	Antenna port is off
			1	Antenna port is on

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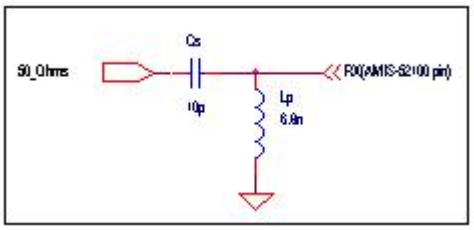

Figure 3: Typical Input Impedance Match to 50Ω (402MHz)

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8.2 VCO1, VCO2, Voltage Controlled Oscillator Tune

The VCO1 and VCO2 pins connect a parallel combination of a capacitor and an inductor to the AMIS-52100 internal voltage controlled oscillator (VCO). The external LC (parallel inductor and capacitor) circuit sets the frequency of the internal VCO. The VCO frequency must be set to be twice the desired TX or RX frequency of the AMIS-52100. The range of the VCO frequency is 600MHz to 1536MHz.

The voltage on these pins can be used to indicate proper operation of the AMIS-52100 PLL/VCO circuits, refer to the AMIS application note; “First Time Users Guide to working with the Transceiver IC” for more information.

Table 11: VCO Control Registers

VCO/PLL Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x06	Charge Pump	0,1	00	20uA
			01	25uA
			10	50uA*
			11	100uA
	VCO Current	2,3,4	000	180uA
			001	220uA
			010	260uA
			011	300uA
			100	340uA*
			101	380uA
			110	420uA
			111	460uA
	PLL Divider	7	0	Divider is 64
			1	Divider is 128

*Denotes the normal value

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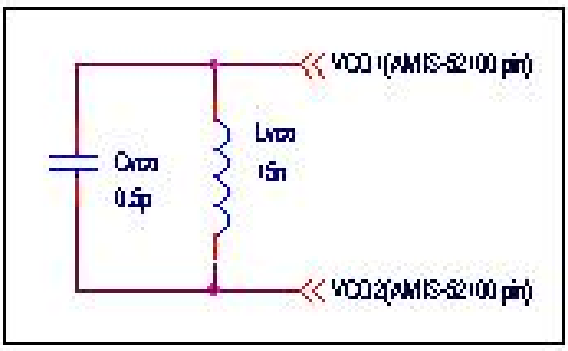

Figure 4: Typical Components for VCO Tuning at 402MHz

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8.3 LPFILT, Loop Filter

The LPFILT pin connects the AMIS-52100 internal phase lock loop (PLL) frequency synthesizer to an external loop filter. An external loop filter allows the design engineer to optimize the operation of the AMIS-52100 to meet the requirements of their product application. For more information see the AMIS application note: “Extending to Frequencies outside the 403MHz Target”.

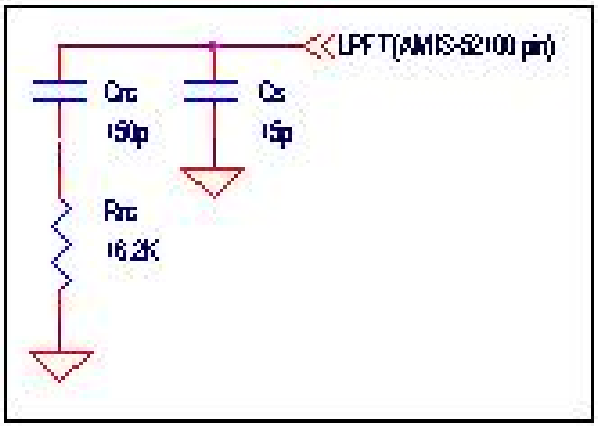

Figure 5: Typical Loop Filter

8.4 RSSI/BG, Analog Output

The RSSI/BG pin is used to output the signal from the RSSI circuits, the output of the voltage from the bandgap voltage reference or a bypass capacitor node. The RSSI output is a true analog representation of the received signal level. The pin can also be programmed to output the voltage of the bandgap voltage reference. When using the AMIS-52100 in the clock and data recovery mode, a capacitor needs to be connected from the RSSI/BG pin to ground. A typical value for this capacitor is 2.2nF. Additional information on the CDR function can be found later in this document. Table 12 presents the registers that control the function of the RSSI/BG pin.

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Table 12: RSSVBG Pin Control Registers

RSSI Pin Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0e	Bandgap on RSSI	3	0	Normal operation
			1	BG output on RSSI*
0x1e	RSSI Ext Amp	4	0	Tri-stated
			1	RSSI signal

*Note that device needs to be in RX, TX or crystal on moded for bandgap voltage to be present on pin.

8.5 CREF, Current Reference Bias

A resistor must be connected to the AMIS-52100 CREF pin to provide a current bias to the internal bandgap voltage reference circuit. It is critical that this resistor be a 33.2KΩ with one percent or better tolerance for proper operation of the bandgap voltage reference.

R(Bias) = 33.2KΩ (1%)

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8.6 GND, Ground

The GND pin is the ground connection for the digital and analog circuits in the AMIS-52100.

8.7 CLKOUT, Internal Clock Output

The CLKOUT pin is an output for the RC oscillator, crystal oscillator signal or the recovered data clock. The crystal oscillator signal output can be divided by 2, 3 or 4. The pin can also be programmed to output the signal from the recovered data clock function. For more information about the clock and data recovery (CDR) function of the AMIS-52100, refer to the section of this document on clock and data recovery.

The CLKOUT pin function control registers are shown in Table 13.

Table 13: Oscillator Output Control Registers

CLKOUT Pin Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0c	CLKOUT enable	7	0	CLKOUT is enabled
			1	CLKOUT is disabled
0x0d	CLKOUT select	4,5	00	Automatic control
			01	RC OSC
			10	Xtal
			11	Off
0x0e	XTAL divide	0,1	00	Divide by 4
			01	Divide by 3
			10	Divide by 2
			11	Divide by 1

8.8 X1, X2, External Crystal Reference

X1 and X2 pins connect a parallel resonance oscillator crystal to the AMIS-52100 internal oscillator circuit. The external crystal should meet the requirements as listed in Table 14, however, the two load capacitors should be sized slightly smaller than the recommended value for the crystal, because the AMIS-52100 adds capacitance in the internal trim circuit. For additional information, see the AMIS Application Note; “Quick Start Crystal Oscillator Circuit Operation and Setup”. The crystal parameters are shown in Table 14.

Table 14: External Crystal Parameters

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Parameter	Min.	Typ.	Max.	Units	Conditions
Crystal Frequency	12.56		12.65	MHz	Targeted
	10.9		14.0		Non Quick Start
	9.375		24.0		Using Quick Start
Crystal ESR			70	Ω	
Crystal Tolerance		10		ppm	
Load Capacitance	Load capacitors should be smaller than recommended for the crystal to allow for frequency tune				

8.9 I^2CDATA, I^2CCLK, I^2C Control Interface Bus

The AMIS-52100 implements an I^2C serial 8 bit bi-directional interface with the pins I^2CDATA and I^2CCLK. The AMIS-52100 implements the protocol for a slave device. The clock for the interface is generated by the external master device. The interface will support the normal (0 – 100 Kbits/second) or the fast (0 – 400Kbits/second) data modes. The interface conforms to the Phillips specification for the I^2C bus standard. The pins have internal pull up resistors. See Table 15 and Table 16 for some parameters of this interface.

Table 17 shows the register that controls the I^2C address increment function.

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Table 15: Internal I²C Pull-up Resistors

Pin	Function	Typ.	Units
I²CDATA	Internal Pull-up R	15	KΩ
I² CCLK	Internal Pull-up R	15	KΩ

Table 16: I²C Bus Device Addressing

Device	Address (Bin)	HEX	Function
AMIS-52100	01101000	68	Device write
AMIS-52100	01101001	69	Device read

Table 17: I²C Control Register

I²C Control Register				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0c	I²C address increment	2	0	Increment after write
			1	Do not increment

The I²CDATA and I²CCLK lines are also used to signal an external controller about internal AMIS-52100 activities such as wakeup. The receiver can be woken by energy detection during a Sniff operation. The AMIS-52100 can set the application wakeup timer to wake it from time to time to alert an external controller to perform tasks as defined by the application. The I²CDATA and I²CCLK lines are used to inform the external controller as to what event woke the AMIS-52100. These functions, Sniff Mode and application wakeup, are discussed later in this document.

8.10 TX/RX, Data Input/Output

The transmit/receive (TX/RX) pin function can be programmed to be an input for RF transmissions, an output for RF reception, the RC oscillator signal output, or the recovered data output from the CDR circuits.

In transmit mode, this pin is the digital data input to the AMIS-52100 RF transmit circuit. The data turns the transmit output power amplifier (PA) on or off. The AMIS-52100 does not perform any protocol conversion on the data bit stream, it is simply a serial bit stream. The state of the TX/RX pin either turns the output amplifier on, outputting RF signal. Or turns the output amplifier off, no RF signal output. The TX/RX input can be inverted which causes the state control of the RF output amplifier to be inverted also.

In receive mode, this pin is the digital data output from the AMIS-52100 receivers. The received data is recovered as a high/low (digital ones and zeros) serial bit stream, the AMIS-52100 does not modify the received data protocol. The receiver is just a pass through function. The data output state due to the presence of energy in the receiver can be programmed to be either a high level or a low level at the TX/RX pin. An external controller is needed to decode the information in the recovered data bit stream.

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When programmed to be an oscillator output, the TX/RX pin outputs the signal from the RC oscillator. This signal can be used to monitor the frequency of the RC oscillator to trim the frequency to the desired value.

The TX/RX pin can be programmed to output the recovered data obtained from the clock and data recovery circuits. The AMIS-52100 must be programmed into the CDR mode for this. More information on CDR is found in a later section on CDR.

The functions of the TX/RX port are controlled by writing to the registers shown in Table 18 of the AMIS-52100.

Table 18: TX/RX Pin Definition Control Registers

Register (HEX)	Name	Bits	States	Comments
0x0e	RC OSC on TX/RX	2	0	RX/TX normal
			1	RC OSC output
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

8.11 VDD, Supply Voltage

The VDD pin is the power supply pin for the AMIS-52100. The voltage on this pin is typically 3.0V. Please refer to the section "Operating and Maximum Specifications" of this document for the VDD operating conditions.

8.12 RFPWR, DC Voltage Output

The AMIS-52100 generates a regulated DC voltage that is output on the RFPWR pin. This voltage should be fed through a DC connection to the RFOUT pin to power the output stage of the RF PA. The AMIS-52100 adjusts the voltage level through the value of the register shown in
Table 19.

Table 19: TX Voltage control Register

RFPWR Voltage Control Register				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x02	RFPWR trim	All		0xff is highest power

8.13 RFOUT, RF Output Signal

The AMIS-52100 uses a high efficiency non-linear output driver to produce the high power RF signal. This final driver must be connected through a DC connection to the RFPWR pin of the AMIS-52100. External components are required to match the output to a 50Ωload or to an external antenna. Figure 6 shows a typical matching circuit for the RFOUT pin.

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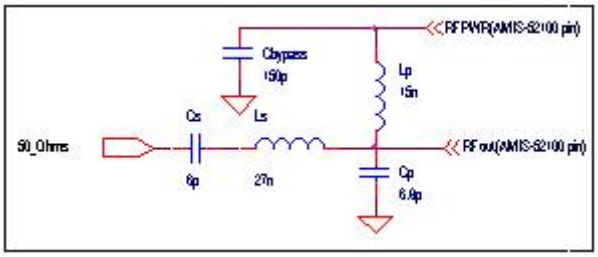

Figure 6: Typical RFOUT Output Impedance Match to 50Ω (402MHz)

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9.0 Circuit Functional Description

The functions of the AMIS-52100 are presented in this section. These functions are:

- Receiver
- Transmitter
- Sniff
- Quick Start
- Data Detection
- Clock and Data Recovery
- Application Wakeup
- I^2C Protocol
- Registers
- Alternative Wakeup
- Power on-Reset/Brownout

9.1 Receiver

RF signals often suffer from reflections along the path of propagation. These reflected signals arrive at the receiver antenna with different phases or time delays. The different phases of the reflected signals causes the signal strength at the receiver to vary. This variation can be large enough to cause the receiver to miss information. The AMIS-52100 sums the signals from the dual receiver channels inside the data detection circuits. This reduces the effect of the multipath reflections. The receivers in the AMIS-52100 require that the frequency be trimmed, the receiver oscillator frequency be tuned, the data rate filters be selected, and a signal threshold set as shown in Table 20.

Table 21 lists some characteristic parameters for the receivers. Figure 7 shows a typical received data waveform.

Table 20: Receiver Control Registers

RX1 or RX2 Receiver Register Control				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x00	ANT1 trim	All		Inverse relationship register value to internal capacitance
0x01	ANT2 trim	All		Inverse relationship register value to internal capacitance
0x05	RX XTAL tune	All		
0x0a	Data threshold	All		Reference level for detecting data logic state
0x0c	ANT1 enable	0	0	Antenna port is off
			1	Antenna port is on
	ANT2 enable	1	0	Antenna port is off
			1	Antenna port is on
	RX enable	3	0	Receiver is off
			1	Receiver is on
0x0f	Data filter	4,5,6	000	1.1kHz
			001	2.3kHz
			010	5.2kHz
			011	10.4kHz
			100	1.18kHz
			101	2.57kHz
			110	7.0kHz
			111	20.45kHz
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

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Table 21: RF Input Electrical Characteristics

Specification	Settings	Conditions	Typ.	Max.	Units	Comments
Input Resistance			2		KΩ	
Input Capacitance	Trim 0x00	Min. tune	3		pFarads	
	Trim 0xff	Max. tune	6		pFarads	
Sensitivity		1 Kbps	-117		dBm	w/CDR
Frequency			403.5		MHz	Target frequency
Max Input				-10	dBm	
IP3			+8		dBm	
IP2			+66		dBm	

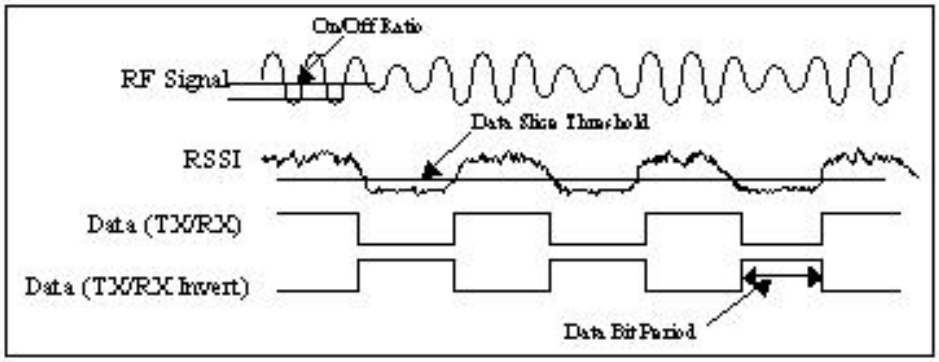

Figure 7: Received Waveform

9.2 Transmitter

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The RF transmitter is a non-linear open drain device. It requires a DC signal path to RFPWR, which is the output of the internal power supply to the transmitter. The transmitter is switched on and off with the serial transmit data stream. The output requires a tuned resonant circuit externally to form the desired waveform. This resonant circuit should be resonant at the desired output frequency. The transmitter output also requires filtering to reduce the harmonics to acceptable levels. The circuit includes a parallel LC tank (Lp and Cp) tuned to 402MHz (including internal capacitance) and a series LC (Ls and Cs) to produce a 403MHz output while reducing the harmonics. The transmitter requires that the output power level be programmed, the transmit frequency be tuned and the data rate be selected as shown in the registers of Table 23 lists some characteristic parameters for the transmitter.

Figure 8 shows what the transmit output waveform could look like.

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Table 22: Transmitter Control Registers

TX/RX Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x02	TX power	All		
0x04	TX XTAL trim	All		
0x0c	TX enable	4	0	Transmitter is off
			1	Transmitter is on
0x0f	Data filter	4,5,6	000	1.1kHz
			001	2.3kHz
			010	5.2kHz
			011	10.4kHz
			100	1.18kHz
			101	2.57kHz
			110	7.0kHz
			111	20.45kHz
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

Table 23: Output Impedance Characteristics

Specification	Settings	Conditions	Min.	Typ.	Max.	Units
Output Impedance		Resistance		22		Ω
		Capacitance		3		pFarads
Output Power	RFPWR 0x00			-26		dBm
	RFPWR 0xff		11	12	13	dBm
Harmonics		Ext circuit		-35		dBm
Frequency Range		Target	402		405	MHz
		Quick Start	350		448	MHz
		Full range	300		768	MHz
Modulation				ASK/OOK		
On/Off Ratio	TX output			70		dBm

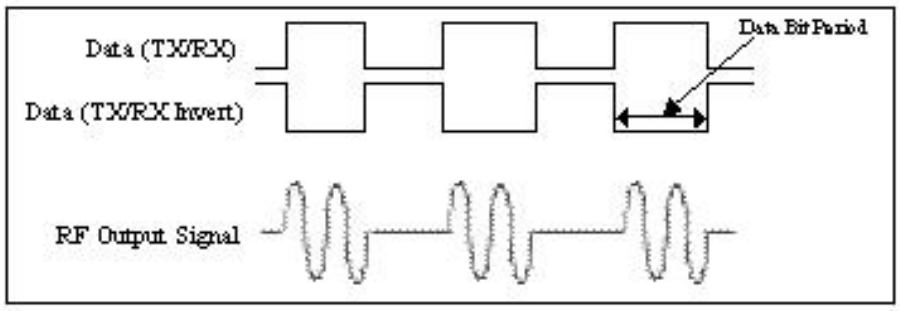

Figure 8: Transmit Waveforms

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9.3 Sniff Mode

Very low power applications will want to program the AMIS-52100 to use the Sniff Mode. This mode turns the receiver and crystal oscillator off for a programmed time. At the end of this time the receiver wakes and “sniffs” for incoming RF energy. If energy is detected, the receiver wakes the full receive function and starts data recovery from the RF carrier. If energy is not detected, the receiver returns to the low power or “sleep” state. The operation of the Sniff Mode is very programmable. The time that the receiver is asleep can be programmed from microsecond to seconds. Once the receiver wakes to detect RF energy, there is a programmable delay before the receiver checks for energy. There is another delay that accounts for circuit delays. Finally, there is a programmable delay after energy is detected and before the receiver samples the recovered energy to determine the logical state of the recovered data. Table 24 lists these registers. Refer to the AMIS application note “Sniff Mode” for more information.

Figure 9 and Figure 10 show waveforms that show the timing of the Sniff Mode.

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Table 24: Sniff Function Control Registers

Control Registers Associated with the Sniff Function				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0b	SNIFF Threshold	All		Reference level for detected RF
0x0c	WAKE on RSSI	5	0	Do not wake on RSSI
			1	Wake on RSSI > threshold
0x0d	SNIFF TIMER RES	3	0	Resolution is set to 0.5mS per step
			1	Resolution is set to 64mS per step
0x13	DATA FILTER	All		Delay from RX wakeup to data sampled
0x16	IRQ DELAY	All		Time I^2C and TX/RX are active to indicate a wakeup
0x18	RSSI DELAY	All		Delay from wakeup to RSSI being checked
0x19	SNIFF TIMER	All		Time that receiver is off in Sniff Mode
0x1a	OFFSET DWELL	All		Time allowing receiver to power up (typically >40uS)
0x1b	DATA FILTER PRE-DIVIDER	All		Delay from data detection to pre-clock output

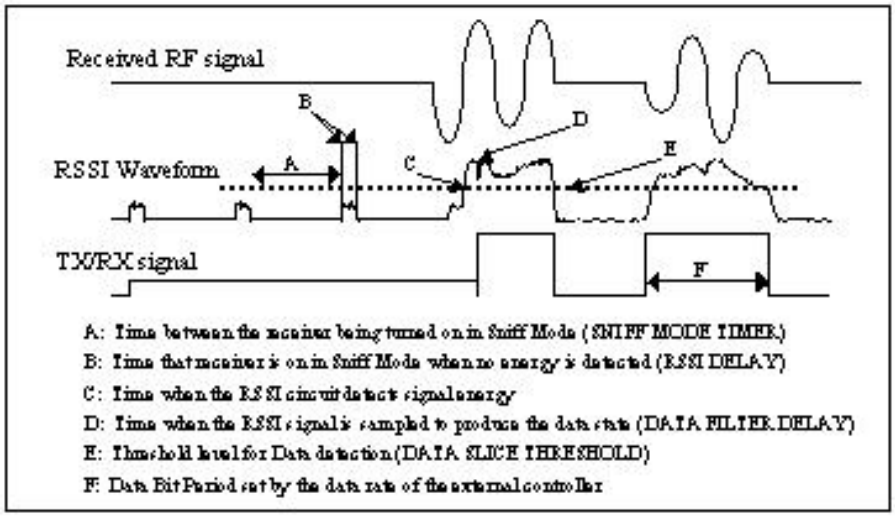

Figure 9: Receiver Data Acquisition in Sniff Mode

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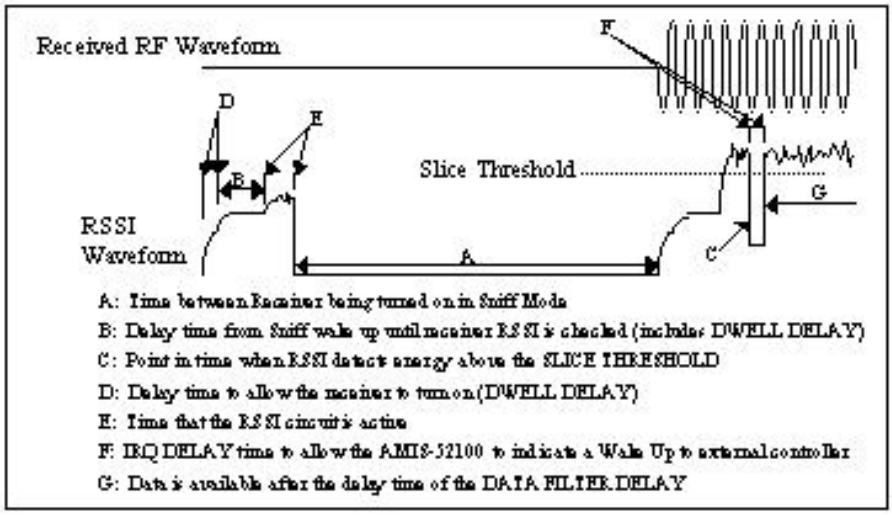

Figure 10: Sniff Timing at RF Energy Detection

9.4 Quick Start

There are two oscillators in the AMIS-52100, a low power 10kHz RC oscillator and a crystal oscillator.

The RC oscillator is used to keep the AMIS-52100 running in a very low power mode. This oscillator is used to form the clocks for the Sniff Mode timers and the application wakeup timers. Figure 11 shows a block diagram of the clocks in the AMIS-52100. The crystal oscillator is the reference that is used to create the RF frequencies for transmit and receive. It is the reference for timing functions in the AMIS-52100. An RC oscillator is used to produce a kicker signal when the crystal oscillator is needed to Quick Start.

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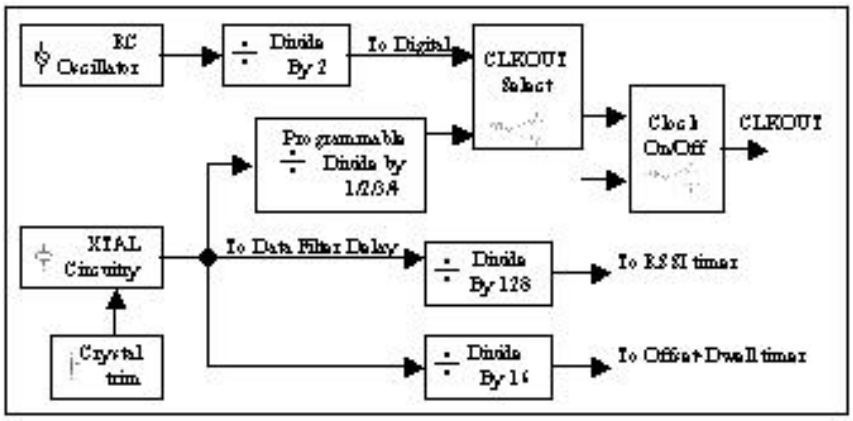

Figure 11: Internal Clocks

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A kicker circuit stimulates the crystal oscillator circuit with oscillations close to the correct frequency. This reduces the time it takes for the frequency to be locked. The receiver is on frequency and ready to receive the incoming signal much faster with the use of this circuit. The Quick Start function is necessary when using the Sniff Mode. Table 25 lists the registers that function with Quick Start. Refer to the AMIS application note “Quick Start Crystal Oscillator Circuit Operation and Setup” for more information.

Table 25: Quick Start Control Registers

Quick Start Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x03	Kicker Trim	All		Trim the internal RC OSC to form a kick-start to the XTAL oscillator
0x0e	Kick Config1	4	0	Common mode clamp disabled (startup)
			1	Common mode clamp enabled (normal)
	Kick Config2	5	0	Normal operation
			1	Continuous kick on

9.5 Data Detection

The RSSI circuit creates an analog voltage waveform (18mV/dB) that follows the signal strength of the RF signal. A data slice circuit then samples that waveform to create the digitized data. The slice circuit in the AMIS-52100 can be programmed to operate in one of three modes; DAC mode, average mode or peak mode. The DAC mode compares a fixed slice threshold value to the level in the slice output. The digital data state is determined by the level of the slice output being above or below that fixed threshold. Refer to AMIS application note “Setting Up the Data Slicing Modes” for more information. Figure 12 shows a typical waveform for the DAC mode.

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Table 26Table 26 shows the control registers for the auto slice modes.

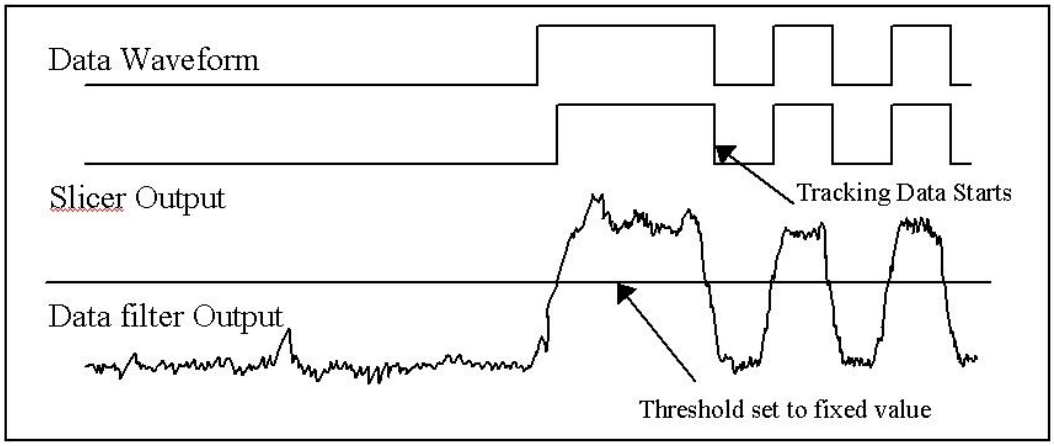

Figure 12: DAC Slice Mode Waveform

The average mode generates a threshold value automatically. This generated threshold is used to compare to the output of the slice circuit to re-create the digital data. The slice circuit uses an external capacitor to generate a charge time constant that is equal to charging to 95 percent of a bit level in two bit time periods. The data protocol should add a header to the data to allow the slice circuit to determine the average level. Refer to AMIS application note “Setting Up the Data Slicing Modes” for more information. Figure 13 shows a typical waveform for the average mode. Table 26 shows the control registers for the auto slice modes.

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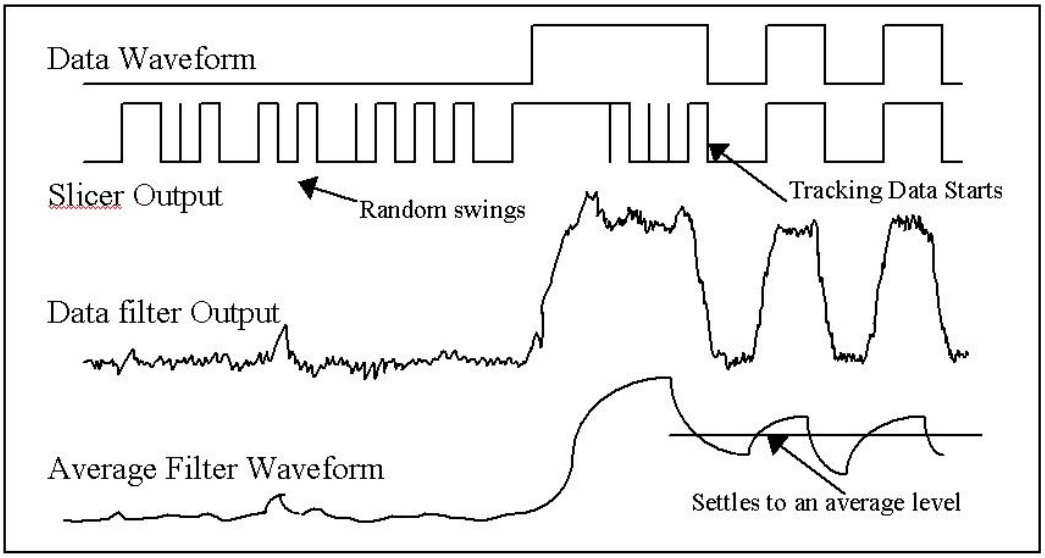

Figure 13: Average Slice Mode Waveform

The peak mode also generates a threshold value automatically. This generated threshold is used to compare to the output of the slice circuit to re-create the digital data. The slice circuit uses an external capacitor with an internal peak detector to form the peak value of the data waveform. A threshold value is set 6dB below this peak value. The capacitor value should be selected so that the peak detector does not discharge during periods of continuous zeros, while being small enough to allow the peak detector to reach the peak value quickly. Refer to AMIS application note "Setting Up the Data Slicing Modes" for more information. Figure 14 shows a typical waveform for the Peak mode.

Table 26 shows the control registers for the auto slice modes.

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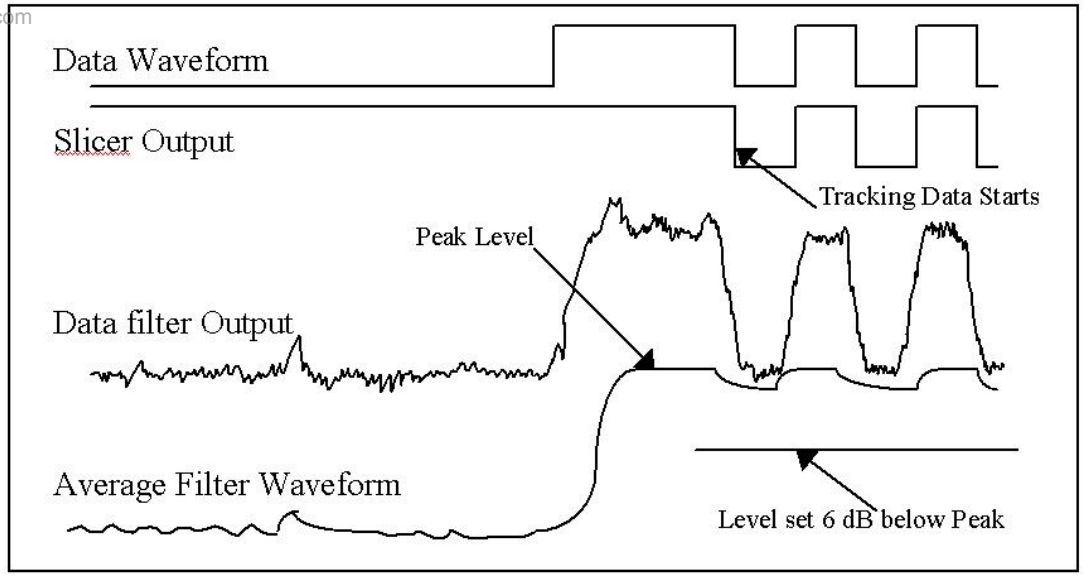

Figure 14: Peak Slice Mode Waveform

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Table 26: Auto Slice Control Registers

Auto Slice Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0a	DATA SLICE THRESHOLD	All		Set a fixed reference level for the slice output to be compared to in the DAC mode
0x0f	HYSTERESIS	0,1	00	0mV hysteresis used in the threshold circuit
			01	20mV hysteresis used in the threshold circuit
			10	50mV hysteresis used in the threshold circuit
			11	100mV hysteresis used in the threshold circuit
	AUTOSLICE	2,3	00	DAC mode used for data detection (DEFAULT)
			01	Average mode used for data detection
			10	Peak mode used for data detection
			11	DAC mode used for data detection

9.6 Data and Clock Recovery

Data recovered in a noisy environment or from a small RF signal usually is jittery. The AMIS-52100 can remove much of that data jitter by recovering a synchronous clock signal from the incoming data. The AMIS-52100 can be set to do auto slice data detection. The clock and data recovery circuits can be programmed to generate a data clock for synchronously clocking the data out of the AMIS-52100, removing much of the jitter in this process. The AMIS-52100 has an internal PLL that must be programmed to the frequency of the data by setting the values in the FWORD register and setting the coefficients of the filter. If these values are close to the data rate, the AMIS-52100 will recover the data clock from the incoming detected data. The CDR circuit can also be set or clamped with a tolerance to the frequency difference between the supposed data rate and the actual data rate to improve the performance of the CDR function. The CDR circuit can be set to reset after a programmed number of data time periods without data. This stop check function allows the CDR circuit to reacquire the clock when new data is received, maintaining better clock to data synchronization.

Table 27 presents the registers associated with the data and clock recovery function. Refer to the AMIS application note “Clock and Data Recovery Circuit Operation and Setup” for more information.

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Table 27: Data and Clock Recovery Control Registers

Data and Clock Recovery Associated Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x07	FWORD LSB	All		Sets the initial internal clock frequency for the clock and data recovery circuits
0x08	FWORD	All		
0x09	FWORD MSB	All		
0x0d	DATA MUX	6	0	TX/RX normal signals
			1	Recovered data on TX/RX
	CLKMUX	7	0	Normal CLKOUT signals
			1	Recovered CLOCK output on CLKOUT
0x10	K_0	0,1,2	000	Filter coefficient gain is 1
			001	Filter coefficient gain is 2
			010	Filter coefficient gain is 4
			011	Filter coefficient gain is 8
			100	Filter coefficient gain is 16
			101	Filter coefficient gain is 32
			110	Filter coefficient gain is 64
			111	Filter coefficient gain is 128
	K_1	4,5,6	000	Filter coefficient gain is 1
			001	Filter coefficient gain is 2
			010	Filter coefficient gain is 4
			011	Filter coefficient gain is 8
			100	Filter coefficient gain is 16
			101	Filter coefficient gain is 32
			110	Filter coefficient gain is 64
			111	Filter coefficient gain is 128
0x11	K_2	0,1,2	000	Filter coefficient gain is 0.125
			001	Filter coefficient gain is 0.250
			010	Filter coefficient gain is 0.500
			011	Filter coefficient gain is 1.000
			100	Filter coefficient gain is 2
			101	Filter coefficient gain is 4
			110	Filter coefficient gain is 8
			111	Filter coefficient gain is 16
	FsDIV	4,5,6	000	Sample frequency divider is 2
			001	Sample frequency divider is 4
			010	Sample frequency divider is 8
			011	Sample frequency divider is 16
			100	Sample frequency divider is 20
			101	Sample frequency divider is 32
			110	Sample frequency divider is 40
			111	Sample frequency divider is 48
0x12	STOP CHECK	0,1	00	StopCheck bits: disabled
			01	StopCheck bits: 2
			10	StopCheck bits: 4
			11	StopCheck bits: 8
	LOOPCLAMP	2,3	00	Loop clamp value is: +-BaudClk/8
			01	Loop clamp value is: +-BaudClk/16
			10	Loop clamp value is: +-BaudClk/32
			11	Loop clamp value is: +-BaudClk/64
	FREERUN	4	0	Phase alignment enabled
			1	Phase alignment disabled
	CRD RESET	5	0	CDR reset disabled
			1	CDR reset enabled
	AUTO/MANUAL RESET	6	0	POR reset (auto)
			1	CDR reset enabled (manual)
	SAMPLE WINDOW	7	00	Sampling starts with bit start edge
			00	Sampling centered around bit center

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The clock and data recovery function requires that the receiver be able to recover the data from the incoming RF signal. There is a method to test the clock and data recovery function without having to set the receiver up to receive data. This is a test mode that allows an input data stream (square wave at 1/2 the data rate) to be input on the RSSI pin and recovered clock will appear on the CLKOUT pin

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while recovered data will appear on the TX/RX pin. The AMIS-52100 must be set up for clock and data recovery (See the AMIS application note “Clock and Data Recovery Circuit Operation and Setup”). Then the following register in Table 28 defines the test select.

Table 28: Clock and Data Recovery Test Mode

Clock and Data Recovery Test Control Register			
Register (HEX)	**Binary Code**	**HEX Code**	**Comments**
0x1d	00001110	0x0e	Normal RSSI digital input
	00001111	0x0f	CDR start bit digital input to RSSI

9.7 Application Wakeup

Very low power applications can take advantage of the application wakeup function in the AMIS-52100. The AMIS-52100 is placed in a low power or “sleep” state until the programmable application wakeup timer goes off. This wakes the AMIS-52100 so that it can alert the external controller that the application may perform required operations. Since the AMIS-52100 can be awakened by either RF energy detection, in Sniff Mode, or by the application wakeup timer, an external controller can interrogate the I^2C bus pins to determine which function cause the AMIS-52100 to wake. Also, when the AMIS-52100 is in the power down or “sleep’ state, an external controller can wake it. Table 29 presents the registers associated with this application wakeup function.

Table 29: Application Wakeup Control Registers

Application Wakeup Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x14	AW TIMER DIV	All		Divides the RC oscillator to form a clock for the AW
0x15	AW TIMER	All		Number of AW clock periods before a AW wakeup
0x17	PRE/POST AW DELAY	All		Number of CLKOUT clock periods before the TX/RX pin goes low for a AW cycle

9.8 I^2C Interface

The I^2C is a two pin bi-directional serial interface communication bus. There is a data line and a clock line. Serial data on the data pin is clocked into or out of the AMIS-52100 by the clock pin. The AMIS-52100 is implemented as a slave device, which means that an external controller is the master. The master forms the clock signal for all transactions between the master (external controller) and the slave (AMIS-52100). The slave device acknowledges writes to it and the master acknowledges reads from the slave. The serial bit rate can be as high as 400Kbps and is set by the clock of the master. A communication link is started with a start sequence. Communication continues as long as the master and slave acknowledge each write or read. Communication is ended with a stop sequence. These are illustrated by Figure 15, Figure 16 and Figure 17.

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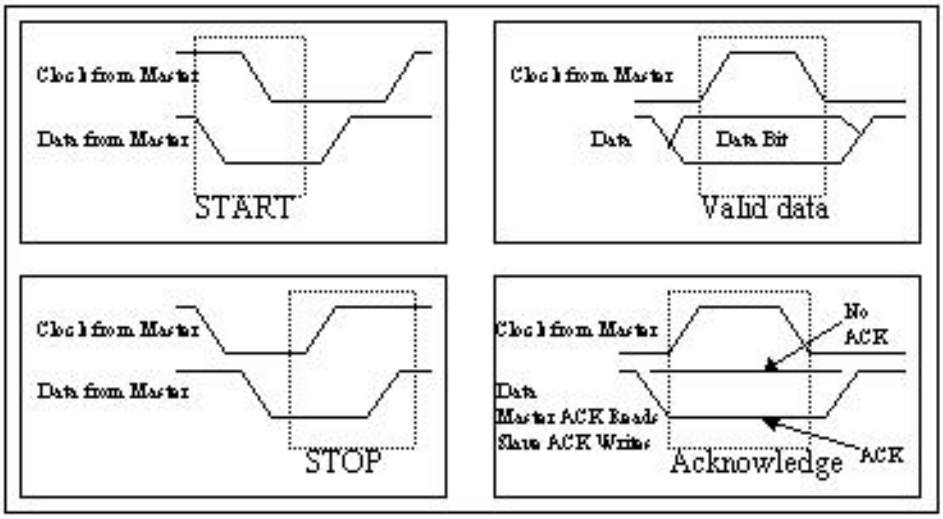

Figure 15: I^2C Valid Control Waveforms

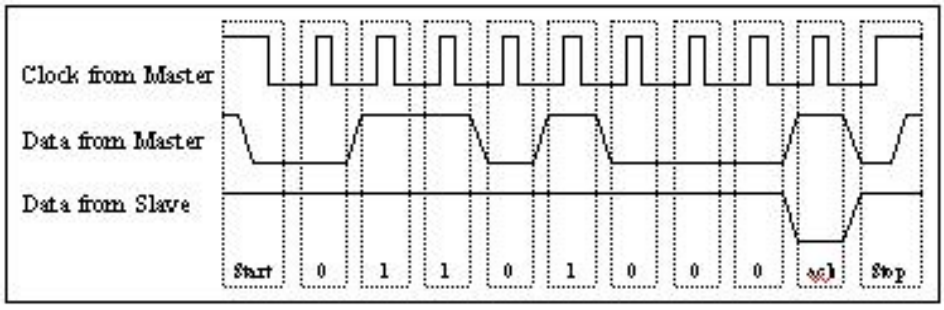

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Figure 16: I^2C Protocol in a Write 68 (Hex) or a Data Write Request

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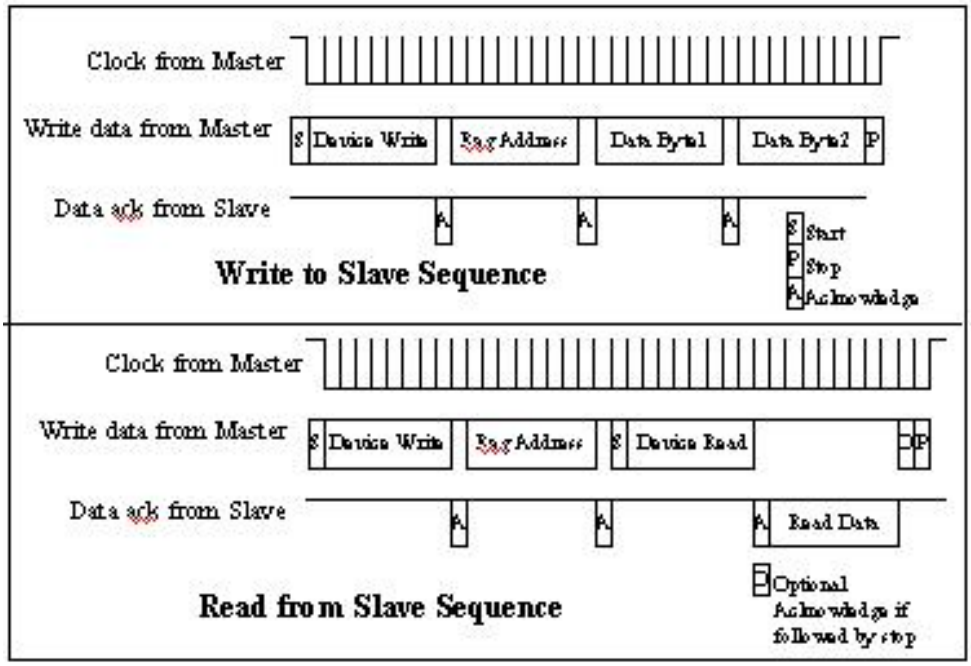

Figure 17: I²C Write and Read Protocol

9.9 Registers

The AMIS-52100 is comprised of 31 registers. These registers are presented in the AMIS application note: "AMIS-52100 Register Description for Transceiver IC".

9.10 Power-on-Reset/Brownout Detection

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The POR/brownout detection circuit ensures that the AMIS-52100 will be in a reset state when VDD drops below a certain threshold voltage, and remains in this state until VDD rises above another threshold voltage. The POR circuit characteristics are illustrated in Figure 18.

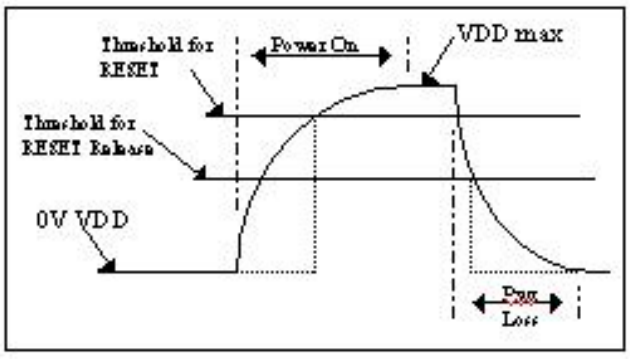

Figure 18: Power-on-Reset Characteristics

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9.11 Alternative Wake-Up

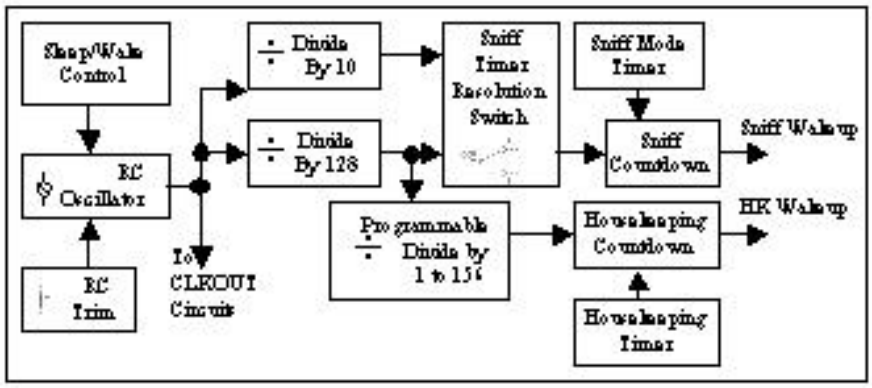

Figure 19: Wakeup Circuits

The AMIS-52100 will wake from a low power mode upon the reception of RF energy, an application wakeup time out or when signaled by an external controller. The low power mode is when the RF circuits are shut off, the crystal oscillator is shut off, the CLKOUT circuits are shut off and only the RC oscillator and wakeup divider chain are running. When the AMIS-52100 receiver detects energy and wakes up, the RX/TX pin is set low while the I^2CDATA and I^2CCLK pins are allowed to remain pulled high. When the application wakeup timer wakes the AMIS-52100 to inform the external controller that tasks need to be performed, the TX/RX and I^2CDATA pins are set low while the I^2CCLK pin is allowed to remain high. The TX/RX pin can be used to alert the external controller that a wake up occurred in the AMIS-52100. Then the external controller can interrogate the I^2C pins to determine what caused the wake up to occur. The external controller can also cause the AMIS-52100 to wake up by setting both the I^2CDATA and I^2CCLK lines low. These functions are shown in the following Table 30.

Table 30: Wakeup Truth Table

Wakeup Truth Table					
Wakeup Source	**TX/RX**	**I^2CDATA**	**I^2CCLK**	**CLKOUT**	**Comments**
SNIFF	0	1	1	XTAL out	Wake on RF energy detect
HK Cycle	0	0	1	RC oscillator	Wake due to HK timer timeout
External	1	0	0	Don't care	Wake due to external controller

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10.0 Ordering Information

Ordering Code	Device Number	Package Type	Industry Application	Shipping Configuration
19293-001-XTP (or XTD)	AMIS-52100-I/A	20-pin SSOP (209mil) (shrink small outline package)	Industrial, automotive, other	Tape&Reel (-XTP) Tube/Tray (-XTD)
19293-002-XTP (or XTD)	AMIS-52100-M	20-pin SSOP (209mil) (shrink small outline package)	Medical	Tape&Reel (-XTP) Tube/Tray (-XTD)
19293-003-DIE	AMIS-52100-I/A	Bare die	Industrial, automotive, other	Waffle-pack
19293-004-DIE	AMIS-52100-M	Bare die	Medical	Waffle-pack

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11.0 Company or Product Inquiries

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