

1.0 General Description

The AMIS-710227 (PI227MC-A4), AMIS-710228 (PI228MC-A4) and AMIS-710229 (PI229MC-A4) are a family of contact image sensor (CIS) modules. As a family group they are called AMIS-710227/228/229 modules. They are long-contact image sensor modules using MOS image sensor technology for high-speed performance and high sensitivity. They contain their own complete optical system including the light source; accordingly, they make a very compact imaging system. The four parallel video outputs give this family of CIS modules their high-speed performance. They all possess identical electrical circuit components, as well as the mechanical and optical components, except for their LED light sources. Accordingly, they differ in their specification because the different light sources limits the effective high-speed performance. The three modules are suitable for scanning A4 size (216mm) documents with 8 dots per millimeter (dpm) resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- Ultra-high-speed
- Four parallel analog video outputs clocked at 5.0MHz
- 90 μ sec/line scanning speed @ 5.0MHz clock rate with optional light sources, selected from the option of three above modules
- 8dpm resolution, 216mm scanning length
- Wide dynamic range
- LED light source (selectable among the three above modules)
- Standard A4 size \cong 14mm x 19mm x 232mm
- Low power
- Light weight

3.0 Functional Description

Each of the three modules in the family, AMIS-710227/228/229, consists of four major components. The first of them is the printed circuit board (PCB) on which the 27 imaging chips, AMIS-720220 (PI3020), are bonded. These sensor chips, produced by AMI Semiconductor, are monolithic devices with 64 photo-sensing elements. Each of 27 chips are complete self-contained scanning chips and have their control circuits integrated in the chips, so that they can be cascaded to provide 1728 photo-element modules. The AMIS-720220 chips are integrated with the photo sensors' associated multiplex switches, a digital shift register and chip selection switch. The chip's shift register sequentially clocks out the integrated image charges from each sensing element and passes them through the chip-select switch and out onto the video line. The chip-select switches are sequentially switched as each of the predecessor chips completes its scan. These 27 sensors, bonded on a PCB, are grouped into four sub-cascaded sections. Each contiguously cascaded chips section is connected on separate video lines, resulting in four video outputs VOUT1, VOUT2, VOUT3, and VOUT4. Before the signal, charges from the four video lines appear at their respective outputs where they are converted to signal voltages by four on-board buffer amplifiers, one for each of its corresponding video section. The first three sections VOUT1, VOUT2 and VOUT3 have seven sensor chips, while the VOUT4 has six sensor chips. Since each sensor chip has 64 pixels, there are a total of 1728 pixels. See Figure 1.

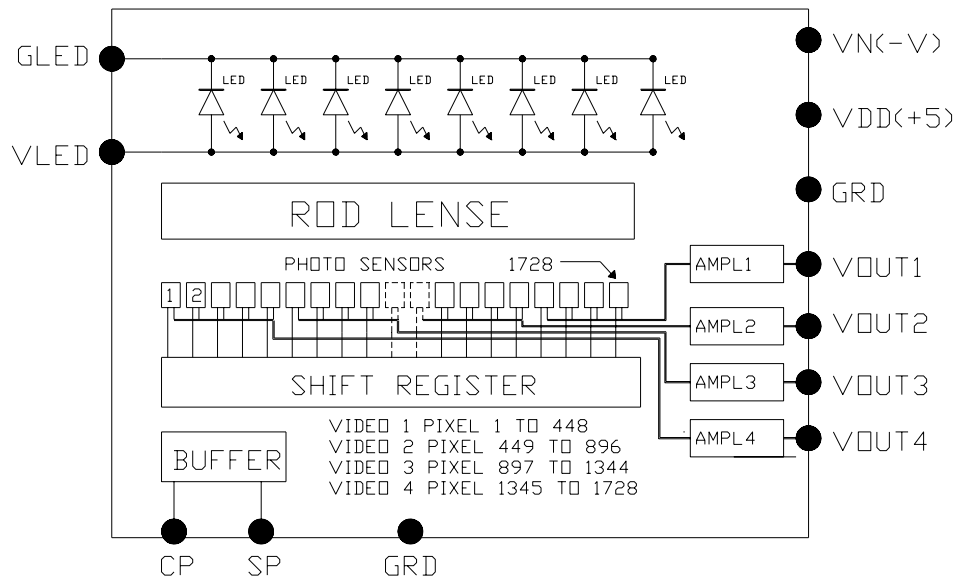
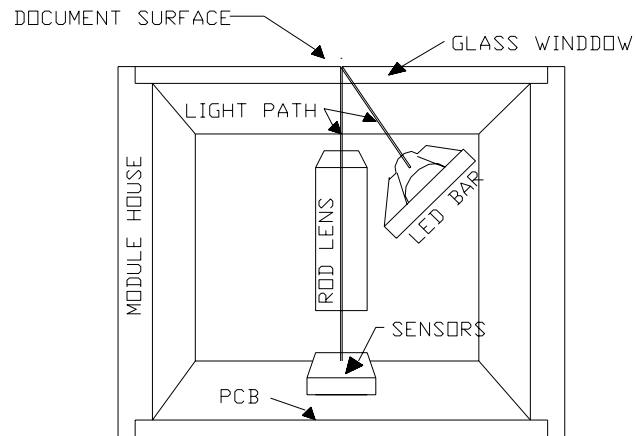


Figure 1: AMIS-710227/228/229 Module Block Diagram

(See Table 4-A for Pin Out Designation)

Mounted in the module housing along with the PCB is the second major component. It is a one-to-one graded indexed micro lens array that focuses the scanned documents' image onto the sensing line of the sensor chips. The third major component, mounted in the module, is the LED light source. See Figure 2. This pictorial cross section shows the LED bar light source and its illumination path as it reflects the image from the document and focuses through the ROD lens on to its image sensing line of the sensing chips. All components are housed in a small plastic housing and covered with the fourth major component, a glass window. This cover glass not only serves to protect all of the critical components within the housing from dust, but also serves a minor role in the optical system. Together with rest of the module's optical system, the module is adjusted to obtain the optimum depth-of-focus. See Section 10: MTF Graph and its Discussion.



INSIDE PICTORIAL
OF THE MODULE

Figure 2: AMIS--710227/228/229's Cross Section



4.0 I/O Designation

I/O to the module is a 12-pin connector located on one end of the module. See Figure 6. Table 4-A lists the pin numbers and their designations for the I/O connector. It is JAE IL-Z-12P-S125L3-E connector.

Table 4-A: Pin Configuration

Pin Number	Symbol	Names and Functions
1	VOUT1	Analog video output 1
2	VOUT2	Analog video output 2
3	GND	Ground; 0V
4	VOUT3	Analog video output 3
5	VOUT4	Analog video output 4
6	Vdd	Positive power supply
7	SP (START)	Shift register start pulse
8	GND	Ground; 0V
9	CP (CLOCK)	Sampling clock pulse
10	Vn	Negative power supply
11	GLED	Ground for the light source; 0V
12	VLED	Supply for the light source

5.0 Module vs LED Light Source

Table 5-A lists the LED light source associated with each module model

Table 5-A: Module vs. LED Light Source

Module	LED Light Source
AMIS-710227	660nm Red LED bar
AMIS-710228	High power Yellow-Green LED bar
AMIS-710229	Low power Yellow-Green LED bar

6.0 Absolute Maximum Rating

Table 6-A shows the absolute maximum ratings. The parameters are common to all three modules. Table 6-B shows the absolute maximum ratings that are different among the three modules.

Table 6-A: Electrical Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply	Vdd	7	V
	Idd	100	ma
	Vn	-15	V
	In	35	ma
Input clock pulse (high level)	Vih	Vdd – 0.5	V
Input clock pulse (low level)	Vil	-0.5	V

Note: These parameters are absolute maximums; do not operate under these conditions.

Table 6-B: LED Power Absolute Maximum Rating

Parameter	Symbols	Maximum Rating			Units
		AMIS-710227	AMIS-710228	AMIS-710229	
Power supply: LED light source	Module	AMIS-710227	AMIS-710228	AMIS-710229	
	VLED	6.0	6.0	6.0	V
	ILED	0.7	1.0	1.0	amp

Note: These parameters are absolute maximums; do not operate under these conditions.

7.0 Environmental Specifications

Table 7-A: Operating and Storage Environment

Parameter	Symbols	Maximum Rating	Units
Operating temperature ⁽¹⁾	Top	0 to 50	°C
Operating humidity ⁽¹⁾	Hop	10 to 90	%
Storage temperature ⁽¹⁾	Tstg	-20 to +75	°C
Storage humidity ⁽¹⁾	Hstg	10 to 90	%

Note:

1. These are standard specifications for the CIS modules.

8.0 Electro-Optical Characteristics (25°C)

Table 8-A is the electro-optical characteristics common all three modules. Table 8-B, Table 8-C and Table 8-D show the different characteristics for each of the three LED light sources.

Table 8-A: Common Electro-Optical Characteristics

Parameter	Symbol	Value	Units	Notes
Total number of photo detectors		1728	Elements	
Section 1, 2 & 3 number of photo detectors		448	Elements	
Section 4 number of detectors		384	Elements	
Pixel-to-pixel spacing		125	µm	

Table 8-B: AMIS-710227 Electro-Optical Characteristics

AMIS-710227 660 RED LED				
Parameter	Symbol	Value	Units	Note
Line scanning rate	Tint ⁽¹⁾	90	µsec	@ 5.0MHz clock frequency
Clock frequency ⁽²⁾	Fclk	5.0	MHz	
Bright output voltage ⁽³⁾	Video output	1.0	Volt	
Bright output non-uniformity ⁽⁴⁾	Up	<+/-30	%	
Dark non-uniformity ⁽⁵⁾	Ud	<40	mV	
Dark output voltage ⁽⁶⁾	Dark level (DL)	<200	mV	
Modulation transfer function ⁽⁷⁾	MTF	>40	%	

See notes below Table 8-D

Table 8-C: AMIS-710228 Electro-Optical Characteristics

AMIS-710228 High Power Yellow-Green LED				
Parameter	Symbol	Value	Units	Note
Line scanning rate	Tint ⁽¹⁾	90	µsec	@ 5.0MHz clock frequency
Clock frequency ⁽²⁾	Fclk	5.0	MHz	
Bright output voltage ⁽³⁾	Video output	0.5	Volt	
Bright output non-uniformity ⁽⁴⁾	Up	<+/-30	%	
Dark non-uniformity ⁽⁵⁾	Ud	<40	mV	
Dark output voltage ⁽⁶⁾	Dark level (DL)	<200	mV	
Modulation transfer function ⁽⁷⁾	MTF	>40	%	

See notes below Table 8-D

Table 8-D: AMIS-710229 Electro-Optical Characteristics

AMIS-710229 Low Power Yellow-Green LED

Parameter	Symbol	Symbol	Units	Notes
Line scanning rate	Tint ⁽¹⁾	150	μsec	@ 3.0MHz clock frequency
Clock frequency ⁽²⁾	Fclk	3.0	MHz	
Bright output voltage ⁽³⁾	Video output	0.5	Volt	
Bright output non-uniformity ⁽⁴⁾	Up	<+/-30	%	
Dark non-uniformity ⁽⁵⁾	Ud	<40	mV	
Dark output voltage ⁽⁶⁾	Dark level (DL)	<200	mV	
Modulation transfer function ⁽⁷⁾	MTF	>40	%	

Definition:

1. Tint is the line scanning rate or integration time. Tint is determined by the interval between two SP.
2. Fclk: main clock frequency, also equals the video sampling frequency
3. The video output level is controlled with a voltage adjustment as well as the Integration time and LED light power.
4. $Up = \{[Vp(max) - Vp(min)] / Vp(max)\} \times 100\%$
Where Vp(max) = maximum peak pixel and Vp(min) = minimum pixel
5. $Ud = Vdmax - Vdmin$
Vdmin is the minimum output voltage with LED off.
Vdmax is maximum output voltage with LED on.
6. See paragraph under Reset Level and Video Sampling Time.
7. See Section 10: MTF Graph and its Discussion. A graph of the typical MTF vs. DOF Graph is depicted with discussion.

9.0 Reset Level and Video Sampling Time

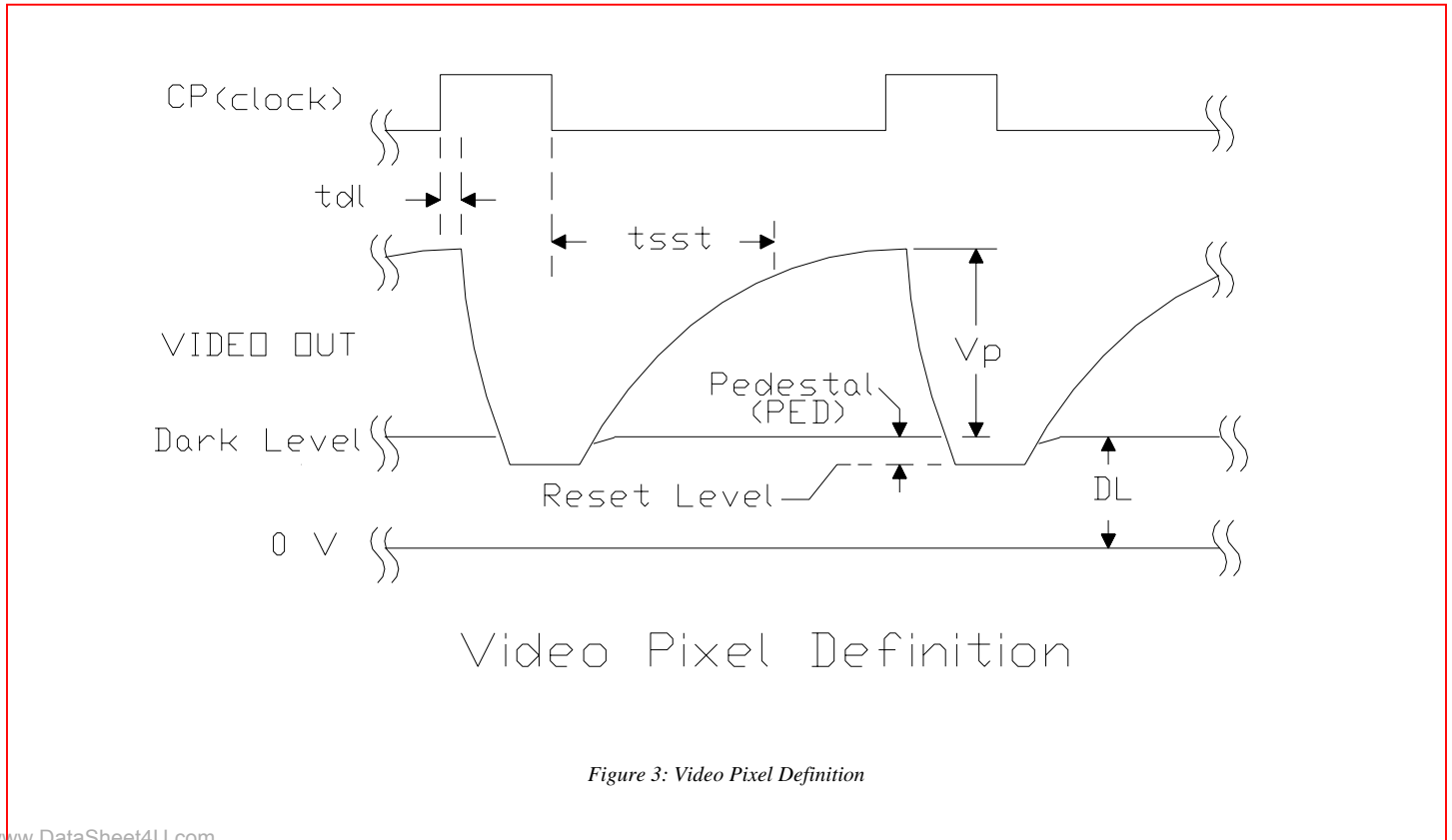


Figure 3 graphically shows the video signal waveform and defines the single video pixel structure. The signal output waveform is shown relative to the input clock waveform as well as the symbols and terminologies used to define the performance specifications. Figure 3 serves to explain the terminology used to characterize the dark signal levels and the recommended video pixel sampling times.

Note 6, under Table 8-D, specifies the dark level (DL). This is the level during the dark read-out, i.e., either the module sits on black target or the light source is turned off. It is measured from ground or 0V. The reset level is a reference level for the reset switch which is not necessarily on ground because after the reset the signal is passed through an amplifier. The difference between the dark level and the reset level is called the pedestal (PED). In most cases, the offset control of the amplifier is used to adjust the dark level to 0V or ground. Hence, the reset level will sit below ground.

The video pixels demonstrated in this graph emanate from an ideal CIS module with a phototransistor imaging structure. The video output at high speeds, such as 5.0MHz, does not instantly rise to its final value. Given enough time, it would asymptotically approach its steady state value. But, at high speeds it is impractical to wait for a final stable value. Accordingly, as Figure 3 indicates, the output signal continues to rise towards its steady state value. Consistent with the forgoing comments, in Note 7 under Table 8-D, instead of the conventional signal sampling time (tsst) is defined to substitute the conventional settling time definition. This definition is used because the output signal continues to rise asymptotically to the final stable value, but not within a practical time in high speed applications. This is true even when the video rises to its peak value (Vp) indicated on the MTF Graph, see Figure 4.

10.0 MTF Graph and its Discussion

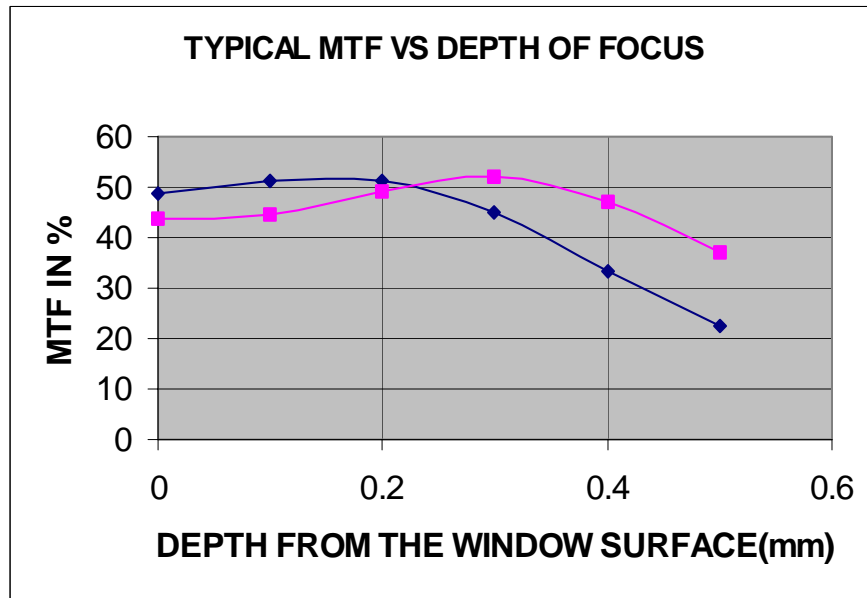


Figure 4: Typical MTF vs. Distance

This graph essentially shows the working depth-of-focus. Two curves indicate the spread among the modules. Note that MTF is greater than 40 percent out to a distance greater than 0.4mm from the glass surface. Since this module is a 200dpi module, a pixel density of 200 pixels per inch, the MTF was measured with a 100dpi or a 50 line-pair per inch optical bar pattern. The test was conducted with the pixel rate set to 2.5MHz.

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The effective algorithm used in the measurements is as described by the following equation:

$$MTF = \frac{[V_p(n) + V_p(n+1)]/2 - [V_p(n+2) + V_p(n+3)]/2}{[V_p(n) + V_p(n+1)]/2 + [V_p(n+2) + V_p(n+3)]/2}$$

Where n is 1, 2,1728th, $V_p(n)$ is the signal amplitude of the nth pixel.

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11.0 Operating Conditions (25°C)

Table 11-A: Recommended Operating Conditions (25°C):

Item	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd (positive)	4.5	5.0	5.5	V
	Vn (negative)	-10	-5	-4.0	V
	Idd (positive)	60	66	75	ma
	In (negative) ⁽¹⁾	20	20	20	ma
Input voltage at digital high	Vih	Vdd-1.0	Vdd-0.5	Vdd	V
Input voltage at digital low	Vil	0		0.6	V
Clock frequency	Fclk	0.2 ⁽²⁾		5.5 ⁽³⁾	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration		45.5	50		ns
Integration time	Tint	82	150		μs
Operating temperature ⁽⁴⁾	Top		25	50	C

Table 11-B: AMIS-710227 Operating Conditions (25°C)

AMIS-710227				
Parameter	Min.	Typ.	Max.	
VLED		5.0	5.5	V
ILED		480	550	ma

Table 11-C: AMIS-710228 Operating Conditions (25°C)

AMIS-710228				
	Min.	Typ.	Max.	
VLED		5.0	5.5	V
ILED		TBD	TBD	ma

Table 11-D: AMIS-710229 Operating Conditions (25°C)

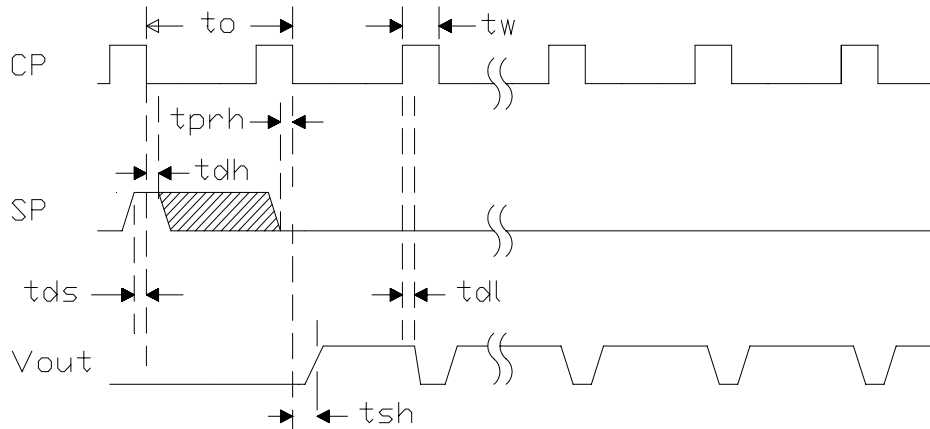
AMIS-710229				
	Min.	Typ.	Max.	
VLED		5.0	5.5	V
ILED		TBD	TBD	ma

Notes:

1. Current is essential constant current with supply voltage
2. Determined by the longest tolerable integration time, because of leakage current build up, the integration time is recommended to be no greater than 10ms
3. The maximum call out is for the modules' electrical speed. The light source still dictates the highest speed performance.
4. This specification is a standard used by the CIS makers for the Fax Industry.

12.0 Switching Characteristics (25°C)

The switching characteristics (25°C) for the I/O clocks are shown in the diagram of Figure 5. Each switch timing characteristic for each waveform is represented by its symbolic acronym. Each corresponding switching time is defined in the Table 12-A. Note: Only one video output is shown because all four videos have identical electrical characteristics. The only physical difference is in Section 4,



MODULE TIMING DIAGRAM

output, VOUT4. Section 4 has only 6 sensor chips, hence its active scan is shorter by 64 pixels.

Figure 5: Module Timing Diagram

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Table 12-A: Timing Symbol's Definition and Timing Values

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	t_o	0.20		4.0	μ s
Clock pulse width	t_w	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of SP ⁽¹⁾	t_{prh}	0			ns
Data setup time	t_{ds}	20			ns
Data hold time	t_{dh}	0			ns
Signal delay time	t_{dl}	20			ns
Signal settling time	t_{sh}	100			ns

Note:

- "Prohibit crossing of start pulse" is to indicate that the SP should not be active high between any two consecutive clock pulses, specifically, between two consecutive low-going clock pulses. See the timing diagram. All falling clock edges under an active high SP loads the internal shift register, therefore the SP must be active over only one falling clock edge. High SP over all rising clock edge is ignored by the shift register. One simple way to ensure that the SP will not be actively high during two consecutive falling clock edges is to generate the SP on a rising clock edge and terminate it on the following rising clock edge.

13.0 Mechanical Structure of the Module

The isometric sketch, Figure 6, of the housing shows the connector location, the approximate overall dimensions and the general geometric layout of the module. It is not intended for use as a design reference. The detailed drawing for any of the AMIS-710227/228/229 modules is available upon request.

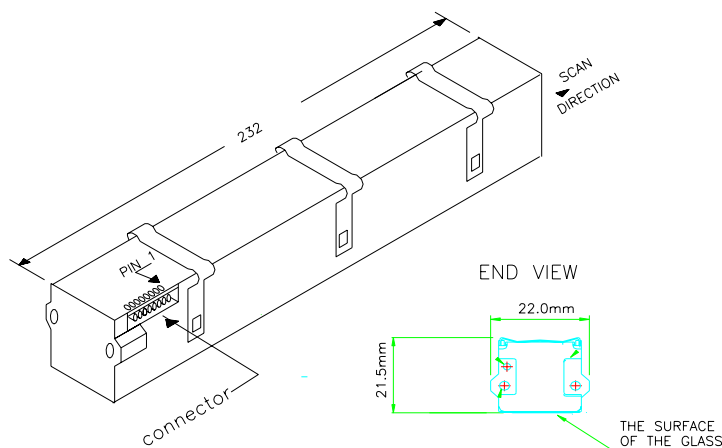


Figure 6: AMIS-710227/228/229 Module Mechanical Overview

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14.0 Company or Product Inquiries

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