AMIS-710324-A4: 300dpi CIS Module

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Data Sheet

1.0 General Description

The AMIS-710324-A4 (PI324MC-A4) is a contact image sensor (CIS) module. It is a dual-analog-output contact image sensor, using MOS image sensor technology for high-speed performance and high sensitivity. The AMIS-710324-A4 is suitable for scanning A4 size (216mm) documents with 11.8 dots per millimeter (dpm) resolution. Applications include fax machines, game systems, a variety of mark readers and other automation equipment requiring document scanners.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- 11.8dpm resolution, 216mm total scanning length (2592 pixels long)
- Two independent analog outputs (split into two sections of 1248 pixels and 1344 pixels)
- Up to 270μsec/line scanning speed with red light source
- Wide dynamic range
- Red LED light source
- Compact size ≅ 14mm x 19mm x 232mm
- Low power
- Light weight

3.0 Functional Description

The AMIS-710324-A4 imaging array consists of 27 sensors, AMIS-720321 (PI3021), produced by AMI Semiconductor. The sensor is a monolithic chip with an array of 96 photo sensing elements, of which 27 are cascaded to provide 2592 photo-detectors. Additionally, these chips give the users the readout flexibility in selecting their desired data format. These cascaded chips are segregated into two electrically independent sections of 13 chips and 14 chips, but they are still contiguously aligned in a single row, see Figure 1 (the module's block diagram). This configuration lends itself to a positional stream of video pixels, whether they are read in parallel or sequentially from the two output ports.

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Each chip contains a set of multiplex switches, and a digital shift register to control the chips sequential readout. Additionally, the chips contain a chip selection switch that is interrogated in a sequence as each predecessor chip completes its scanning process. Since this module has two output ports from two independently controlled sections of chips, the users are required to enter a set of control clocks and power into each section through the two provided connectors located on each end of the module.

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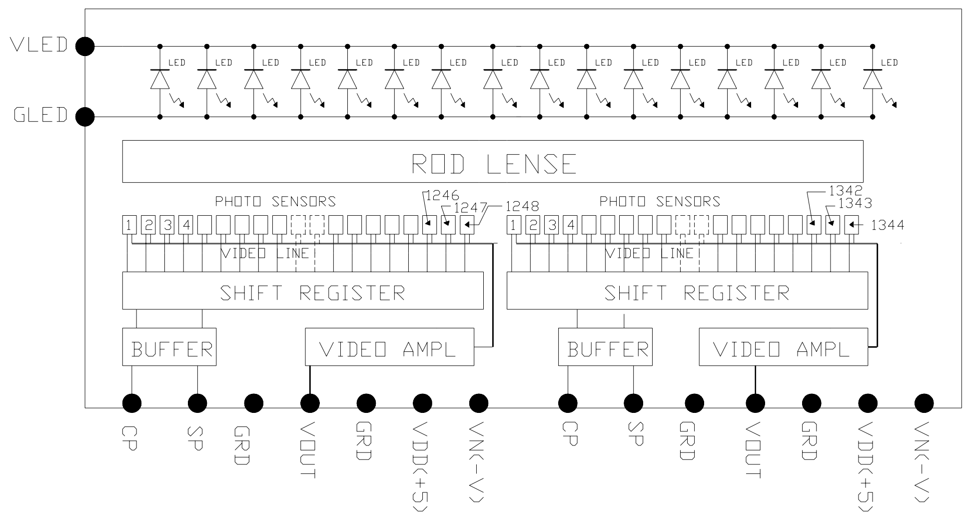

Figure 1: AMIS-710324-A4 Module Block Diagram (See Table 1 for Pin Out Designation)

Figure 2 depicts a cross sectional pictorial of the module. Mounted in the module is a one-to-one graded indexed micro lens array that focuses the scanned documents' image onto the chip's sensing line. The sensing line is located along the module's sensor axis, known as the read line. These photon images are transformed into proportional video charges and processed by two on-board amplifiers. The video signal from the amplifier transmits a sequential stream of video pixels to the video output pin of the AMIS-710324-A4 module. Also mounted in the housing is a LED light source. Figure 2 shows the LED bar and its illumination path. The path traces the ray from the LED and is reflected from the document and focused through the ROD lens and onto the sensors. All these components are housed in a small plastic housing with a cover glass. The cover glass serves as a window with the outside surface as the focal point for the image on the document. It also serves to protect the imaging array, the micro lens assembly and the LED light source from dust.

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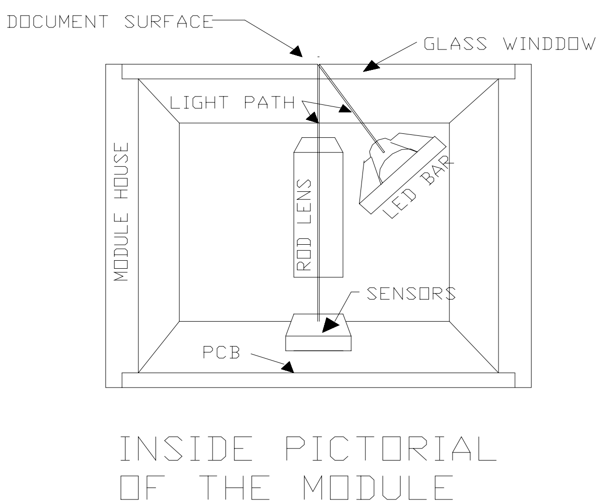

Figure 2: AMIS-710324-A4 Cross Section

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4.0 I/O Designation

There are two connectors located at the ends of the modules. The outline of the module in Figure 5 of the mechanical section illustrates these connector locations. With the module window facing down on a flat surface and with the viewer looking down on the backside of the module, the connectors are located on each end of the module with their pins pointing toward the viewer. The connectors for Section 1 have 12 pins and are located on the right-hand side. The part number is JAE IL-Z-12P-S125L3-E. Its pin numbers and designations are listed in Table 1.

Table 1: Pin Configuration for Section 1 Connector

Pin Number	Symbol	Names and Functions
1	Vout1	Analog video output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V)	Negative power supply
5	Gnd	Ground; 0V
6	SP1	Shift register SP
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source
11	LED (future)	Supply for future LED source
12	LED (future)	Supply for future LED source

The connector for Section 2 has eight pins and is located on the left-hand side. The part number is JAE IL-Z-8P-S125L3-E. The pin numbers and designations for the connector are listed in Table 2.

Table 2: Pin Configuration for Section 2 Connector

Pin Number	Symbol	Names and Functions
1	Vout2	Analog video output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V)	Negative power supply
5	Gnd	Ground; 0V
6	SP2	Shift register SP
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse

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5.0 Absolute Maximum Rating

Table 3: Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply voltage	Vdd	7	V
	Idd	70	mA
	Vn	-15	V
	In	20	mA
	VLED	6.0	V
	ILED	0.65	A
Input clock pulse (high level)	Vih	Vdd +.5	V
Input clock pulse (low level)	Vil	-0.5	V

Note: These are the absolute maximums and are not to be used in prolonged operation.

6.0 Operating Environment

Table 4: Operating Environment

Parameter	Symbols	Maximum Rating	Units
Operating temperature	Top	0 to 50	°C
Operating humidity	Hop	10 to 85	%
Storage temperature	Tstg	-25 to +75	°C
Storage humidity	Hstg	5 to 95	%

7.0 Electro-Optical Characteristics at 25°C

Table: Electro-Optical Characteristics at 25°C

Parameter	Symbol	Parameter	Units	Note
Total number of photo detectors		2592	Elements	The sum of both sections
Number of detectors in Section 1		1248	Elements	
Number of detectors in Section 2		1344	Elements	
Pixel-to-pixel spacing www.DataSheet4U.com		84.7	µm	
Line scanning rate	Tint(1)	270	µsec	@ 5.0MHz clock frequency
Clock frequency(2)	f	5.0	MHz	
Bright output voltage(3)	Vpavg	1.0	V	
Bright output non-uniformity(4)	Up	<+/-30	%	
Adjacent pixel non-uniformity(5)	Uadj	<25	%	
Dark non-uniformity(6)	Ud	<100	mV	
Dark output voltage(6)	Vd	<150	mV	Average dark level from the video reset level
Typical modulation transfer function(7)	MTF	50	%	

Notes:

(1) Tint: Line scanning rate or integration time. Tint is determined by the interval of two start pulses. The line scan time is determined by the longest array with both Section 1 and 2 operating in parallel. The longest array is Section 2, with 1344 pixels, running at a 5MHz pixel rate.

(2) f: main clock frequency

(3) Vpavg = $\sum Vp(n)/1248$ for section 1 and Vpavg = $\sum Vp(n)/1344$ for Section 2, where: Vp(n) is the peak value of any n^{th} pixel in a give scan.
This level is factory adjusted with an internal potentiometer after setting the scan times to the minimum allowable for a fixed clock frequency. In this case, ≈ 275µsec at 5MHz clock frequency. This value is then used as a reference to adjust the dark level and to call out the dark uniformity (see Note 6 on dark uniformity).

(4) Up is defined as follows: Upmax = [(Vpmax - Vpavg) / Vpavg] x 100% or Upmin = [(Vpavg - Vpmin) / Vpavg] x 100%
where: Vpmax=the maximum value of the peak n^{th} video pixel, Vp(n),
and: Vpmin = the minimum value of the peak video n^{th} video pixel, Vp(n).
Up = +/-30% is selected from the greater absolute value of Upmax of Upmin. If |Upmax| > |Upmin| then Up = +|Upmax| is selected, if |Upmin| > |Upmax| then Up = -|Upmin| is selected. In either case, |Upmax| + |Upmin| ≤ 60%.

(5) Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)] x 100%
Upadj is the non-uniformity percentage pixel to pixel

(6) See Section 8.0 for discussion on dark uniformity, Ud.

(7) See Section 9.0 on MTF Discussion and Graph.

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8.0 Dark Uniformity, Ud

Figure 3 exemplifies the definitions of the terminology, which are used to explain the video signal characteristics. Dark uniformity is defined as Ud = Vdmax - Vdmin; where Vdmax and Vdmin are the maximum and minimum voltage of Vd, the average dark level of total pixels in the scan line when the LED light is turned off. Vd is measured from the reset level and the amplitude between the dark level and this reset level is called pedestal. The pedestal level is caused by the resetting operation of the pixel. Although the pedestal remains constant for a constant clock frequency, the reset level will vary from ground because the dark level, Vd, is factory adjusted to ground (0V).

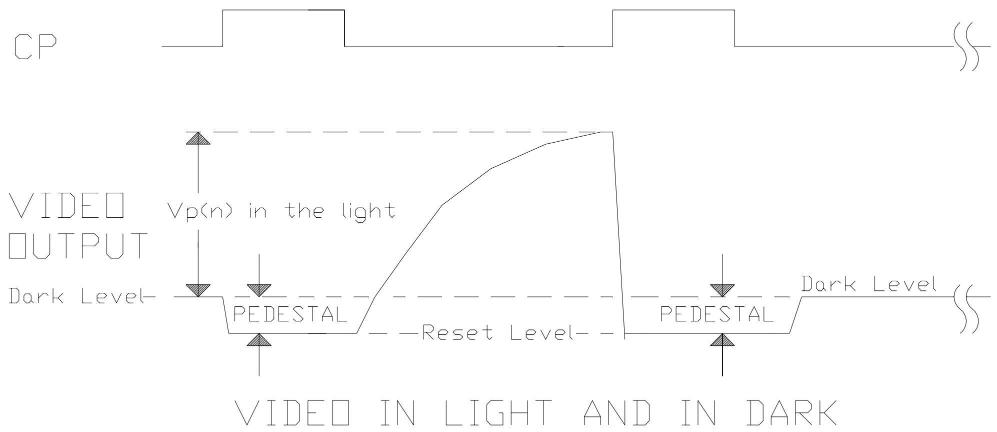

Figure 3: Definition of the Video Pixel in the Light and in the Dark

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9.0 MTF Graph and its Discussion

Figure 4 depicts MTF versus Distance. This graph essentially shows the working depth of focus. Since this module is a 300dpi module, with a pixel density of 300 pixels per inch, the MTF was measured with a 150dpi or a 75 line-pair per inch optical bar pattern. The tests were conducted at a pixel rate of 2.5MHz.

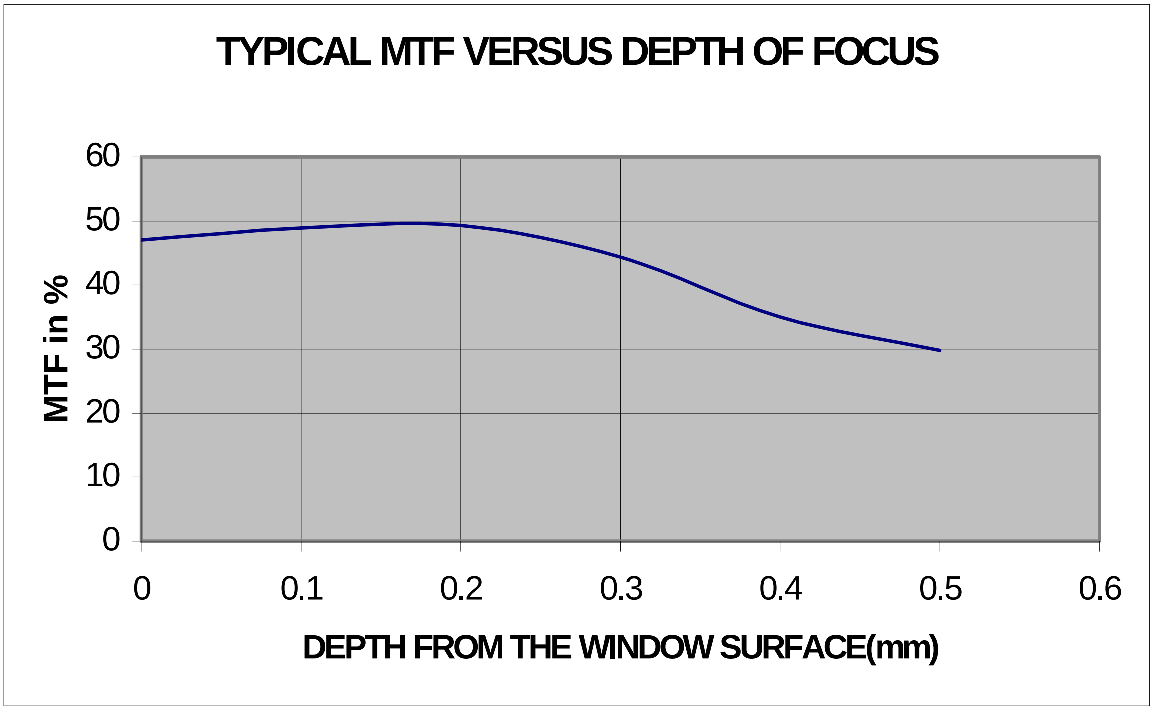

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Figure 4: MTF versus Distance

The effective algorithm used in the measurements is as described by the following equation:

MTF={[Vp(n)+Vp(n+1)]/2-[Vp(n+2)+Vp(n+3)]/2}/{[Vp(n)+Vp(n+1)]/2+[Vp(n+2)+Vp(n+3)]/2}
Where n is 1, 2, ...2592th, Vp(n) is the signal amplitude of the nth pixel.

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10.0 Recommended Operating Conditions (25°C)

Table 5: Recommended Operating Conditions (25°C)

Item	Symbol	Min.	Mean	Max.	Units
Power supply	Vdd	4.5	5.0	5.5	V
	Vn.	-4.5	-5	-12	V
	VLED		5.0	5.5	V
	Idd (1&2)		35	55	ma
	Ivn (1&2)		6.0	10.0	ma
	ILED		460	600	ma
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.8	V
Clock frequency	f			5.5	MHz
Clock pulse high duty cycle		25			%
Clock pulse high duration		50			ns
Integration time	Tint(1)	0.270		5.0	ms
Operating temperature	Top		25	50	°C

11.0 Switching Characteristics (25°C)

The timing diagram for both arrays Section 1 and Section 2, are shown in Figure 5.

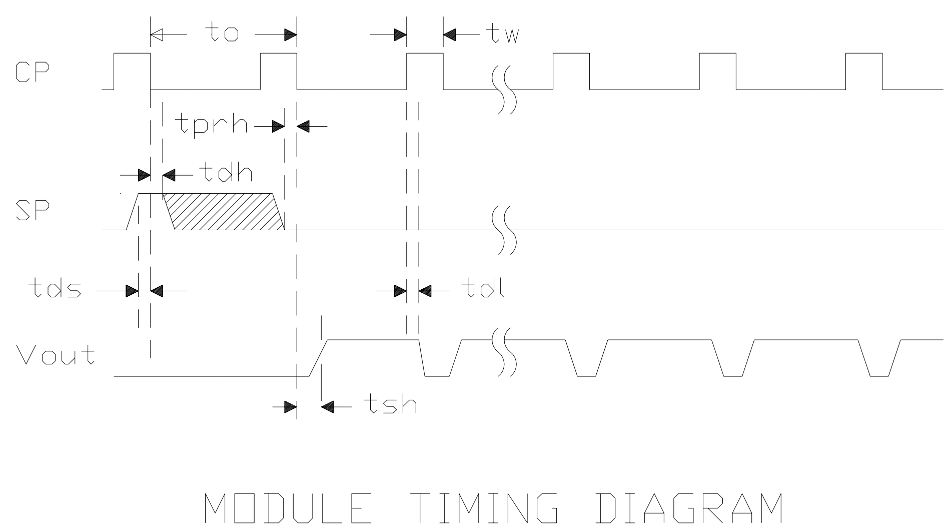

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Figure 5: Timing Diagram for both Section 1 and Section 2

The switching characteristics for the I/O clocks are labeled symbolic acronyms for each corresponding clock's switching edges. The corresponding times for these symbols are given in Table 6.

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Table 6: Symbol Definitions for the Timing Diagram

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	0.20		4.0	µs
Clock pulse width	tw	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of SP	tprh	15			ns
Data setup time	tds	20			ns
Data hold time	tdh	20			ns
Signal delay time	tdl	50			ns
Signal settling time	tsh	120			ns

12.0 AMIS-710324-A4 Module and its Mechanical Dimensions

Figure 6 is an overview drawing of the module. If a detailed drawing is desired, especially for a design in application, a full size drawing is available upon request.

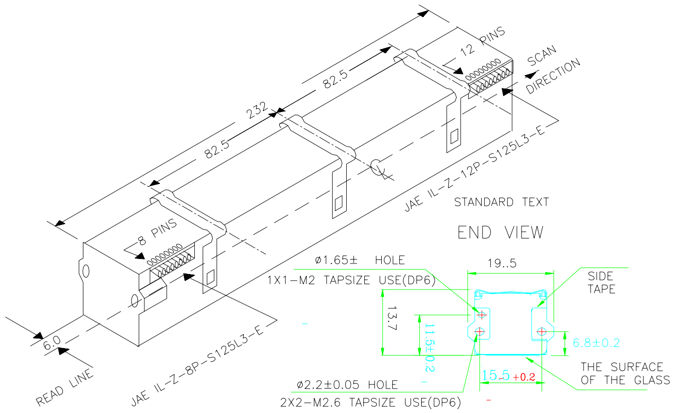

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Figure 6: Mechanical Overview of the Module

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13.0 Company or Product Inquiries

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