1.0 General Description

The AMIS-710400-A4 (PI400M-A4) is a contact image sensor (CIS) module. It is a long contact image sensor, using MOS image sensor technology for high-speed performance and high sensitivity. The AMIS-710400-A4 is suitable for scanning A4 size (216mm) documents with 15.7 dots per millimeter (dpm) resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- 15.7dpm resolution, 216mm scanning length
- 700μsec/line scanning speed @ 5.0MHz clock rate
- Wide dynamic range
- Analog output
- Yellow-Green light source 575nm
- Compact size $\cong$14.6mm x 19.5mm x 232mm
- Low power
- Light weight

3.0 Functional Description

The AMIS-710400-A4 imaging array consists of 27 sensors, which are cascaded to provide 3456 photo-detectors with their associated multiplex switches and a digital shift register, which controls its sequential readout. Mounted in the module is a one-to-one graded indexed micro lens array, which focuses the scanned documents to image onto its sensing plane. The on-board amplifier processes the video signal to produce a sequential stream of video at the video output pin of the AMIS-710400-A4 module.

Illumination is accomplished by means of an integrated LED light source. All components are housed in a small plastic housing, which has a cover glass, which acts as the focal point for the object being scanned and protects the imaging array, micro lens assembly and LED light source from dust. I/O to the module is the 10-pin connector located on one end of the module (see Figure 4). The cross section of the AMIS-710400-A4 is shown in Figure 1 and the block diagram in Figure 2.

AMI **SEMICONDUCTOR**
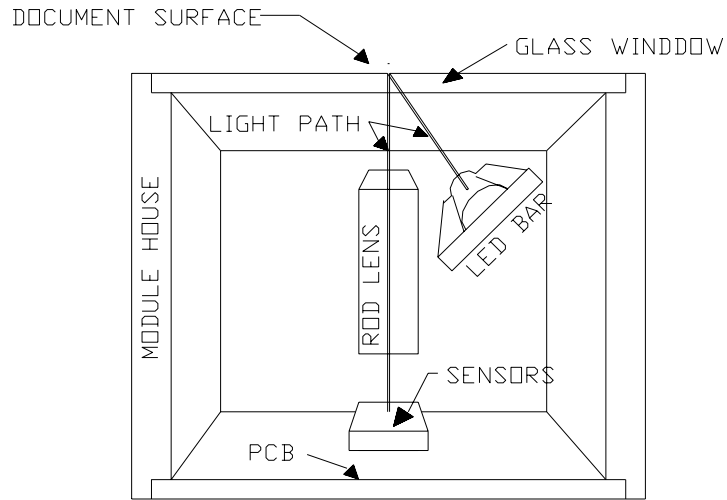
Data Sheet

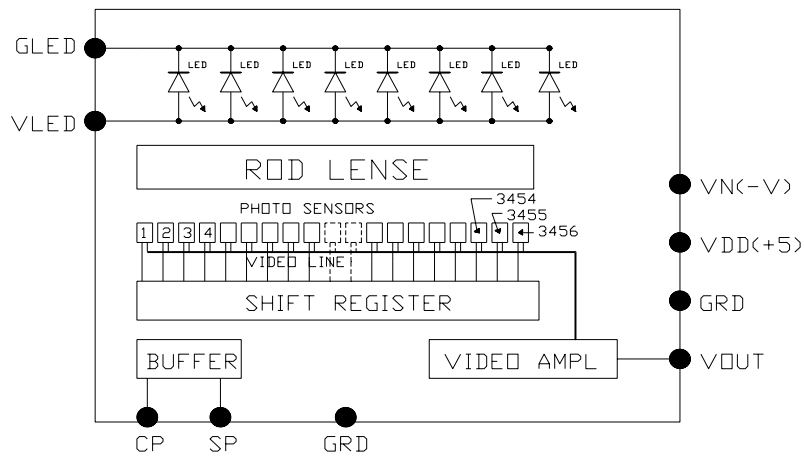*Figure 1: AMIS-710400-A4 Cross Section*

Figure 2: AMIS-710400-A4 Module Block Diagram (See Table 1 for Pin Configuration)

Table 1: Pin Configuration

Pin Number	Symbol	Names and Functions
1	Vout	Analog video output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V to -12V)	Negative power supply
5	Gnd	Ground; 0V
6	SP	Shift register start pulse
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source

4.0 Absolute Maximum Rating

Table 2: Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply voltage	Vdd	10	V
	Idd	60	ma
	Vn	-15	V
	In	10	ma
	VLED	6	V
	ILED[1]	250	ma
Input clock pulse (high level)	Vih	Vdd – 0.5	V
Input clock pulse (low level)	Vil	-0.5	V

Note:
(1)   The LED light source is for current-controlled operation. The output video is adjusted to a 1.0V maximum, using a standard white document - similar to white typing paper.

5.0 Environmental Specifications

Table 3: Operating and Storage Environment

Parameter	Symbols	Maximum Rating	Units
Operating temperature[1]	Top	0 to 50	°C
Operating humidity[1]	Hop	10 to 85	%
Storage temperature[1]	Tstg	-25 to+75	°C
Storage humidity[1]	Hstg	5 to 95	%

Note:
(1)   These are standard specifications for the CIS modules. The TBD is to show that these parameters will be tested later and added to our data sheet.

6.0 Electro-Optical Specifications at 25°C

Table 4: Electro-Optical Specifications at 25°C

Parameter	Symbol	Parameter	Units	Note
Number of photo detectors		3456	Elements	
Pixel-to-pixel spacing		63.5	μm	
Line scanning rate	Tint[1]	864	μsec	@ 4.0MHz clock frequency
Clock frequency[2]	f	4.0	MHz	
Bright output voltage[3]	Video output	1.0	Volts	
Bright output non-uniformity[4]	Up	<50	%	
Dark non-uniformity[5]	Ud	150	mV	
Dark output voltage[6]	Dark level	100	mV	
Modulation transfer function[7]	MTF	>30	%	

Notes:
(1)   Tint: line scanning rate or integration time. Tint is determined by the interval between two start pulses (SP).
(2)   f: main clock frequency, which also equals the video sampling frequency.
(3)   The video output level is controlled with LED current source.
(4)   Up = {[Vp(max) –Vp(min)]/Vp(max)}x100%
        Where VP(max) = maximum peak pixel and VP(min) = minimum pixel.
(5)   Ud = Vdmax – Vdmin
        Vdmin is the minimum output voltage with LED off.
        Vdmax: maximum output voltage with LED off
(6)   This level is measured from the reset level, which is located between the pixels during the pixel reset duration. The reset level is at ground, 0V. It can be adjusted with the offset potentiometer located on the module.
(7)   MTF = [(Vp(n) – Vp(n+1)] / (Vp(n)+ Vp(n+1)) x 100 [%]
        Vp(n): n[th] maximum output pixel from a 8.0lp/mm target.
        V(n+1)[th]: (n+1)[th] minimum output pixel from a 8.0lp/mm target.
(8)   lp / mm: line pair per mm

7.0 Recommended Operating Conditions (25°C)

Table 5: Table 5: Recommended Operating Conditions (25°C)

Item	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd	4.5	5.0	5.5	V
	Vn.	-4.5	-5	-12	V
	Idd				ma
	ILED			250	ma
	VLED		+5.0		V
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.8	V
Clock frequency	f	0.5	4.0	5.0	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration			62.5		ns
Integration time	Tint		864		μs
Operating temperature[1]	Top		25	50	$^\circ$C

Note:
(1)   See the note under Table 3.

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8.0 Switching Characteristics (25°C)
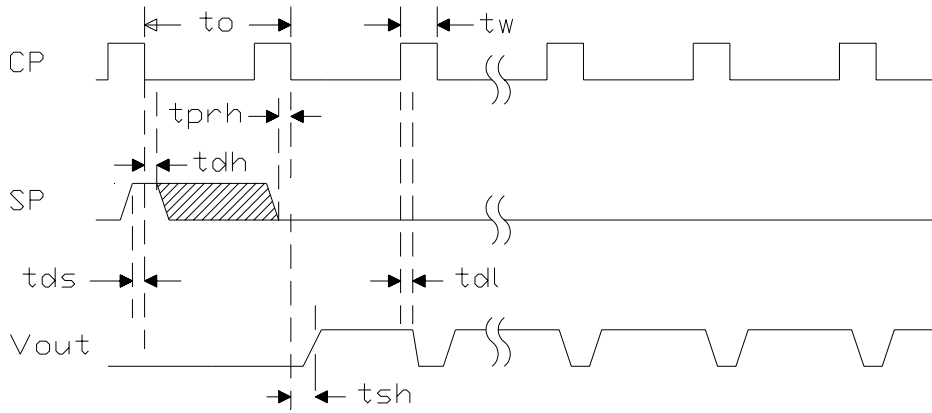
Figure 3: Module Timing Diagram

The switching characteristics (at 25°C) for the I/O clocks are shown in Figure 3. For the timing symbol definitions see Table 6.

Table 6: Timing Symbol's Definition and Timing Values

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	0.20		2.0	μs
Clock pulse width	tw	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of SP[1]	tprh	0			ns
Data setup time	tds	20			ns
Data hold time	tdh	0			ns
Signal delay time	tdl	20			ns
Signal settling time	tsh	100			ns

Note:

"Prohibit crossing of start pulse" is to indicate that the start pulse should not be active high between any two consecutive high going clock pulses or two consecutive low going clock pulses (see Figure 3). Only one high going clock under the active high start pulse initiates the internal shift register, and it must not be active over two high going clocks. All low going clock pulses will not initiate the shift register, but to ensure that the start pulse will not be actively high during two consecutive high going clocks, the circuit should be designed to keep the start pulse active only for one low going clock cycle.

9.0 Mechanical Structure of the Module

For the dimensions of the AMIS-710400-A4 module see Figure 4.
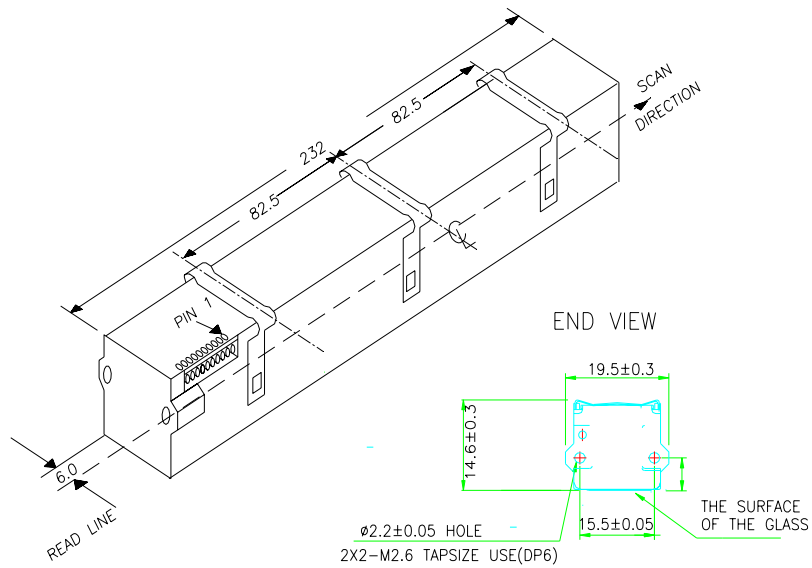
Figure 4: Mechanical Structure

10.0 Company or Product Inquiries

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