1.0 Description

The AMIS-710651-A4 (PI651MC-A4C) is a color contact image sensor (CIS) module. The module contains 15 image-sensor chips, AMIS-720058 (PI6058E), a product of AMI Semiconductor. These chips are sequentially cascaded to provide a line array of photo-detectors. Each photo-detector in the image sensor possesses its own independent processing circuit. As the photo-sensors' digital shift register scans the image sensor chip, it sequentially produces the video signals at the output of the image array. The AMIS-710651-A4's mechanical outline drawing is shown in Figure 6.

2.0 Key Features

- 600 and 300dpi selectable resolutions
- 23.6dpm and 11.8dpm, 216mm scanning length
- 344 or 172 image sensor elements (pixels)
- Low power-single power supply at 3.3V
- Light source, lens and sensor are integrated into a single module
- High speed page scan - up to 1.30msec/line @ 4MHz pixel rate
- Analog output
- RGB color LED light source
- Compact size ≅ 12.3mm x 18.9mm x 23mm
- Light weight

3.0 Overview

The AMIS-710651-A4 has a 216mm read width. Its minimum line rate is 1.30ms/line with a maximum clock pulse (CP) equal to 4.0MHz (pixel rate (PRATE) of 4.0MHz). Unless stated otherwise, all data was taken with CP = 3.0MHz (PRATE = 3.0MHz) and an integration time of 1.75ms/line. The sensor photo-site density is 23.64elements/mm. The module has one analog video output, two clock inputs, clock and start pulse (CP and SP), one reference voltage input for the amplifier output bias level control, one power supply input and four LED inputs.

4.0 Scan Overview

Table 1 describes a scan overview.

Table 1: Scan Overview

Parameter	Specification	Note
Read width	216mm	
Sensor photo-site density	42.3 elements/mm 84.7 elements/mm	600dpi 300dpi
Active photo elements	5160 elements	
Line read time (1)	~ 1.30ms/line	Tested @ 4.0MHz (PRATE)
Clock frequency (1)	4.0MHz	Max. rate
Pixel rate (1)	4.0MHz	Max. rate

Note:
Since the light power is fixed, if the line-scan rate is set proportional to the clock rate, then the integration time reduces as the clock frequency is increased, hence its exposure. The reduction in the exposure proportionately reduces the video output. Accordingly, the signal-to-noise ratio reduces as the frequency increased.

5.0 Physical Overview

Table 2 describes a physical overview.

Table 2: Physical Overview

Parameter	Specification	Note
Image sensors	A<OS-720058	See image sensor data sheet
Module outside dimension	≅12.3mm x 18.9mm x 232mm	Figure 6
Circuit power supply	Typical 3.3V @ 70mA	
Data output	One analog output	

6.0 Recommended Operating Conditions

All tests were conducted at the typical pixel rate of 3.0MHz

Table 3: Recommended Operating Conditions (25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	VDD		3.3		V
	IDD		70	100	mA
Video output level	VP (1)	0.15	0.2		V
Reference voltage input	VREF (2)		1.2		V
Input voltage for digital high (input clocks, SP and CP)	VIH	3.2	VDD	VDD +0.3	V
Input voltage for digital low (input clocks SS and CP)	VIL	0		0.8	V
Clock frequency	FREQ (3)	0.50	3.0	4.0	MHz
Pixel frequency	PRATE (3)	0.50	3.0	4.0	MHz
Clock pulse high duty cycle	DUTY (4)		50		%
Clock pulse high duration	TPW	200			ns
Integration time	TINT (5)	~1300		10000	µs
Operating temperature	TOP (6)		25	50	°C

Notes:

(1) VP represents the average value Vp(n) for all n in line scans, where n is the sequential number of a pixel. This signal pixel level should be operated at less than saturation levels, i.e., <1.3V.

(2) VREF is used to adjust the video output bias. Under normal operation it is left unconnected.

(3) FREQ is the input clock (CP) frequency and the pixel rate (PRATE). The minimum rate for FREQ and PRATE should be consistent with the maximum TINT, see Note (5).

(4) DUTY is the ratio of the clock's pulse width to its pulse period.

(5) TINT is the time interval between two start pulses (SP). Hence, if SP is generated from a clock count down circuit, it will be directly proportional to the clock frequency. There must be a minimum of (56+1204) clock cycles between the two SPs. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion to determine the desired leakage tolerance level for the given system.

(6) TOP is a conservative engineering estimate. It is based on measurements of similar CIS modules. In production, they are measured under standard QA practices, that is, under the control of ISO 9000 standards.

7.0 Electro-Optical Characteristics (25°C)

All tests were conducted at the typical pixel rate of 3.0MHz

Table 4: Electro-Optical Characteristics (25°C)

Parameter	Symbol	Typ.	Units	Note
Number of active photo detectors		5160 2580	Elements	600dpi 300dpi
Pixel-to-pixel spacing		42.3 84.6	µm	600dpi 300dpi
Line scan rate	TINT (1)	~1.75	ms/line	@ 3.0MHz clock frequency
Clock frequency	FREQ (2)	3.0	MHz	
Pixel rate	PRATE (2)	3.0	MHz	
Bright output voltage	Vpavg (3)	0.2	V	
Bright output non-uniformity	+/- Up (4)	< /-30	%	
Bright output total non-uniformity	Uptotal (5)	<60	%	
Adjacent pixel non-uniformity	Uadj (6)	<25	%	
Dark non-uniformity	Ud (7)	<150	mV	
Dark output voltage range	VDL (8)	1.2<VDL<1.5	V	
Random noise	RNL (9)	<24 <4	p-p mV rms mV	
Modulation transfer function	MTF (10)	40	%	

Notes:

(1) Scan rate (integration time), TINT, is determined by the time interval between two SPs. See Table 3, Note 5.

(2) Clock frequency, FREQ, is the input clock frequency and its corresponding PRATE is the pixel sample rate.

(3) Bright output voltage Vpmax = maximum pixel value of Vp(n), Vpmin = minimum pixel value of Vp(n), Vpavg = $\sum$ Vp(n)/5160; where Vp(n) is the n^{th} pixel in a line scan with the module scanning a uniform white target and Vp values are measured with a uniform exposure.

(4) Bright output non-uniformity Up(+) = [(Vpmax - Vpavg) / Vpavg] x 100%, Up(-)= [(Vpavg - Vpmin) / Vpavg] x 100%, whichever polarity with the highest absolute value is selected.

(5) Bright output total non-uniformity: Uptotal = [Vpmax -Vpmin]/Vpavg x 100%

(6) Adjacent pixel non-uniformity: Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n))] x 100%
Upadj is the non-uniformity in percentage. It is the maximum difference amplitude between two neighboring pixels.

(7) Dark non-uniformity: Ud = Vdmax – Vdmin
Vdmax is the max. pixel value of the video pixel in the dark. Vdmin is the min. pixel value of the video pixel in the dark. The references for these levels are the dark level (VDL).

(8) Dark output voltage range (VDL) is the level between the output dark level and ground.

(9) Random noise (RNL): The rms value was calculated from measured p-p thermal noise taken at output from a selected pixel. The rms is defined as one standard deviation of at least 64 pixels sampled. The calculation of the standard deviation is based on an idealized Gaussian probability curve.

(10) Modulation transfer function is defined as MTF = [(Vmax - Vmin) / (Vmax + Vmin)] x 100%. MTF is a measure at the glass surface. Vmax is the maximum output voltage at 300lp/inch (at 1/2 of the optical Nyquest frequency) and Vmin is the minimum output voltage at 300lp/inch.

8.0 Electrical Clocking Characteristics

Table 5: Clock Amplitude Duty Characteristics (25°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock input voltage	VIH(1)	See Table 3			
	VIL (1)				
Clock frequency	FREQ (2)	Note 3	3.0	4.0	MHz
Pixel rate	PRATE (2)	~1.30	3.0	4.0	MHz
Line read time	TINT (4)	45		~10	ms
Clock pulse duty cycle	Ratio = twp / tp (5)				%

Notes:

(1) The clocks, CP and SP are compatible with CMOS clock drivers.

(2) FREQ is the clock frequency and PRATE is the pixel sample rate.

(3) Minimum values are not specified because it will be determined by the maximum TINT value. See Note 4.

(4) TINT is the line scan read time, which depends on the interval between the SP entries. The minimum time is determined by (1/clock frequency) x (5160 + 150) pixels. Note that there are a few extra pixels used to determine the typical line time of 820µsec @ 3.0MHz PRATE (see Figure 1). There are 55 clocks required to transfer and reset the photo-sites before the video can be scanned out. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.

(5) The definition for the symbols used in the ratio is defined in Figure 1. A duty cycle of exactly 50 percent is recommended to maintain equal pixel duration between odd and even pixels.

9.0 Timing Diagram

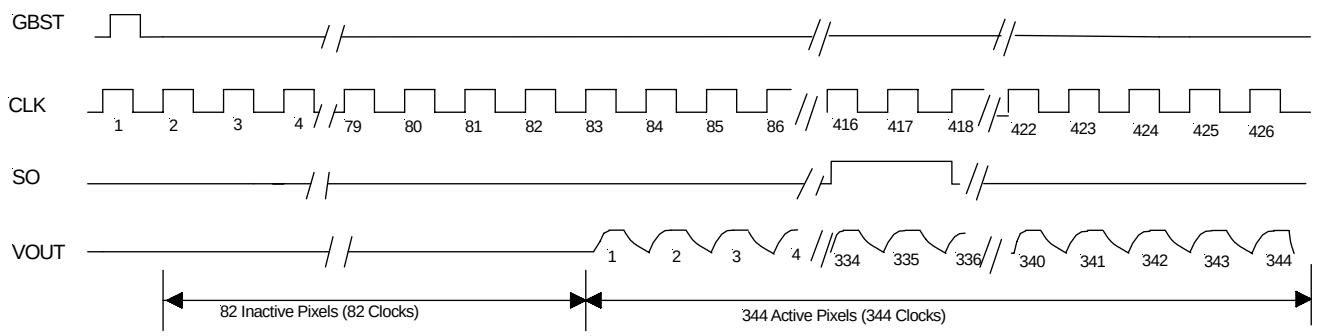

Figure 1: Overall Timing Diagram for the 600dpi Mode

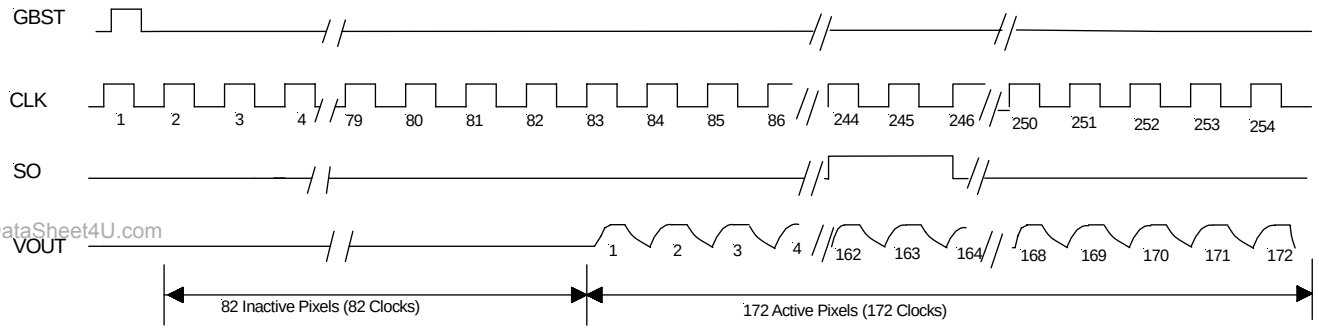

Figure 2: Overall Timing Diagram for the 300dpi Mode

Figure 1 and Figure 2 detail the timing of the CLK, GBST, Vout, and SI/SO signals in further detail, which have the same timing requirements for both the 600 and 300dpi modes. In Figure 1, note that Pixel 83 is the first active pixel because the first 82 pixels are dummy pixels.

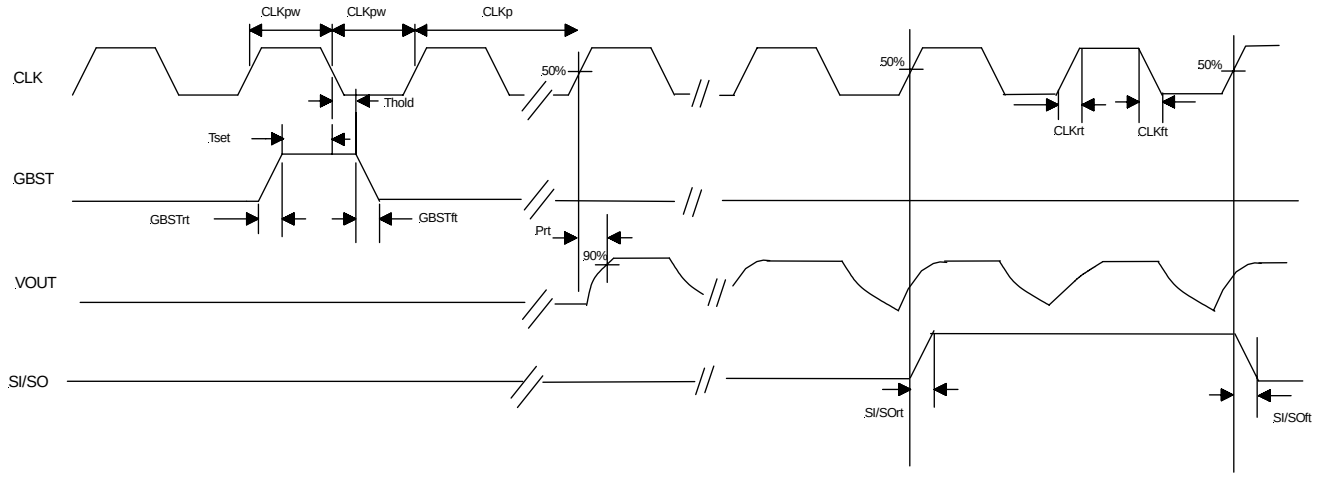

Figure 3: Rise and Fall Times for both the 600/300dpi Modes

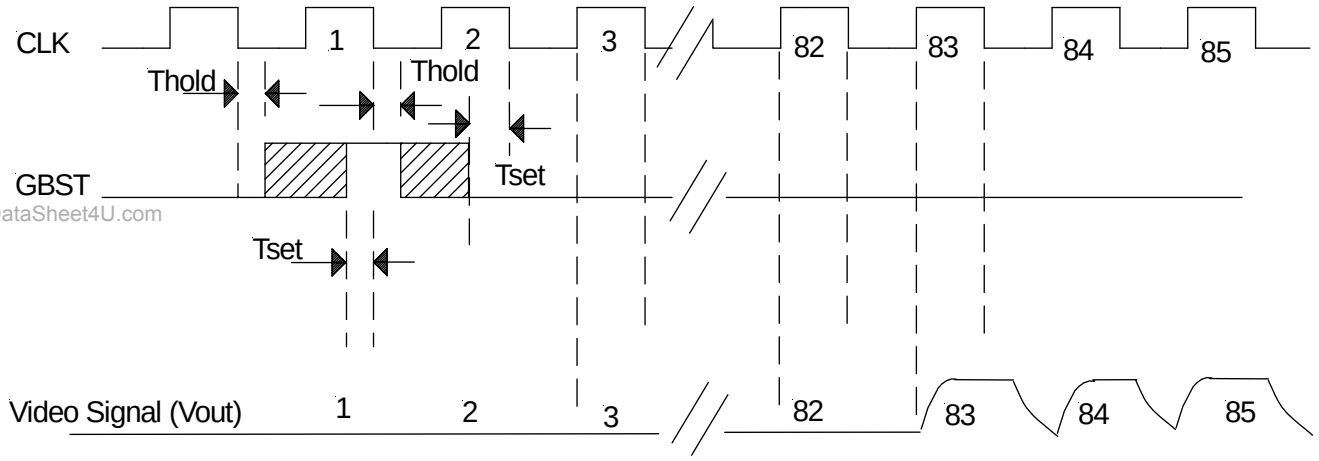

Figure 4: Timing of GBST-to-First Pixel of the First Sensor for both the 600/300dpi Modes

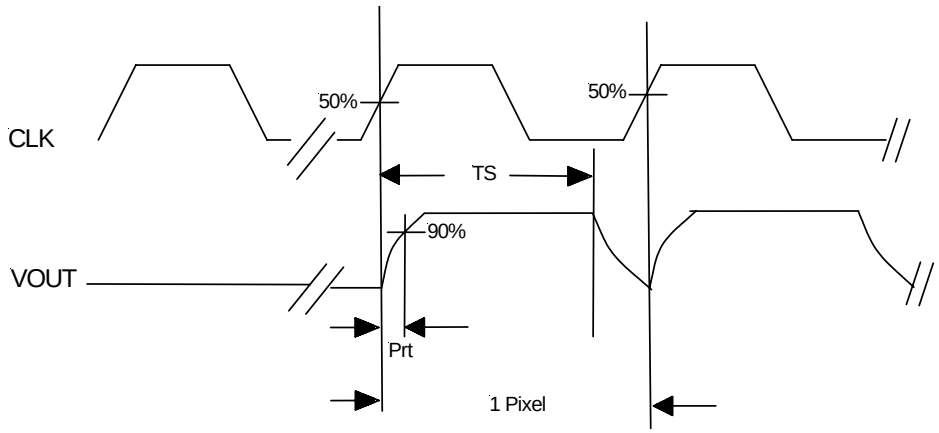

Figure 5: Pixel Timing

Table 6: Clock Timing Characteristics for Timing Diagrams

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	CLKp	250	250	2000	ns
Clock pulse width	CLKpw		125		ns
Clock duty cycle			50		%
Prohibit crossing time SP	tprh	30			ns
Data setup time	Tset	20			ns
Data hold time	Thold	25			ns
Signal delay time	tdl			50	ns
Signal settling time	tst			130	ns
Signal fall time	tsigf			60	ns

Notes:

(1) All of the symbol definitions used in Table 6 are shown in the figures in Section 9.0. The clocks, CP and SP are compatible with CMOS clock drivers.

(2) Maximum clock cycle time, as with minimum FREQ, must be consistent with maximum TINT. See Table 3, Note 3.

10.0 Maximum Ratings

Table 7: Maximum Ratings (Not to be Used for Continuous Operation)

Parameter	Symbol	Specification	Note
Power supply voltage	VDD	3.3V	
Input voltage	VIN	VDD	SP & CP
Ambient temperature	TA (PCB surface)	0 to 50°C -10 to +75°C	Operational storage
Ambient humidity	HA	0 to 80%	Non-condensing
Maximum operating case temperature	PCB temperature	70°C	

11.0 I/O Connector Pin Configuration

The connector is for a 12-pin flex-strip-line cable, PDK97-1201. The connector location is shown in Figure 6, an ISO drawing of the AMIS-710651-A4 module. It also shows the location of Pin 1.

Use caution when connecting the power to the LED!

Note that all the negative sides of the LED sources are connected to the cathodes. These I/O sources are current inputs. Constant current sources are used to control the balance of the color in the RGB outputs. Their typical voltage drops are between 2.3 to 2.7V. Under no circumstances should the applied current be greater than 30mA, otherwise the LED source will be damaged.

Table 8: Connector Pin Outs

Pin Number	Pin Names	Symbol	I/0	Names and Functions
1	Analog signal output	VOUT	O	Analog signal output
2	Ground	GND	I	Ground; 0V
3	Power supply	VDD	I	Positive 3.3V
4	DPI-control	SR	I	Selects resolution control
5	Reference voltage	VREF	I	For externally or internally controlling the dark bias level
6	Start pulse	SP	I	Shift register start pulse
7	Ground	GND	I	Ground; 0V
8	Clock	CP (CLK on the schematic)	I	Clock input for the module
9	Common	VLED (common anode on the schematic)	I	Common anodes for all LED, plus 5.0V terminal
10	LED green	GLED	I	Cathode green LED input
11	LED red	RLED	I	Cathode red LED input
12	LED blue	BLED	I	Cathode blue LED input

12.0 Mechanical Outline Drawing

A simplified ISO drawing of the module housing is shown Figure 6. The drawing is not to scale but sufficient dimensions are shown for use in a preliminary application study. Furthermore, it shows the I/O connector location, its Pin 1 location, the read line location and LED pad locations. For detailed design information, please contact AMIS for a complete housing drawing.

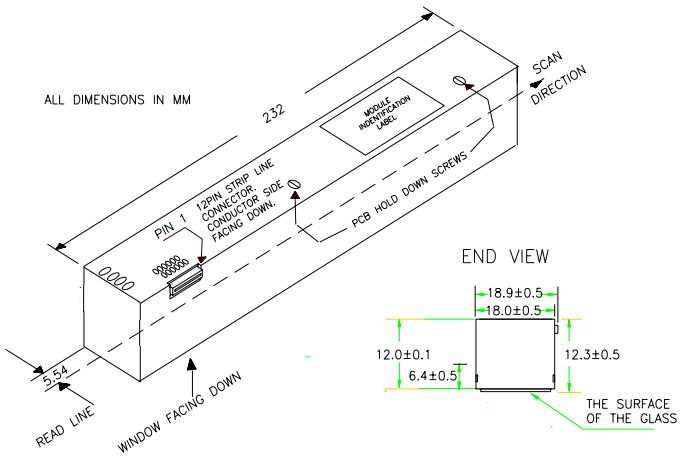

Figure 6: Mechanical Structure

13.0 Company or Product Inquiries

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