

# AML 6210DP A/V Processor User's Guide

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## Revision History

Revision Number	Revised Date	By	Changes
0.1	2008/3/3	bwester	Initial release
0.2	2008/3/3	Bwester	Fix some errors in diagram and text
0.3	2009/2/13	J Z	Revise pin description
0.4	2010/03/25	J Z	Revise content

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# 1 Introduction

The AML6210DP A/V processor is a complete integrated system targeting the digital picture frame market. The device combines a super fast JPEG decoder, all digital LCD drivers/TCON signals, USB and card-reader I/Os and a 32-bit host CPU in a small 144 pin package.

The embedded 32-bits core CPU handles all system related application software. It executes AVOS, the base operating system for AML6210DP. All applications and drivers run on top of AVOS. Drivers including USB drivers, card-reader hardware driver, and video and other hardware related programming interfaces are provided by AVOS. Applications include graphical user interfaces and file system sub-system are also included. Developers can add additional applications to customize for each platform.

The core CPU interfaces to the video and audio processing hardware. It performs advanced digital audio decoding. It provides support for all existing audio formats and it also has enough flexibility to accommodate new audio standards. Popular audio formats like MPEG Layer I/II/III, LPCM, MP3, WMA, AAC and WAV can be supported.

JPEG pictures are processed by dedicated picture decoding hardware and the flexible Picture AMRISC™ engine. The hardware and microcode combination is capable of decoding JPEG pictures with no limits in picture resolution. Once decoded, the output pictures are passed to a sophisticated video sub-system that performs image analysis, enhancement and scaling functions. Contrast enhancement, hue adjustment, video scaling, video interpolation, and zoom are also supported. The high-resolution scalar supports both up-scaling and down-scaling of images and video. The scalar can also mix in multiple graphics and OSD layers for the final display. The integrated video encoder supports all digital LCD panel resolutions thru the on-chip triple panel DACs. In addition, a programmable digital LCD TCON is included for the AML6210DP to interface to digital LCD panels directly.

The AML6210DP also integrated a USB 2.0 High Speed OTG controller/PHY and card-reader controller. The card-reader controller can support SD/SDHC, MS/MS-Pro/MS-Duo/MS-Pro Duo, MMC, xD and CF cards. FAT and FAT32 file systems are supported. The USB controller can be connected to USB hard disk, FLASH drive, digital cameras and MP3 players. The AVOS drivers and applications for AML6210DP firmware includes the basic USB device driver, USB protocol stacks to support bulk and INTR transfer, Hub, Mass-Storage (MS) class and Picture Transfer Protocol (PTP). The AVOS USB firmware also supports multiple file systems and includes flexible file transfer functions between USB devices.

AML6210DP A/V processor has a set of very flexible clocking circuits that implement the adaptive AMPOWER-II power reduction algorithms. The chip works in conjunction with the AVOS software to reduce total power consumption based on processing load, type of media streams being processed and the output requirements. With AMPOWER-II, the system can reduce power consumption for portable applications and helps consumer electronics to achieve the Energy Star rating. In addition, AMPOWER-II also provides higher performance within smaller, thermally constrained environments.

## 2 Features

The AML6210DP chip is very flexible and most of the capabilities are under firmware control. The following list of features may or may not be included in the firmware library or binary, depending on the actual application and platform.

- **High Integration**
  - Embedded 32-bits core RISC processor for system control
  - Complete JPEG decoding logic and video scaling logic
  - Complete audio decoding and stereo audio DACs
  - Integrated digital LCD video signals and TCON
  - Integrated USB 2.0 High Speed OTG port
  - Integrated card reader controllers
  - Integrated NAND FLASH controller
- **JPEG Decoding**
  - Super fast hardware decoding of JPEG picture
  - Unlimited pixel resolution (currently test with 16M pixel pictures)
  - Supports scaling (zoom in or out), rotation and transition effects
  - Automatic image analysis and enhancement
- **Other Images/Pictures Decoding**
  - Decodes BMP, PNG, GIF, TIFF and other popular picture formats
  - Supports zoom in and out, rotation and transition effects
- **Special Trick Modes:**
  - Pause
  - Reverse playback
  - Multiple steps fast forward/backward
- **Picture Processing**
  - Automatic image analysis and enhancement
  - Variable steps picture zooming (up to 8x)
  - On-Screen-Display (OSD) capable of supporting 4/16/256 colors or True-Color
  - OSD alpha-blending over video display
- **TV Encoder / TCON**
  - Digital video output signals especially for digital LCD panels
  - Programmable tint, brightness and other TV enhancements
  - Integrated programmable timing controller (TCON) for digital LCD panels
- **Graphics**
  - Graphics can be scaled independently of the video output
  - Unified graphics memory architecture for maximum flexibility and system cost savings
- **Audio Decoding**
  - Full MPEG audio layers I, II and III
  - Capable of decoding popular audio formats including: MP3, WMA and WAV
- **Audio Post Processing and Output**
  - Integrated a 2-channel audio DACs
  - Muting, volume control, etc.
- **USB Interface**
  - Integrated OTG 2.0 High Speed controller and PHY
  - Backward compatible with USB 1.1 devices
  - USB OTG port can be configured as USB device, host or OTG port

- DMA support for data movement for BULK, INTR and ISO transfer
  - USB device driver, native USB protocol stack supported in AVOS firmware
  - Integrated support for Mass-storage class (MS-Class) and Picture Transfer Protocol (PTP)
  - USB Hub support
  - Video, audio and image decoding from USB attached MS-Class or PTP devices
  - Connecting to PCs or Apple computers as USB MS-Class devices
- **Card Reader Interfaces and Controllers**
- Support MS, SD/SDHC, MMC, and xD memory card formats
  - Supports reading and play back of audio and picture multimedia files
  - AVOS software supports all file operations via file system on each memory card
- **Core CPU Sub-system**
- 32-bit core CPU dedicated for user applications
  - Embedded debug interface using ICE/JTAG
  - Shared MPEG SDRAM as run time data storage for minimal system cost
  - Integrated interrupt controller
  - Integrated general purpose timers and counters
  - Integrated general purpose DMA controllers
  - Supports up to 8M bytes of 8-bit FLASH chip
  - Supports single SDRAM interface (m1\_\*). The SDRAM interface can support 8M or 16M bytes of SDRAM.
- **System, Peripherals and Misc. Interfaces**
- One 27 MHz crystal oscillator for A/V system
  - AMPOWER-II power reduction algorithm for portable devices
  - Numerous programmable GPIO pins for system control and interrupts
  - Integrated i2c master controllers, remote control input circuitry, quad PWM output pins
  - 1.25 volt and 3.3 volt power supplies
  - 3.3 volt I/O support
  - 144 pins LQFP RoHS package

## 3 External Interfaces

### 3.1 Global Configurations

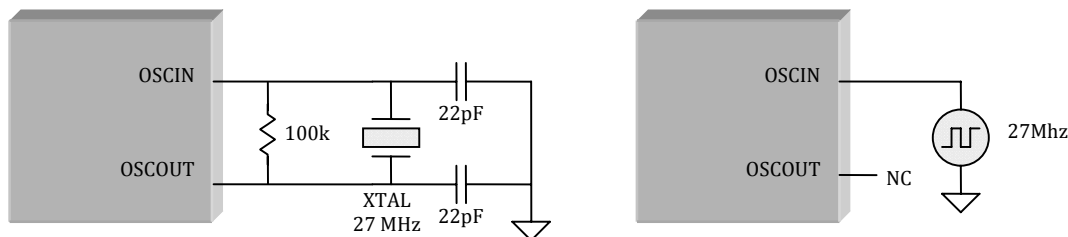
#### 3.1.1 Power-On Configuration

The chip has a common active-low reset signal called *reset\_n*. This signal puts the entire chip into a known state by resetting internal registers and state-machines to their default states. Typically this signal is held low for at least 100 msec after the power and crystal clock is stabilized. The reset process also plays a role in configuring certain functions within the chip. Using the state of the configuration pins and the rising edge of the *reset\_n* signal, the user can dictate the configuration of the JTAG pins and the boot device. The configuration pins should be pulled up or down using 10K resistors to either 3.3v or ground.

PIN	Function
m1_a_10	This pin controls the <b>JTAG</b> configuration after RESET: <ul style="list-style-type: none"> <li>➤ Tie to 3.3v with 10k resistor for JTAG debugging</li> <li>➤ Tie to ground with a 10k resistor to use the JTAG pins as GPIO</li> </ul>
m1_we_n	This pin controls the <b>Boot Option</b> after RESET: <ul style="list-style-type: none"> <li>➤ Tie to 3.3v with 10k resistor if the boot device is NAND FLASH</li> <li>➤ Tie to ground with a 10k resistor if the boot device is NOR FLASH</li> </ul>
m1_dqml	This pin controls the <b>FLASH Data Wide</b> after RESET: <ul style="list-style-type: none"> <li>➤ Tie to 3.3v with 10k resistor for 16-bit FLASH device</li> <li>➤ Tie to ground with a 10k resistor for 8-bit FLASH device</li> </ul>
m1_cas_n	This pin controls the <b>NAND Page Size</b> after RESET (only for NAND flash): <ul style="list-style-type: none"> <li>➤ Tie to ground with a 10k resistor for 2048 bytes page size</li> <li>➤ Tie to 3.3v with 10k resistor for 512 bytes page size</li> </ul>
m1_ras_n	This pin controls the <b>NAND Flash Size</b> after RESET. The pin controls the number of ALE pulses that are issued to set the ROW address. <ul style="list-style-type: none"> <li>➤ Tie to 3.3v with 10k resistor for large size NAND flash device that needs 3 ALE pulses</li> <li>➤ Tie to ground with a 10k resistor for small size NAND device that needs 2 ALE pulses</li> </ul>

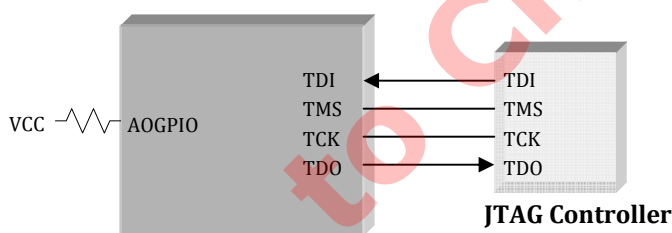
### Clocks

The AML6210DP has multiple internal clock domains, but all the internal clock domains are derived from a single external reference: *OSC*. As illustrated below, the crystal/oscillator pin pairs (OSCIN/OSCOU) can be connected to a crystal or driven from an external oscillator. In the typical A/V application, a 27 MHz crystal is connected to the *OSC* pins. The following diagram depicts a typical crystal circuit; the actual values of the components depend on the type of crystal used in the application.



### 3.1.3 JTAG for Software Development

The embedded core processor can be controlled through its JTAG port using the embedded ICE interface. The embedded ICE interface allows the developer to download code/data to the SDRAM memory, probe registers on the AML6210DP chip, execute and debug the RISC code using a user friendly development environment. The JTAG interface is enabled by tying m1\_a\_10 high as illustrated below.

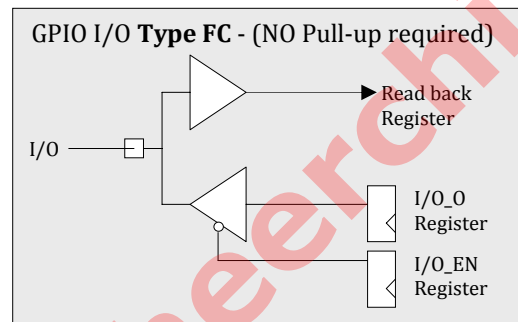
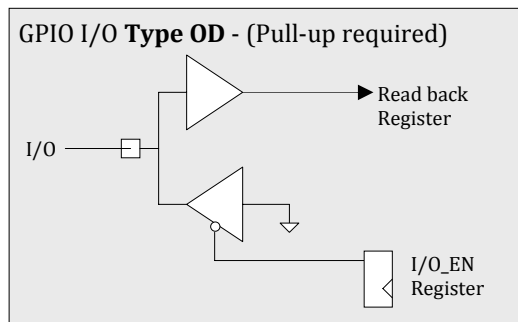
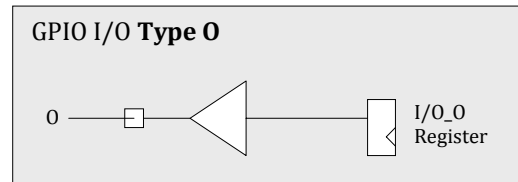
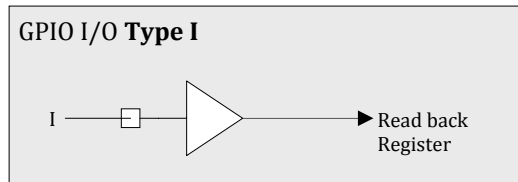


### 3.1.4 GPIOs

Configurable hardware controllers (e.g. i2c, card-reader, etc.) and DMAs are integrated into the AML6210DP device to speed up the common operations and relieve the core RISC for user-level applications. Since hardware controllers and state-machines cannot cover all possible external devices or system-level signals, numerous general-purpose I/O pins are available on the chip for purpose like Portable Media Player keypads. Each GPIO pin can be independently configured to be an input or an output. As indicated in the diagram, there are various I/O types.



**GPIO PAD TYPES**

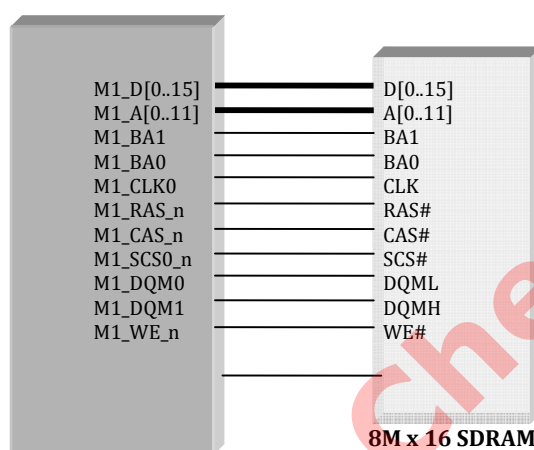


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## 3.2 Memory Interfaces

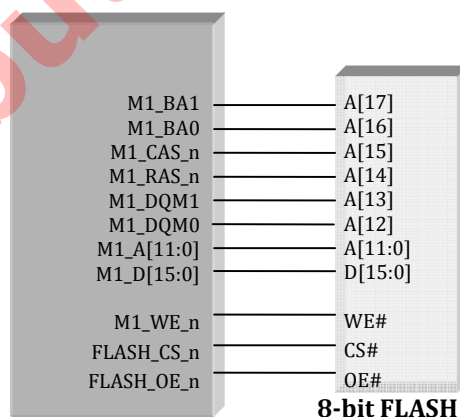
### 3.2.1 SDRAM Interfaces

The AML6210DP device uses external SDRAM for data storage and code execution. The SDRAM1 interface is labeled as *m1\_\** interface. The SDRAM interface can access up to 16M bytes of memory. Depending on the application, 166MHz 4Mx16 or 8Mx16 SDRAM chips can be used. The following example depicts a system with 8M bytes of SDRAM on *m1\_\** interface.



### 3.2.2 FLASH Interface

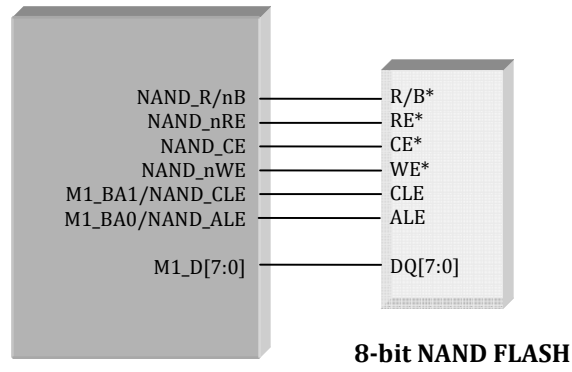
The FLASH interface can accommodate an 8-bits FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (*m1\_\**) interface. Up to 8M bytes of FLASH is accessible with the 8-bits wide FLASH interface design. The FLASH should be connected as indicated in the following diagram:



### 3.2.3 NAND FLASH Interface

The NAND FLASH interface can accommodate an 8-bits or 16-bits NAND FLASH device. Due to the limited number of I/O pins, the FLASH interface is shared with the SDRAM (*m1\_\**) interface. NAND FLASH has a very

large capacity that ranges from 32MB to more than 1GB. The NAND FLASH should be connected as indicated in the following diagram:

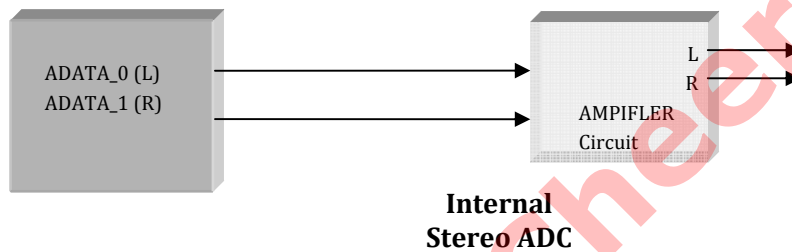


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### 3.3 Audio Interfaces

A pair of audio DACs is provided in the AML6210DP device. The audio DACs are designed for connecting to small speaker inside the photo frame or ear buds for external listening. A simple external amplifier is needed. Please see the following sample circuit diagram.

Internally, the delta-sigma algorithm is used to improve the performance and ensure high SNR output. The implementation includes a multi-tap interpolation filter which increases the sample rate of the audio channels to the modulator rate. Then the audio stream is passed through a sigma-delta modulator that generates the serial PWM data stream. An internal analog filter is then used for out-of-band noise filtering and analog signal reconstruction. External amplifier is needed to provide the necessary current to drive the speakers or head phones.



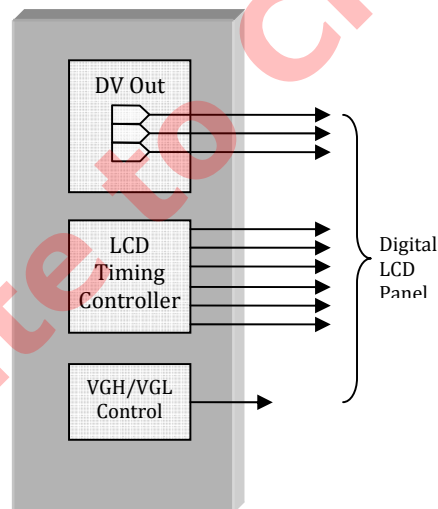
## 3.4 Video Output Interfaces

### 3.4.1 Digital Video Output

The AML6210DP integrated internal LCD video scalar and encoder and high-resolution triple panel DACs (PDAC) for direct connection to digital LCD panels. The LCD scale and encoder convert the video images to the LCD resolution and prepare the image to be displayed. Then special LCD specific dithering logic and gamma correction algorithm is applied before the video data is sent to the digital video output.

### 3.4.2 LCD Timing Controller

The AML6210DP AV processor has a built-in LCD timing controller (TCON) that works in conjunction with the digital video output to provide the best video performance on a digital LCD panel. The TCON and digital video output drive the digital LCD panel directly without any additional logic. AML6210DP's TCON is programmable and can be used in any small to medium size digital LCD panels. The LCD TCON also includes a dedicated VGH/VGL pulse generator for the LCD panel voltage generator. Together with some simple passive components, VGH/VGL can be generated.



## **3.5 Peripherals**

### **3.5.1 Card-Reader Interface**

The AML6210DP have an integrated hardware controller for SD/MS/MMC/xD card-reader operations. The hardware controller is capable of executing the low-level card interface protocols, computing the CRC or checksum, and transferring data to/from SDRAM. The hardware provides interface for the necessary signals (e.g. SD\_CLK, SD\_CMD, SD\_D0-3 for SD cards) but signals like card detect and write-protect are provided using GPIO only.

### **3.5.2 USB Interface**

AM6210DP AV processor has integrated one high speed USB 2.0 OTG controller and PHY into the chip. The output USB signal (DP/DM) can drive the external USB controller (e.g. Hub, FLASH drive, camera, PC, Mac, etc.) directly. The OTG controller can acts as a high speed USB Host or USB Device or a try OTG controller.

## 4 Operating Conditions

### 4.1 DC Characteristics

Table 4-1 DC Characteristics

$V_{DD} = 3.3 \pm 0.3V, T_A = 0 \text{ to } 65^\circ C$

Symbol	Parameters	Condition	Min	Typ	Max	Unit
$V_{IH}$	High Level Input		2.0		3.3	V
$V_{IL}$	Low Level Input		-0.3		0.8	V
VT+	Schmitt trigger, positive going Threshold			1.5		V
VT-	Schmitt trigger, negative going threshold			0.93		V
Voh	High-level output voltage	Ioh = -2.0mA to 24mA	2.4			V
Vol	Low-level output voltage	Iol = 2.0 mA to 24mA			0.4	V
$I_{IH}$	High-level input current	$V_{in} = V_{DD}$		10nA	1	uA
$I_{IL}$	Low-level input current			10nA	1	
Ioz	Tri-state output leakage current			10nA	1	
$P_D$	Power Dissipation	$V_{in} = V_{DD}$			0.8	W

### 4.2 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Table 4-2 Absolute Maximum Ratings

Characteristic	Value	Unit
1.25V Core Supply Voltage	1.4	V
3.3V Pads Supply Voltage	3.6	V
Input voltage, $V_I$	-0.5 ~ 4.6	V
Output voltage, $V_O$	-0.5 ~ 4.6	V
Junction Temperature	125	°C

### 4.3 Recommended Operating Conditions

Table 4-3 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{DD(CORE)}$	1.25V Core Supply Voltage	1.2	1.25	1.32	V
$V_{DD(PADS)}$	3.3V Pads Supply Voltage	3.0	3.3	3.6	V
$T_J$	Operating Temperature	0		65	°C

## 5 Pin-out

The AML6210DP A/V processor pin-out is described in the following table.

**Abbreviations:**

- I == Input digital pin, O == Output digital pin, I/O == Input/Output pin
- AI == Analog input pin, AO == Analog output pin, AIO == Analog input/output pin
- P == Power pin, AP == Analog power pin, NC == No connection

Pin #	Pin Name	Description	Alternate Usage / Comments	Type
1	VAA3V	Analog power	3.3V analog power	AP
2	APAD0	Audio output	Audio output - LEFT	AP
3	APAD1	Audio output	Audio output - RIGHT	AO
4	AGND	Analog ground	Analog ground	AP
5	TCON_STH2	LCD Panel signal	LCD panel clock pulse	I/O
6	TCON_STH1	LCD Panel signal	LCD panel clock pulse	I/O
7	TCON_OEV1	LCD Panel signal	LCD panel clock pulse	I/O
8	TCON_CPV1	LCD Panel signal	LCD panel clock pulse	I/O
9	VDD33	Digital I/O Power	Digital I/O 3.3V Power	P
10	TCON_STV1	LCD Panel signal	LCD panel clock pulse	I/O
11	TCON_STV2	LCD Panel signal	LCD panel clock pulse	I/O
12	VSS33	Digital Ground	Digital Ground	P
13	TCON_VCOM	LCD Panel signal	LCD panel clock pulse	I/O
14	TCON_OEH	LCD Panel signal	LCD panel clock pulse	I/O
15	TCON_CPH1	LCD Panel signal	LCD panel clock pulse	I/O
16	GPIO // XD_INS	GPIO	GPIO for card reader	I/O
17	GPIO // SD_INS	GPIO	GPIO for card reader	I/O
18	GPIO // MS_INS	GPIO	GPIO for card reader	I/O
19	NAND_WE_n	NAND Interface	NAND Interface WE	I/O
20	NAND_RDYBSY	NAND Interface	NAND Interface RDYBSY	I/O
21	NAND_CE_n	NAND Interface	NAND Interface CE	I/O
22	NAND_RD_n	NAND Interface	NAND Interface RD	I/O
23	VDD12	Digital Core Power	Digital core 1.2V power	P
24	M1_A_3	M1_A_3	SDRAM1 and/or FLASH	I/O
25	M1_A_2	M1_A_2	SDRAM1 and/or FLASH	I/O
26	M1_A_1	M1_A_1	SDRAM1 and/or FLASH	I/O
27	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
28	M1_A_0	M1_A_0	SDRAM1 and/or FLASH	I/O
29	M1_A_4	M1_A_4	SDRAM1 and/or FLASH	I/O
30	M1_A_5	M1_A_5	SDRAM1 and/or FLASH	I/O
31	M1_A_6	M1_A_6	SDRAM1 and/or FLASH	I/O
32	VSS	Digital Ground	Digital ground	P
33	M1_A_7	M1_A_7	SDRAM1 and/or FLASH	I/O
34	M1_A_8	M1_A_8	SDRAM1 and/or FLASH	I/O
35	M1_A_9	M1_A_9	SDRAM1 and/or FLASH	I/O
36	M1_A_10	M1_A_10	SDRAM1 and/or FLASH	I/O

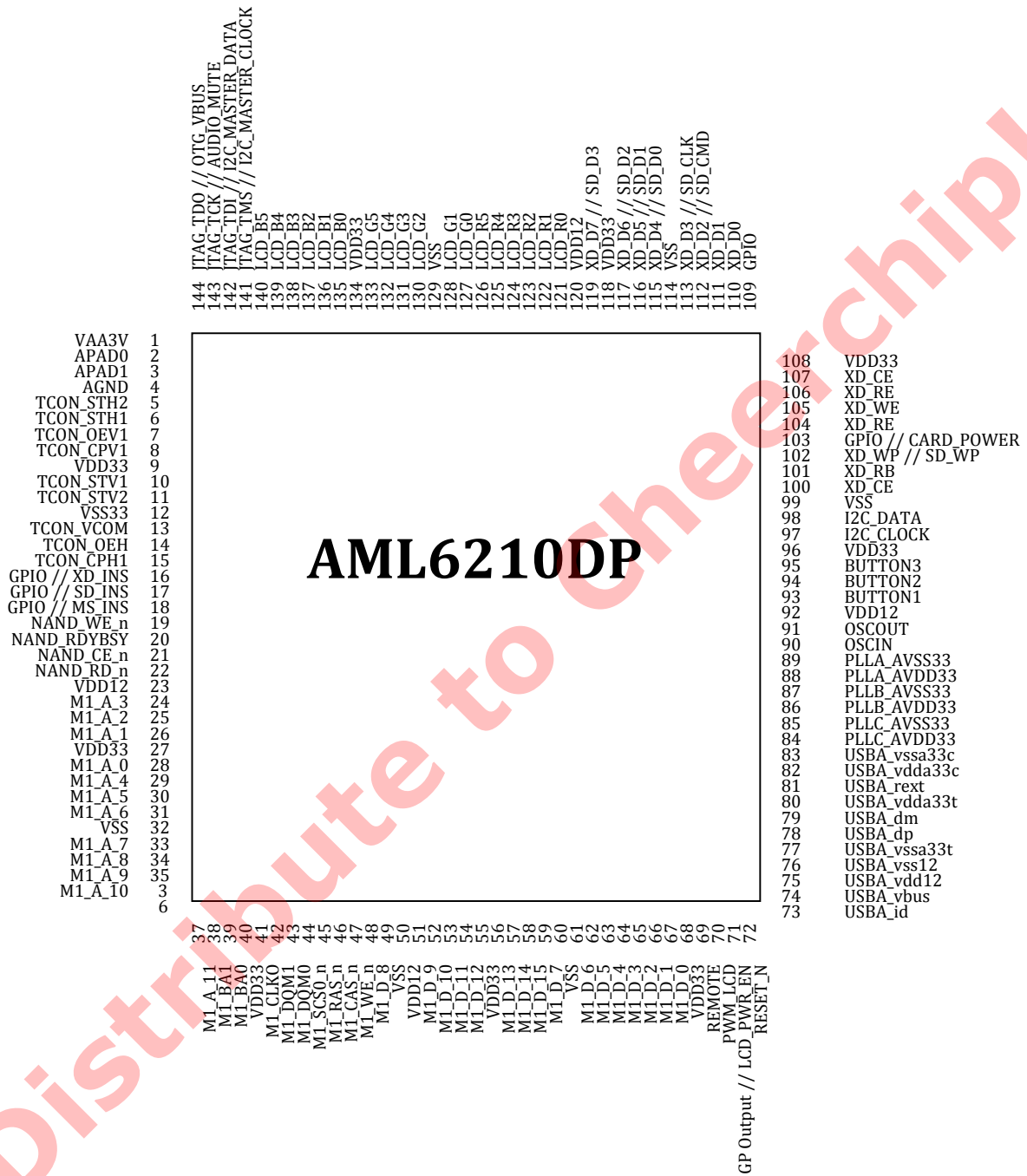


Pin	Pin name	Description	Comments / Alternate usage	Type
37	M1_A_11	M1_A_11	SDRAM1 and/or FLASH	0
38	M1_BA1	M1_BA1	SDRAM1 and/or FLASH	0
39	M1_BA0	M1_BA0	SDRAM1 and/or FLASH	0
40	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
41	M1_CLKO	M1_CLKO	SDRAM1 and/or FLASH	0
42	M1_DQM1	M1_DQM1	SDRAM1 and/or FLASH	0
43	M1_DQM0	M1_DQM0	SDRAM1 and/or FLASH	0
44	M1_SCS0_n	M1_SCS0_n	SDRAM1 and/or FLASH	0
45	M1_RAS_n	M1_RAS_n	SDRAM1 and/or FLASH	0
46	M1_CAS_n	M1_CAS_n	SDRAM1 and/or FLASH	0
47	M1_WE_n	M1_WE_n	SDRAM1 and/or FLASH	0
48	M1_D_8	M1_D_8	SDRAM1 and/or FLASH	I/O
49	VSS	VSS	Digital ground	P
50	VDD12	Digital Core 1.2V	Digital core power 1.2V	P
51	M1_D_9	M1_D_9	SDRAM1 and/or FLASH	I/O
52	M1_D_10	M1_D_10	SDRAM1 and/or FLASH	I/O
53	M1_D_11	M1_D_11	SDRAM1 and/or FLASH	I/O
54	M1_D_12	M1_D_12	SDRAM1 and/or FLASH	I/O
55	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
56	M1_D_13	M1_D_13	SDRAM1 and/or FLASH	I/O
57	M1_D_14	M1_D_14	SDRAM1 and/or FLASH	I/O
58	M1_D_15	M1_D_15	SDRAM1 and/or FLASH	I/O
59	M1_D_7	M1_D_7	SDRAM1 and/or FLASH	I/O
60	VSS	VSS	Digital ground	P
61	M1_D_6	M1_D_6	SDRAM1 and/or FLASH	I/O
62	M1_D_5	M1_D_5	SDRAM1 and/or FLASH	I/O
63	M1_D_4	M1_D_4	SDRAM1 and/or FLASH	I/O
64	M1_D_3	M1_D_3	SDRAM1 and/or FLASH	I/O
65	M1_D_2	M1_D_2	SDRAM1 and/or FLASH	I/O
66	M1_D_1	M1_D_1	SDRAM1 and/or FLASH	I/O
67	M1_D_0	M1_D_0	SDRAM1 and/or FLASH	I/O
68	VDD33	I/O Power 3.3V	Digital I/O power 3.3V	P
69	REMOTE	Remote	Remote Control	I
70	PWM_LCD	LCD PWM	PWM for the LCD ?	I/O
71	GP Output // LCD_PWR_EN	GPO	GPO for LCD_power control	0
72	RESET_N	Reset	Master Reset	I

Pin	Pin name	Description	Comments / Alternate usage	Type
73	USBA_id	USBA identifier	USB Mini-receptacle Identifier between mini-A/mini-B plug	AI
74	USBA_vbus	USBA mini VBUS	USB power supply pin (5 volt). An off-chip charge pump is used to provide power to the VBUS pin.	AP
75	USBA_vdd12	USBA Digital 1.2V Power	Digital 1.2V power for USB-A	AP
76	USBA_vss12	USBA Digital Ground	Digital ground for USB-A	AP
77	USBA_vssa33t	USBA ground	Analog ground for USB-A transceiver	AP
78	USBA_dp	USBA D+	D+ analog signal from the USB cable	A
79	USBA_dm	USBA D-	D- analog signal from the USB cable	A
80	USBA_vdda33t	USBA 3.3V power	Analog 3.3V power for USB-A transceiver	AP
81	USBA_rext	USBA Ext Ref resistor	External resistor that controls the bias current for USB	AP
82	USBA_vdda33c	USBA 3.3V power	Analog 3.3V power for USB-A core	AP
83	USBA_vssa33c	USBA ground	Analog ground for USB-A core	AP
84	PLL_AVDD33	PLL VDD	PLL power	AP
85	PLL_AVSS33	PLL Ground	PLL ground	AP
86	PLLB_AVDD33	PLL VDD	PLL power	AP
87	PLLB_AVSS33	PLL Ground	PLL ground	AP
88	PLLA_AVDD33	PLL VDD	PLL power	AP
89	PLLA_AVSS33	PLL Ground	PLL ground	AP
90	OSCIN	OSC Input	27MHz crystal oscillator input	I
91	OSCOUT	OSC Output	27MHz crystal oscillator output	O
92	VDD12	Digital Core Power	Digital core 1.2V power	P
93	BUTTON1	BUTTON_1	BUTTON or GPIO or MISC	I/O
94	BUTTON2	BUTTON_2	BUTTON or GPIO or MISC	I/O
95	BUTTON3	BUTTON_3	BUTTON or GPIO or MISC	I/O
96	VDD33	VDD	Digital Power 3.3V	P
97	I2C_CLOCK	GPIO	GPIO	I/O
98	I2C_DATA	GPIO	GPIO	I/O
99	VSS	VSS	Digital Ground	P
100	XD_CE	Card Reader I/O	Card Reader I/F or GPIO	I/O
101	XD_RB	Card Reader I/O	Card Reader I/F or GPIO	I/O
102	XD_WP// SD_WP	Card Reader I/O	Card Reader I/F or GPIO	I/O
103	GPIO// CARD_POWER	Card Reader I/O	Card Reader I/F or GPIO	I/O
104	XD_RE	Card Reader I/O	Card Reader I/F or GPIO	I/O
105	XD_WE	Card Reader I/O	Card Reader I/F or GPIO	I/O
106	XD_RE	Card Reader I/O	Card Reader I/F or GPIO	I/O
107	XD_CE	Card Reader I/O	Card Reader I/F or GPIO	I/O
108	VDD33	Digital I/O Power	Digital I/O 3.3V power	P

Pin	Pin name	Description	Comments / Alternate usage	Type
109	GPIO	GPIO	General Purpose I/O or CARD_ENABLE	I/O
110	XD_D0	Card Reader I/O	Card Reader I/F or GPIO	I/O
111	XD_D1	Card Reader I/O	Card Reader I/F or GPIO	I/O
112	XD_D2 // SD_CMD	Card Reader I/O	Card Reader I/F or GPIO	I/O
113	XD_D3 // SD_CLK	Card Reader I/O	Card Reader I/F or GPIO	I/O
114	VSS	VSS	Digital Ground	P
115	XD_D4 // SD_D0	Card Reader I/O	Card Reader I/F or GPIO	I/O
116	XD_D5 // SD_D1	Card Reader I/O	Card Reader I/F or GPIO	I/O
117	XD_D6 // SD_D2	Card Reader I/O	Card Reader I/F or GPIO	I/O
118	VDD33	Digital I/O Power	Digital I/O 3.3V power	P
119	XD_D7 // SD_D3	Card Reader I/O	Card Reader I/F or GPIO	I/O
120	VDD12	VDD	Digital Power 1.2V	P
121	LCD_R0	LCD Video Out	LCD Video Signal Output	O
122	LCD_R1	LCD Video Out	LCD Video Signal Output	O
123	LCD_R2	LCD Video Out	LCD Video Signal Output	O
124	LCD_R3	LCD Video Out	LCD Video Signal Output	O
125	LCD_R4	LCD Video Out	LCD Video Signal Output	O
126	LCD_R5	LCD Video Out	LCD Video Signal Output	O
127	LCD_G0	LCD Video Out	LCD Video Signal Output	O
128	LCD_G1	LCD Video Out	LCD Video Signal Output	O
129	VSS	VSS	Digital Ground	P
130	LCD_G2	LCD Video Out	LCD Video Signal Output	O
131	LCD_G3	LCD Video Out	LCD Video Signal Output	O
132	LCD_G4	LCD Video Out	LCD Video Signal Output	O
133	LCD_G5	LCD Video Out	LCD Video Signal Output	O
134	VDD33	VDD	Digital Power 3.3V	P
135	LCD_B0	LCD Video Out	LCD Video Signal Output	O
136	LCD_B1	LCD Video Out	LCD Video Signal Output	O
137	LCD_B2	LCD Video Out	LCD Video Signal Output	O
138	LCD_B3	LCD Video Out	LCD Video Signal Output	O
139	LCD_B4	LCD Video Out	LCD Video Signal Output	O
140	LCD_B5	LCD Video Out	LCD Video Signal Output	O
141	JTAG_TMS// I2C_MASTER_CLOCK	JTAG TMS	JTAG	I/O
142	JTAG_TDI// I2C_MASTER_DATA	JTAG TDI	JTAG	I/O
143	JTAG_TCK// AUDIO_MUTE	JTAG TCK	JTAG	I/O
144	JTAG_TDO// OTG_VBUS	JTAG TDO	JTAG	I/O

### 5.1 Package pin-out diagram



## 5.1 Multiple function pins

Multiple usage pins are used to converse pin consumption for different features. The AML6210DP devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be a GPIO pin also.

The following tables illustrate the applications of the multiple usage pins.

### 5.1.1 Card Reader interface multi-function pins

PIN#	PACKAGE PIN NAME	XD	SD	MS	GPIO
100	XD_RE	XD_RE			AT_GPIO0
101	XD_WE	XD_WE			AT_GPIO1
102	XD_READY	XD_READY			AT_GPIO2
103	XD_CE	XD_CE			AT_GPIO3
104	XD_ALE	XD_ALE			AT_GPIO6
103	XD_CLE				AT_GPIO7
110	XD_D0	XD_D0			AT_GPIO8
111	XD_D1	XD_D1			AT_GPIO9
112	XD_D2	XD_D2	SD_CMD	MS_STB	AT_GPIO10
113	XD_D3	XD_D3	SD_CLK	MS_CLK	AT_GPIO11
115	XD_D4	XD_D4	SD_D0	MS_D0	AT_GPIO12
116	XD_D5	XD_D5	SD_D1	MS_D1	AT_GPIO13
117	XD_D6	XD_D6	SD_D2	MS_D2	AT_GPIO14
119	XD_D7	XD_D7	SD_D3	MS_D3	AT_GPIO15

### 5.1.2 TCON Multi-Function Pins

Pin#	Package Pin Name	LCD TCON	GPIO
5	TCON_STH2	TCON_STH2	LCD_GPIO_29
6	TCON_STH1	TCON_STH1	LCD_GPIO_28
7	TCON_OEV1	TCON_OEV1	LCD_GPIO_24
8	TCON_CPV1	TCON_CPV1	LCD_GPIO_25
10	TCON_STV1	TCON_STV1	LCD_GPIO_26
11	TCON_STV2	TCON_STV2	LCD_GPIO_27
13	TCON_VCOM	TCON_VCOM	LCD_GPIO_31
14	TCON_OEH	TCON_OEH	LCD_GPIO_30
15	TCON_CPH1	TCON_CPH1/2/3	LCD_GPIO_23

### 5.1.3 JTAG interface multi-function pins

Pin#	Package Pin Name	JTAG	MISC	GPIO
141	JTAG_TMS	JTAG_TMS	I2C_MSTR_CLK	JTAG_GPIO_1
142	JTAG_TDI	JTAG_TDI	I2C_MSTR_DATA	JTAG_GPIO_2
143	JTAG_TCK	JTAG_TCK	UART_RX	JTAG_GPIO_0

144	JTAG_TDO	JTAG_TDO	UART_TX	JTAG_GPIO_3
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### 5.1.4 FLASH and m1\_\* interface multi-function pins

Pin#	Package Pin Name	SDRAM Memory Interface Usage (16bits wide only)	NAND FLASH Usage (8-bits wide or 16-bits wide)	NOR FLASH Usage (8-bits wide, maximum of 8Mbytes)	MISC
111	NAND_WE_n		NAND_WE_n		EGPIO_8
112	NAND_RDYBSY		NAND_RDY_BSY		EGPIO_9
113	NAND_CE_n		NAND_CE_n	FLASH_CS_n	
114	NAND_RD_n		NAND_RD_n	FLASH_OE_n	
116	M1_A_3	M1_A_3		FLASH_A_3	
117	M1_A_2	M1_A_2		FLASH_A_2	
118	M1_A_1	M1_A_1		FLASH_A_1	
120	M1_A_0	M1_A_0		FLASH_A_0	
121	M1_A_4	M1_A_4		FLASH_A_4	
122	M1_A_5	M1_A_5		FLASH_A_5	
123	M1_A_6	M1_A_6		FLASH_A_6	
125	M1_A_7	M1_A_7		FLASH_A_7	
126	M1_A_8	M1_A_8		FLASH_A_8	
127	M1_A_9	M1_A_9		FLASH_A_9	
128	M1_A_10	M1_A_10		FLASH_A_10	
1	M1_A_11	M1_A_11		FLASH_A_11	
2	M1_BA1	M1_BA1			
3	M1_BA0	M1_BA0			
5	M1_CLKO	M1_CLKO			
6	M1_DQM1	M1_DQM1		FLASH_A_21	
7	M1_DQM0	M1_DQM0		FLASH_A_20	
8	M1_SCS0_n	M1_SCS0_n			
9	M1_RAS_n	M1_RAS_n		FLASH_A_22	
10	M1_CAS_n	M1_CAS_n			
11	M1_WE_n	M1_WE_n		FLASH_WE_n	
12	M1_D_8	M1_D_8	NAND_8	FLASH_A_12	
15	M1_D_9	M1_D_9	NAND_9	FLASH_A_13	
16	M1_D_10	M1_D_10	NAND_10	FLASH_A_14	
17	M1_D_11	M1_D_11	NAND_11	FLASH_A_15	
18	M1_D_12	M1_D_12	NAND_12	FLASH_A_16	
20	M1_D_13	M1_D_13	NAND_13	FLASH_A_17	
21	M1_D_14	M1_D_14	NAND_14	FLASH_A_18	
22	M1_D_15	M1_D_15	NAND_15	FLASH_A_19	
23	M1_D_7	M1_D_7	NAND_7	FLASH_D_7	
25	M1_D_6	M1_D_6	NAND_6	FLASH_D_6	
26	M1_D_5	M1_D_5	NAND_5	FLASH_D_5	
27	M1_D_4	M1_D_4	NAND_4	FLASH_D_4	
28	M1_D_3	M1_D_3	NAND_3	FLASH_D_3	
29	M1_D_2	M1_D_2	NAND_2	FLASH_D_2	
30	M1_D_1	M1_D_1	NAND_1	FLASH_D_1	

31	M1_D_0	M1_D_0	NAND_0	FLASH_D_0	
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## 6 Mechanical Specifications

The AML6210DP A/V processor is packaged using a 144 pins LQFP package. The mechanical dimensions are given in millimeters as below:

