Application Notes

AML8726-MX

TTL Display User Guide

Revision 0.2 Preliminary

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Table of Content

Revision History

Revision Number	Revised Date	By	Changes
0.1	April.10, 2012	Evoke Zhang	1st Draft Version
0.2	April.16, 2012	Evoke Zhang	Update TCON Signals description

1 General Description

Amlogic AML8726-MX is a highly integrated multimedia application processor SoC for Multimedia Internet Device (MID), tablet and Set Top Box (STB). It integrates a powerful CPU, a 2D/3D graphics subsystem and a state-of-the-art video decoding engine together with all major peripherals.

AML8726-MX integrates three LCD panel timing controllers: TTL, LVDS, and mLVDS. TTL should be used with TTL type LCD panel, LVDS is for LVDS type LCD panel, and mLVDS is for mini-LVDS type LCD panel.

This document is a user guide of AML8726-MX TTL interface for TTL LCD panel timing control only. This document describes:

- RGB data output
- TCON signals
- LCD Basic
- LCD Timing
- LCD Effect
- Android Driver
- Register address mapping
- Register description

2 RGB Data Output

AML8726-MX has 24 pins of TTL RGB data signals to output RGB888 data for supporting 8bits TTL LCD panel. All RGB data signals are connected to a series of GPIO pins via pin multiplex mapping circuit and listed in Table 1.

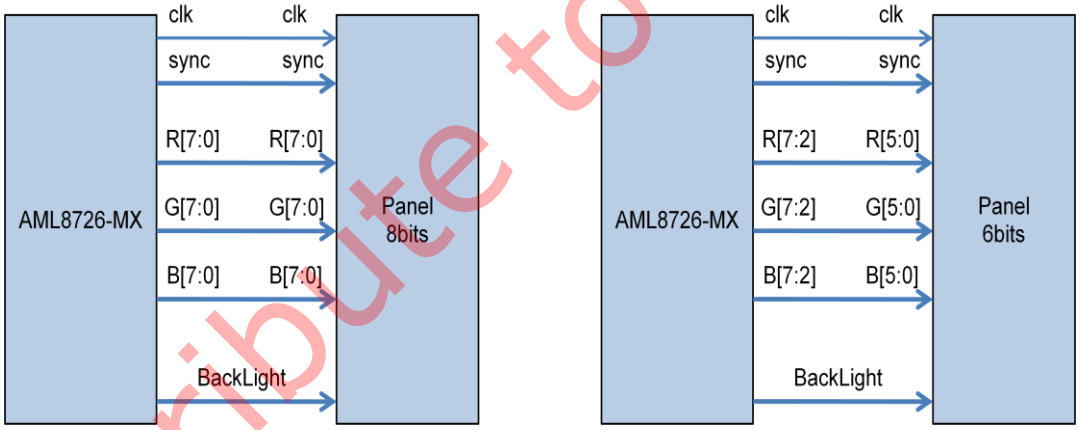
Table 5. RGB data signals Multiplexing Table

Pad Name	Signal Name	Pad Name	Signal Name	Pad Name	Signal Name
GPIOB_0	LCD_R0	GPIOB_8	LCD_G0	GPIOB_16	LCD_B0
GPIOB_1	LCD_R1	GPIOB_9	LCD_G1	GPIOB_17	LCD_B1
GPIOB_2	LCD_R2	GPIOB_10	LCD_G2	GPIOB_18	LCD_B2
GPIOB_3	LCD_R3	GPIOB_11	LCD_G3	GPIOB_19	LCD_B3
GPIOB_4	LCD_R4	GPIOB_12	LCD_G4	GPIOB_20	LCD_B4
GPIOB_5	LCD_R5	GPIOB_13	LCD_G5	GPIOB_21	LCD_B5
GPIOB_6	LCD_R6	GPIOB_14	LCD_G6	GPIOB_22	LCD_B6
GPIOB_7	LCD_R7	GPIOB_15	LCD_G7	GPIOB_23	LCD_B7

When required RGB666 data for a 6bits TTL panel, the RGB data signals must be connected bit[7:2] to panel. It will be display abnormal when connected wrong signals.

The RGB data connection for 8bits and 6bits panel is illustrated in Figure 1.

Figure 1. RGB Data Connection



3 LCD Panel Timing Controller(TCON)

AML8726-MX integrates a complex and flexible digital LCD panel timing controller(TCON) with TTL interface. Most of TTL interface signals are programmable and can be configured by software to meet the control signal timing requirements of various TTL LCD panels.

3.1TCON Signal Pinmux

AML8726-MX provides up to 9 digital timing control signals via build-in TCON function block to control TTL LCD panels. All signals are connected to a series of GPIO pins via pin multiplex mapping circuit and listed in Table 1. About GPIO function settings, please refer to AML8726-MX GPIO User Guide for detailed descriptions.

Table 1. TCON Signals Multiplexing Table

Pad Name	Signal Name	Default Signal Type	Pinmux
GPIOD_2	TCON_STH1	Line signal	reg1[19]
GPIOD_3	TCON_STV1	Frame signal	reg1[18]
GPIOD_4	TCON_OEH	Line signal	reg1[17]
GPIOD_5	TCON_CPV1	Line signal	reg1[16]
GPIOD_6	TCON_OEV1	Line signal	reg1[15]
GPIOD_7	TCON_CPH1	Clock signal	reg1[14]
	TCON_CPH2	Clock signal	reg1[13]
	TCON_CPH3	Clock signal	reg1[12]
GPIOD_8	TCON_VCOM	Line signal	reg1[20]

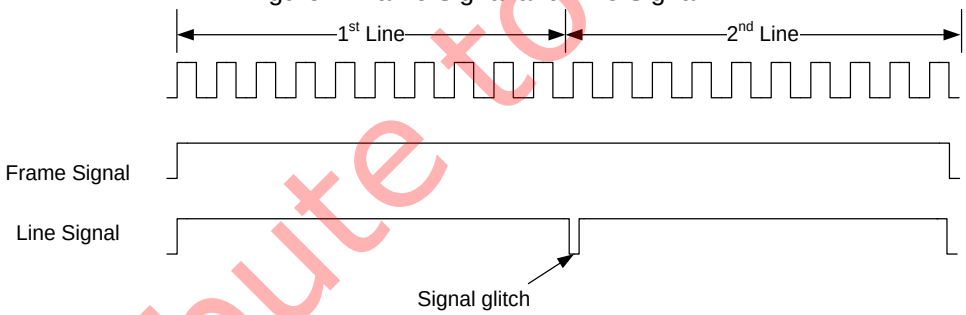
3.2Frame Signal and Line Signal

Two types of TCON signals are defined in AML8726-MX: frame signal and line signal. The difference of these two signals is that an 'Enable' of frame signal, which is typically HIGH, can cross lines in one frame but line signal cannot. For convenience, only the typical case will be described in the following sections.

For example a line signal is set to HIGH. When it crosses the line, the signal will be output LOW and then output HIGH again from the beginning of next line. This will introduce a glitch between two lines.

The example signals are illustrated in Figure .

Figure 2.Frame Signal and Line Signal



Most of TCON signals can be configured as line signal or frame signal by setting TCON_MISC_ADDR register. These signals are:

- STH1
- OEH
- VCOM
- CPV1
- STV1
- OEV1

3.3TCON Signal Timing Control

All TCON signals' timing is configurable and based on TCON master clock or CPH1 signal. For most TCON signals, there are four registers to control each signal's timing:

- Horizontal Start pixel position register (HS)
- Horizontal End pixel position register (HE)
- Vertical Start line position register (VS)
- Vertical End line position register (VE)

All register names and associated signal names are listed in Table 2.

Table 2. TCON Signal Timing Registers

TCON Signal	Horizontal Start Pixel Position Register Name	Horizontal End Pixel Position Register Name	Vertical Start Pixel Position Register Name	Vertical End Pixel Position Register Name
STH1	STH1_HS_ADDR	STH1_HE_ADDR	STH1_VS_ADDR	STH1_VE_ADDR
OEH	OEH_HS_ADDR	OEH_HE_ADDR	OEH_VS_ADDR	OEH_VS_ADDR
VCOM	VCOM_HSWITCH_ADDR		VCOM_VS_ADDR	VCOM_VE_ADDR
CPV1	CPV1_HS_ADDR	CPV1_HE_ADDR	CPV1_VS_ADDR	CPV1_VE_ADDR
STV1	STV1_HS_ADDR	STV1_HE_ADDR	STV1_VS_ADDR	STV1_VE_ADDR
OEV1	OEV1_HS_ADDR	OEV1_HE_ADDR	OEV1_VS_ADDR	OEV1_VE_ADDR

Note: Each register has 12 effective bits and valid value from 0 to 4095.

HS register defines the position of first pixel that the signal is needed to be ACTIVE. HE register defines the position of last pixel that the signal is needed to be ACTIVE. After that pixel, the signal is Inactive. The pixel number is counted from 0.

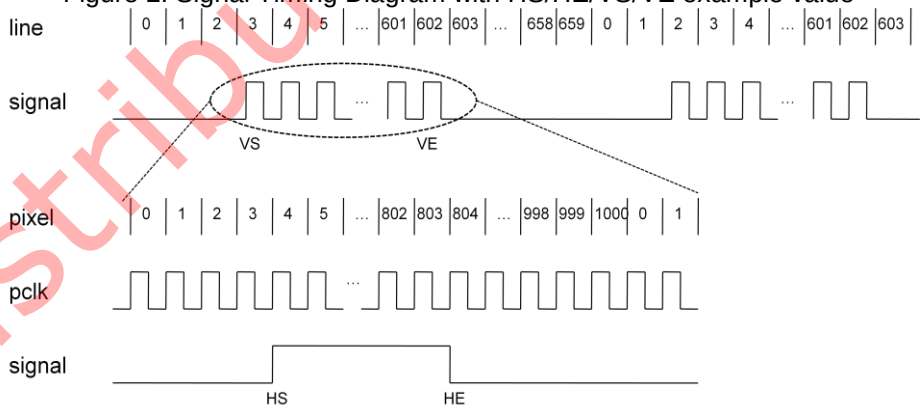
For example:
- The line has 1000 scan pixels and 800 valid pixels.
- The horizontal starting position is 4th pixel.
- The HS register should be set to 4 representing the 4th pixel.
- The HE register should be set to 4+800=804, representing the ACTIVE time of signal is 800 pixels.

VS register defines the position of first line in a frame that the signal is needed to be ACTIVE according to HS and HE registers. And VE register is used to define the position of last line. The line number is counted from 0.

For example:
- A frame has 660 scan lines and 600 valid lines.
- The vertical starting position is 3rd line.
- The VS register should be set to 3 representing the 3rd line.
- The VE register should be set to 3+600-1=602, representing the ACTIVE time of signal is 600 lines.

The timing diagram of signal with HS/HE/VS/VE example values is illustrated in Figure .

Figure 2. Signal Timing Diagram with HS/HE/VS/VE example value



4 LCD Basic

4.1Display Area Definition

The display area are grids of pixels that can be divided into horizontal and vertical. They are illustrated in

VIDEO_ON_PIXEL define internal image data horizontal starting position, VIDEO_ON_LINE define internal image data vertical starting position, they are both decided to AML8726-MX internal hardware, and can not be modified.

4.2Panel Aspect Ratio

Set the right value of Panel Aspect Ratio to ensure the length-to-width ratio of OSD display.

This value is controlled by the members of lcd_basic struct named screen_ratio_width and screen_ratio_height, the quotient of screen_ratio_width dividing screen_ratio_height must match panel active area's width-height ratio.
For example:

- panel active area is 154.08(W)*85.92(H)(unit: mm)
- panel active area's width-height ratio is 1.79, approach to 16:9, so we can set as below:
  . screen_ratio_width = 16,
  . screen_ratio_height = 9,

4.3Panel Interface

The Panel Interface information also must be set in lcd_basic struct, the example is as below:

.lcd_type = LCD_DIGITAL_TTL,
.lcd_bits = 8, //8 or 6

5 LCD Timing

5.1Pixel Clock Calculate

AML8726-MX uses five parameters to set panel pixel clock, such as M, N, OD, div and XD. They are contained in the members named pll_ctrl, div_ctrl and clk_ctrl of lcd_timing struct. The parameters are illustrated in Table 2.

Table 4. pixel clock parameter

Item	Symbol	Range
pll_ctrl[8:0]	M	750M<(M*24/N)<1500M
pll_ctrl[13:9]	N	1~4
pll_ctrl[17:16]	OD	0~2
div_ctrl[7:4]	div	0~5
clk_ctrl[3:0]	XD	1~15

The pixel clock(clk) calculates with below formula:

clk = M*XTAL/(N*2^{OD}*(div+1)*XD) //generally speaking, XTAL=24M

For example:

- .pll_ctrl=0x10221,
  .div_ctrl=0x18803,
  .clk_ctrl=0x111e,
- Then M=33, N=1, OD=1, div=0, XD=14.
- clk=33*24/(1*2*1*14)=28.3MHz.

Pixel clock can be real-time changed by editing the registers HHI_VIID_PLL_CNTL, HHI_VIID_CLK_DIV, HHI_VIID_DIVIDER_CNTL. For details please see the registers description in Chapter 9.

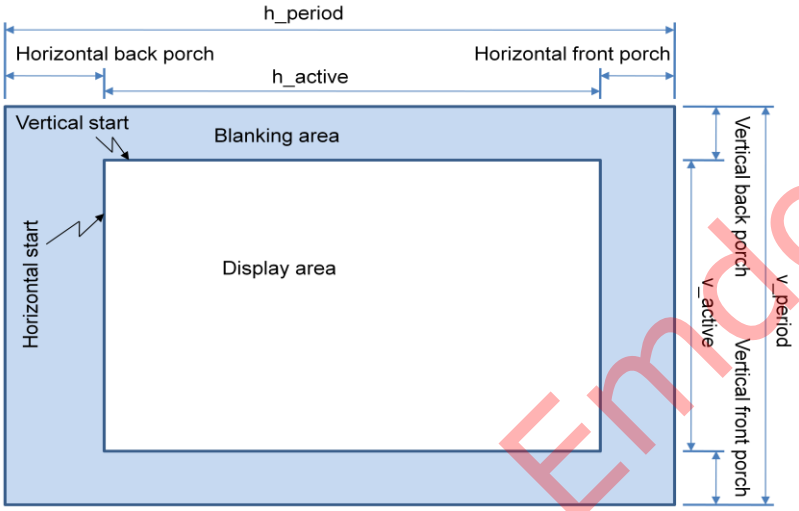
5.2Pixel Clock Spread Spectrum

The clock spread spectrum function is controlled by parameter ss_level, which is assigned to clk_ctrl[19:16] of lcd_timing struct. The range of ss_level is 0~5, means clock spread spectrum width. The example is as below:

.clk_ctrl=0x3111e, //ss_level=3, the clock spread spetrum width is 3%.

.

Figure 3. Display Area



For example:

- A TTL panel's timing are defined as below in Table 3: (These timing are available in panel specification.)

Table 3. Timing

Item	Value	Unit	Related Parameter of AML8726-MX	TCON Signal
Horizontal Display Area	800	pixel	h_active	Hsync (low active)
HS period time	1056	pixel	h_period	
HS pulse width	10	pixel		
HS back porch	70	pixel	Horizontal back porch	
Vertical display area	480	line	v_active	Vsync (low active)
VS period time	535	line	v_period	
VS pulse width	4	line		
VS back porch	20	line	Vertical back porch	

- The display parameter need to set as below:

```
#define  H_ACTIVE          800
#define  V_ACTIVE          480
#define  H_PERIOD          1056
#define  V_PERIOD          525
#define  VIDEO_ON_PIXEL    48
#define  VIDEO_ON_LINE     22
```

H_ACTIVE and V_ACTIVE define the area that real image displays, H_PERIOD and V_PERIOD define horizontal and vertical total timing, they are applied to calculate line frequence and frame rate.

VIDEO_ON_PIXEL define internal image data horizontal starting position, VIDEO_ON_LINE define internal image data vertical starting position, they are both decided to AML8726-MX internal hardware, and can not be modified.

5.3Panel Aspect Ratio

Set the right value of Panel Aspect Ratio to ensure the length-to-width ratio of OSD display.

This value is controlled by the members of lcd_basic struct named screen_ratio_width and screen_ratio_height, the quotient of screen_ratio_width dividing screen_ratio_height must match panel active area's width-height ratio.
For example:

- panel active area is 154.08(W)*85.92(H)(unit: mm)
- panel active area's width-height ratio is 1.79, approach to 16:9, so we can set as below:
  . screen_ratio_width = 16,
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The Panel Interface information also must be set in lcd_basic struct, the example is as below:

.lcd_type = LCD_DIGITAL_TTL,
.lcd_bits = 8, //8 or 6

6 LCD Timing

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pll_ctrl[17:16]	OD	0~2
div_ctrl[7:4]	div	0~5
clk_ctrl[3:0]	XD	1~15

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Pixel clock can be real-time changed by editing the registers HHI_VIID_PLL_CNTL, HHI_VIID_CLK_DIV, HHI_VIID_DIVIDER_CNTL. For details please see the registers description in Chapter 9.

6.2Pixel Clock Spread Spectrum

The clock spread spectrum function is controlled by parameter ss_level, which is assigned to clk_ctrl[19:16] of lcd_timing struct. The range of ss_level is 0~5, means clock spread spectrum width. The example is as below:

.clk_ctrl=0x3111e, //ss_level=3, the clock spread spetrum width is 3%.

6.3TCON Signal Definition

AML8726-MX displays the image with horizontal starting at 67 pixels, vertical starting at 22 lines. they are according to display parameter VDIEO_ON_PIXEL and VIDEO_ON_LINE setting, and can not be modified. TTL panel generally has three synchronization signals to control display, such as Hsync, Vsync and DE. The signals are illustrated in
VIDEO_ON_PIXEL define internal image data horizontal starting position, VIDEO_ON_LINE define internal image data vertical starting position, they are both decided to AML8726-MX internal hardware, and can not be modified.

6.4Panel Aspect Ratio

Set the right value of Panel Aspect Ratio to ensure the length-to-width ratio of OSD display.

This value is controlled by the members of lcd_basic struct named screen_ratio_width and screen_ratio_height, the quotient of screen_ratio_width dividing screen_ratio_height must match panel active area's width-height ratio.
For example:

- panel active area is 154.08(W)*85.92(H)(unit: mm)
- panel active area's width-height ratio is 1.79, approach to 16:9, so we can set as below:
  . screen_ratio_width = 16,
  . screen_ratio_height = 9,

6.5Panel Interface

The Panel Interface information also must be set in lcd_basic struct, the example is as below:

.lcd_type = LCD_DIGITAL_TTL,
.lcd_bits = 8, //8 or 6

7 LCD Timing

7.1Pixel Clock Calculate

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pll_ctrl[13:9]	N	1~4
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clk_ctrl[3:0]	XD	1~15

The pixel clock(clk) calculates with below formula:

clk = M*XTAL/(N*2^{OD}*(div+1)*XD) //generally speaking, XTAL=24M

For example:

- .pll_ctrl=0x10221,
  .div_ctrl=0x18803,
  .clk_ctrl=0x111e,
- Then M=33, N=1, OD=1, div=0, XD=14.
- clk=33*24/(1*2*1*14)=28.3MHz.

Pixel clock can be real-time changed by editing the registers HHI_VIID_PLL_CNTL, HHI_VIID_CLK_DIV, HHI_VIID_DIVIDER_CNTL. For details please see the registers description in Chapter 9.

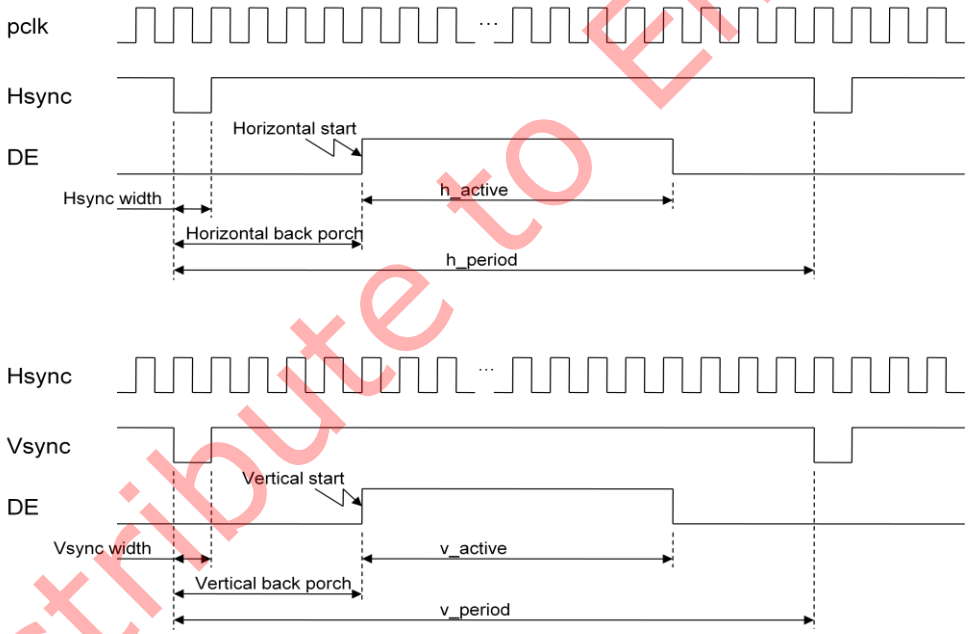
7.2Pixel Clock Spread Spectrum

The clock spread spectrum function is controlled by parameter ss_level, which is assigned to clk_ctrl[19:16] of lcd_timing struct. The range of ss_level is 0~5, means clock spread spectrum width. The example is as below:

.clk_ctrl=0x3111e, //ss_level=3, the clock spread spetrum width is 3%.

.

Figure 4. TCON Signals



For example:

- We still use the timing defined in Table 3.
- The synchronization signals are assigned to AML8726_MX TCON signal in circuit as follow:
  Hsync – sth1, Vsync – stv1, DE – oeh.

- The display parameters need to set as below:

```
.sth1_hs_addr = 20,          //67-70+10    //horizontal start- horizontal_back_porch+hs_pulse_width
                             //if hs<0, hs=hs+H_PERIOD-1
.sth1_he_addr = 10,          //67-70       //horizontal start- horizontal_back_porch
                             //if he<0, he=hs+H_PERIOD-1=67-70+1056-1
.sth1_vs_addr = 0,                       //fixed value
.sth1_ve_addr = V_PERIOD-1,              //fixed value
.oeh_hs_addr = 67,                       //fixed value
.oeh_he_addr = 67+ H_ACTIVE,             //fixed value
```

```
.oeh_vs_addr = VIDEO_ON_LINE,                    //fixed value
.oeh_ve_addr = VIDEO_ON_LINE+V_ACTIVE-1,         //fixed value
.stv1_hs_addr = 0,                               //fixed value
.stv1_he_addr = H_PERIOD-1,                      //fixed value
.stv1_vs_addr = 5,          //22-20+4-1   //vertical start-vertical_back_porch+vs_pulse_width-1
                            //if vs<0, vs=vs+V_PERIOD-1
.stv1_ve_addr = 2,          //22-20       //vertical start-vertical_back_porch
                            //if ve<0, ve=ve+V_PERIOD-1
```

The TCON signals can be changed by editing the TCON registers real-time. For details please see the registers description in Chapter 9.

7.3Pixel Clock and CPH1/2/3 Signal

CPH1 is the main clock signal of pixel clock. All other TCON signals timing is aligned or based on it. In order to support some LCD panels which need different clock phase, two additional main clock signals, CPH2 and CPH3, are provided. CPH1/2/3 can be configured polarity to positive or negative edge to latch data.

CPH1/2/3 signals polarity are setting in the member of lcd_timing struct named pol_cntl_addr as below.(set 1 to configured positive edge)

.pol_cntl_addr = (0x1 << LCD_CPH1_POL) |(0x0 << LCD_CPH2_POL) | (0x0 << LCD_CPH3_POL),

CPH1/2/3 signals phase can be changed by editing the register POL_CNTL_ADDR real-time. For details please see the registers description in Chapter 9.

7.4RGB Swap

AML8726-MX support both swapping R/B data channel and swapping RGB MSB/LSB data for special application.

The member of lcd_timing struct named dual_port_cntl_addr controls the swapping as below.(set 1 to enable swapping)

.dual_port_cntl_addr = (0<<RGB_SWAP) | (0<<BIT_SWAP),

RGB swap can be changed by editing the register DUAL_PORT_CNTL_ADDR real-time. For details please see the registers description in Chapter 9.

8 LCD Effect

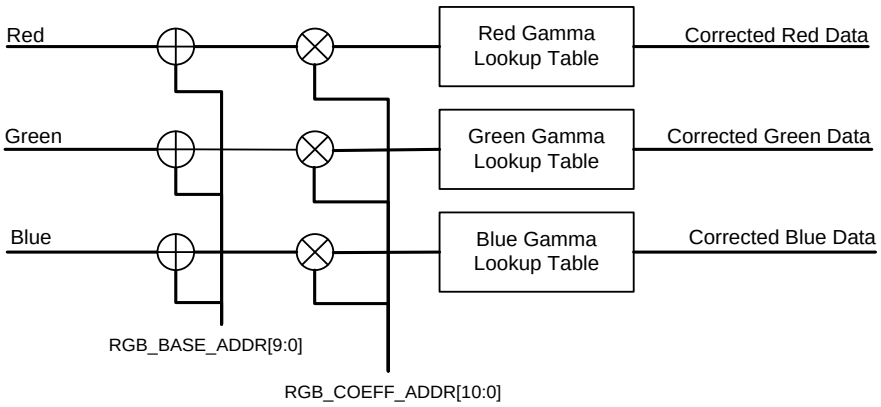
AML8726-MX integrates a build-in data correction engine to compensate nonlinear LCD panel display characteristics and improve the display quality.

All data correction is processed in RGB color gamut only. Each pixel RGB data in processing is 10 bit for each color channel comparing to the 8-bit output to panel.

The data correction process includes three steps:
1. Base shifting
2. Co-effective factor correction
3. Gamma lookup table correction

The data correction data processing is illustrated in Figure .

Figure 5. RGB Data Correction Process



8.1Base Shifting

Base shifting is the first step of gamma correction to correct the luminance of the image. Each pixel RGB data will add the value of the base shifting value in RGB_BASE_ADDR[9:0].

Please notice:

1. The effective values of RGB_BASE_ADDR[9:0] are from -512 to +511.
2. The values of RGB_BASE_ADDR[9:0] will be used for all RGB channels at the same time.

8.2Co-effective factor correction

Co-effective factor correction is the second step to do linear gamma correction of the image. Each pixel RGB data will multiply the value of co-effective factor in RGB_COEFF_ADDR[10:0].

Please notice:

1. The effective value of RGB_COEFF_ADDR[10:0] is from 0 to 1.999023.
2. The value of RGB_COEFF_ADDR[10:0] will be used for all RGB channels at the same time.

8.3Gamma lookup table correction

Gamma lookup table correction is the last step to do non-linear gamma correction based on color mapping using lookup table.

AML8726-MX integrates 768 10-bit registers to store gamma lookup table used by step 3 of gamma correction. The registers are divided into 3 blocks. Each block has 256 10-bit registers to store one color channel gamma lookup table values:

- Red lookup table registers (R_LUT)
- Green lookup table registers (G_LUT)
- Blue lookup table registers (B_LUT)

The gamma table is set as below.

```
static void t13_setup_gama_table(tcon_conf_t *pConf)
{
    int i;
    const unsigned short gamma_adjust[256] = {
        0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,
        32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,
        …… 248,249,250,251,252,253,254,255
    };

    for (i=0; i<256; i++) {
        pConf->GammaTableR[i] = gamma_adjust[i] << 2;
        pConf->GammaTableG[i] = gamma_adjust[i] << 2;
        pConf->GammaTableB[i] = gamma_adjust[i] << 2;
```

```
    }
}
```

Gamma correction is controlled by the member of panel parameter named gamma_cntl_port.(set 1 to enable gamma correction)

.gamma_cntl_port = (1 << LCD_GAMMA_EN),

gamma correction can be enabled/disabled by editing the register GAMMA_CNTL_PORT real-time. For details please see the registers description in Chapter 9.

9 Android Driver

9.1Uboot Driver

Amlogic provides Panel Parameter files for uboot. In Amlogic reference code, the directory is

```
[uboot root]/board/amlogic/[board directory]/
```

It recommends that software creates a single C type source code file for each panel.

9.2Kernel Driver

Amlogic provides Panel Parameter files for Kernel. In Amlogic reference code, the directory is

```
[kernel root]/customer/boards/
```

It recommends that software creates a single C type source code file for each panel.

10 Register Address Mapping

10.1 Register address mapping

The register addresses in this document are provided as address offset. Address mapping is needed to convert register address offset to the physical register address.

The basic formula of address mapping is:

REG_ADDR = BASE_ADDR + (REG_OFFSET << 2)

where:
REG_ADDR: physical register address that software can access the register
BASE_ADDR: the base address of the address bus
REG_OFFSET: the register address offset

The value of base address (BASE_ADDR) may be different in different software implementation. In Amlogic ported Linux kernel and the boot loader uBoot, the base addresses are:

Linux Kernel: 0xF1100000
uboot: 0xC1100000

Software needs to choose BASE_ADDR according implementation environment.

10.2 Register operation for serial debugging

The register can be read or write for serial debugging.

uboot:	read:	md REG_ADDR
	write:	mw REG_ADDR REG_VAL
Linux Kernel:	read:	echo “REG_OFFSET” > /sys/class/i2c/cbus_reg
	write:	echo “w REG_OFFSET REG_VAL” > /sys/class/i2c/cbus_reg

11 Register Descriptions

11.1 Video Clock

Table 5. HHI_VIID_CLK_DIV Register Definition

Name HHI_VIID_PLL_CNTL **Offset** 0x1047 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:18	-	-	-	Reserved
17:16	OD	R/W	0	Video clock parameter OD, see Chapter 5.1 for detail.
15:14	-	-	-	Reserved
13:9	N	R/W	0	Video clock parameter N, see Chapter 5.1 for detail.
8:0	M	R/W	0	Video clock parameter M, see Chapter 5.1 for detail.

Table 6. HHI_VIID_CLK_DIV Register Definition

Name HHI_VIID_CLK_DIV **Offset** 0x104a **Width** 32-bit

Bit	Name	R/W	Default	Description
31:8	-	-	0	Reserved
7:0	XD0	R/W	0	Video clock parameter XD-1, see Chapter 5.1 for detail.

Table 7. HHI_VIID_DIVIDER_CNTL Register Definition

Name HHI_VIID_DIVIDER_CNTL **Offset** 0x104c **Width** 32-bit

Bit	Name	R/W	Default	Description
31:7	-	-	-	Reserved
6:4	PRE_SEL	R/W	0	Video clock parameter div, see Chapter 5.1 for detail.
3:0	-	-	-	Reserved

Table 8. POL_CNTL_ADDR Register Definition

Name POL_CNTL_ADDR **Offset** 0x1487 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:9	-	-	0	Reserved
8	CPH3_POL	R/W	0	CPH3 Polarity Control 0: Active HIGH 1: Active LOW
7	CPH2_POL	R/W	0	CPH2 Polarity Control 0: Active HIGH 1: Active LOW
6	CPH1_POL	R/W	0	CPH1 Polarity Control 0: Active HIGH 1: Active LOW
5:0	-	-	0	Reserved

11.2 TCON Signal

Table 9.STH1_HS_ADDR Register Definition

Name	STH1_HS_ADDR	Offset	0x1490	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STH1_HS_ADDR	R/W	0	STH1 signal horizontal start pixel position.

Table 10.STH1_HE_ADDR Register Definition

Name	STH1_HE_ADDR	Offset	0x1491	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STH1_HE_ADDR	R/W	0	STH1 signal horizontal end pixel position.

Table 11.STH1_VS_ADDR Register Definition

Name	STH1_VS_ADDR	Offset	0x1492	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STH1_VS_ADDR	R/W	0	STH1 signal vertical start pixel position

Table 12.STH1_VE_ADDR Register Definition

Name	STH1_VE_ADDR	Offset	0x1493	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STH1_VE_ADDR	R/W	0	STH1 signal vertical end pixel position.

Table 3.OEH_HS_ADDR Register Definition

Name	OEH_HS_ADDR	Offset	0x1498	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEH_HS_ADDR	R/W	0	OEH signal horizontal start pixel position.

Table 4.OEH_HE_ADDR Register Definition

Name	OEH_HE_ADDR	Offset	0x1499	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEH_HE_ADDR	R/W	0	OEH signal horizontal end pixel position.

Table 5.OEH_VS_ADDR Register Definition

Name	OEH_VS_ADDR	Offset	0x149A	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEH_VS_ADDR	R/W	0	OEH signal vertical start pixel position

Table 6.OEH_VE_ADDR Register Definition

Name	OEH_VE_ADDR	Offset	0x149B	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEH_VE_ADDR	R/W	0	OEH signal vertical end pixel position.

Table 7.VCOM_HSWITCH_ADDR Register Definition

Name	VCOM_HSWITCH_ADDR	Offset	0x149C	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	VCOM_HSWITCH_ADDR	R/W	0	VCOM signal horizontal switch pixel position

Table 18.VCOM_VS_ADDR Register Definition

Name	VCOM_VS_ADDR	Offset	0x149D	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	VCOM_VS_ADDR	R/W	0	VCOM signal vertical start pixel position

Table 19.VCOM_VE_ADDR Register Definition

Name	VCOM_VE_ADDR	Offset	0x149E	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	VCOM_VE_ADDR	R/W	0	VCOM signal vertical end pixel position

Table 20.CPV1_HS_ADDR Register Definition

Name	CPV1_HS_ADDR	Offset	0x149F	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	CPV1_HS_ADDR	R/W	0	CPV1 signal horizontal start pixel position

Table 21.CPV1_HE_ADDR Register Definition

Name	CPV1_HE_ADDR	Offset	0x14A0	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	CPV1_HE_ADDR	R/W	0	CPV1 signal horizontal end pixel position

Table 22.CPV1_VS_ADDR Register Definition

Name	CPV1_VS_ADDR	Offset	0x14A1	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	CPV1_VS_ADDR	R/W	0	CPV1 signal vertical start pixel position

Table 8.CPV1_VE_ADDR Register Definition

Name	CPV1_VE_ADDR	Offset	0x14A2	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	CPV1_VE_ADDR	R/W	0	CPV1 signal vertical end pixel position

Table 9.STV1_HS_ADDR Register Definition

Name	STV1_HS_ADDR	Offset	0x14A7	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STV1_HS_ADDR	R/W	0	STV1 signal horizontal start pixel position

Table 10.STV1_HE_ADDR Register Definition

Name	STV1_HE_ADDR	Offset	0x14A8	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STV1_HE_ADDR	R/W	0	STV1 signal horizontal end pixel position

Table 11.STV1_VS_ADDR Register Definition

Name	STV1_VS_ADDR	Offset	0x14A9	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STV1_VS_ADDR	R/W	0	STV1 signal vertical start pixel position

Table 12.STV1_VE_ADDR Register Definition

Name	STV1_VE_ADDR	Offset	0x14AA	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	STV1_VE_ADDR	R/W	0	STV1 signal vertical end pixel position

Table 28.OEV1_HS_ADDR Register Definition

Name	OEV1_HS_ADDR	Offset	0x14AF	Width	32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEV1_HS_ADDR	R/W	0	OEV1 signal horizontal start pixel position

Table 29.OEV1_HE_ADDR Register Definition

Name OEV1_HE_ADDR **Offset** 0x14B0 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEV1_HE_ADDR	R/W	0	OEV1 signal horizontal end pixel position

Table 30.OEV1_VS_ADDR Register Definition

Name OEV1_VS_ADDR **Offset** 0x14B1 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEV1_VS_ADDR	R/W	0	OEV1 signal vertical start pixel position

Table 31.OEV1_VE_ADDR Register Definition

Name OEV1_VE_ADDR **Offset** 0x14B2 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11:0	OEV1_VE_ADDR	R/W	0	OEV1 signal vertical end pixel position

Table 32.TCON_MISC_ADDR Register Definition

Name TCON_MISC_ADDR **Offset** 0x14C1 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:12	-	-	-	Reserved
11	STH1_SEL	R/W	0	0: STH1 is line signal 1: STH1 is frame signal
10	OEH_SEL	R/W	0	0: OEH is line signal 1: OEH is frame signal
9	VCOM_SEL	R/W	0	0: VCOM is line signal 1: VCOM is frame signal
8:7	-	-	0	Reserved
6	CPV1_SEL	R/W	0	0: CPV1 is line signal 1: CPV1 is frame signal
5	-	-	1	Reserved
4	STV1_SEL	R/W	1	0: STV1 is line signal 1: STV1 is frame signal
3:1	-	-	-	Reserved
0	OEV1_SEL	R/W	0	0: OEV1 is line signal 1: OEV1 is frame signal

Table 13.DUAL_PORT_CNTL_ADDR Register Definition

Name DUAL_PORT_CNTL_ADDR **Offset** 0x14C2 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:2	-	-	-	Reserved
1	RGB_SWP	R/W	0	Setting this bit to 1 swaps Red and Blue color output in data path.
0	BIT_SWP	R/W	0	Setting this bit to 1 swaps the bit order in data path from 7:0 to 0:7.

11.3 RGB Data Effect

Table 34. GAMMA_CNTL_PORT Register Definition

Name GAMMA_CNTL_PORT **Offset** 0x1480 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:1	-	-	-	Reserved
0	GAMMA_EN	R/W	0	Gamma correction enable 0: disable gamma correction 1: enable gamma correction

Table 35. RGB_BASE_ADDR Register Definition

Name RGB_BASE_ADDR **Offset** 0x1485 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:10	-	-	-	Reserved
9:0	RGB_BASE_ADDR	R/W	0	Gamma correction base shifting value

Table 36. RGB_COEFF_ADDR Register Definition

Name RGB_COEFF_ADDR **Offset** 0x1486 **Width** 32-bit

Bit	Name	R/W	Default	Description
31:11	-	-	-	Reserved
10:0	RGB_COEFF_ADDR	R/W	0	Gamma correction coefficient value