AML8726-MX

Quick Reference Manual

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Amlogic, Inc.

REVISION HISTORY

Revision Number	Revision Date	Changes
0.9	2011/12/28	Initial draft

CONTACT INFORMATION

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Contents

1. General Description

AML8726-MX is an advanced connected multimedia processor designed for Tablet/MID, Set Top Box (STB) and high-end media player applications. It integrates powerful CPU/GPU, and a state-of-the-art video decoding engine with all major peripherals to form the ultimate low power multimedia SoC.

The integrated processor is dual core ARM Cortex-A9 CPU with 32KB L1 instruction and 32KB data cache for each core and a large 512KB L2 unified cache to improve system performance. In addition, the Cortex-A9 CPU includes the NEON SIMD co-processor to improve software media processing capability. The dual core ARM Cortex-A9 CPU can run up to 1.5GHz and has a wide bus connecting to the memory sub-system.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The Dual core ARM Mali-400 GPU handles all the OpenGL ES 1.1/2.0 and OpenVG graphics programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. The video output pipeline can perform advanced image correction and enhancements. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks.

Three additional processors offload the Cortex-A9 CPU by handling all audio and video decoding processing – the MediaCPU and two MediaDSPs with a dedicated hardware video decoders. The MediaCPU is audio optimized and handles all audio decoding tasks. The dual MediaDSPs with hardware decoder can decode all HD video formats including H.264, MVC, MPEG-1/2/4, VC-1/WMV, AVS, RealVideo and MJPEG streams. The video decoding engine is also capable of decoding JPEG pictures with no size limitation.

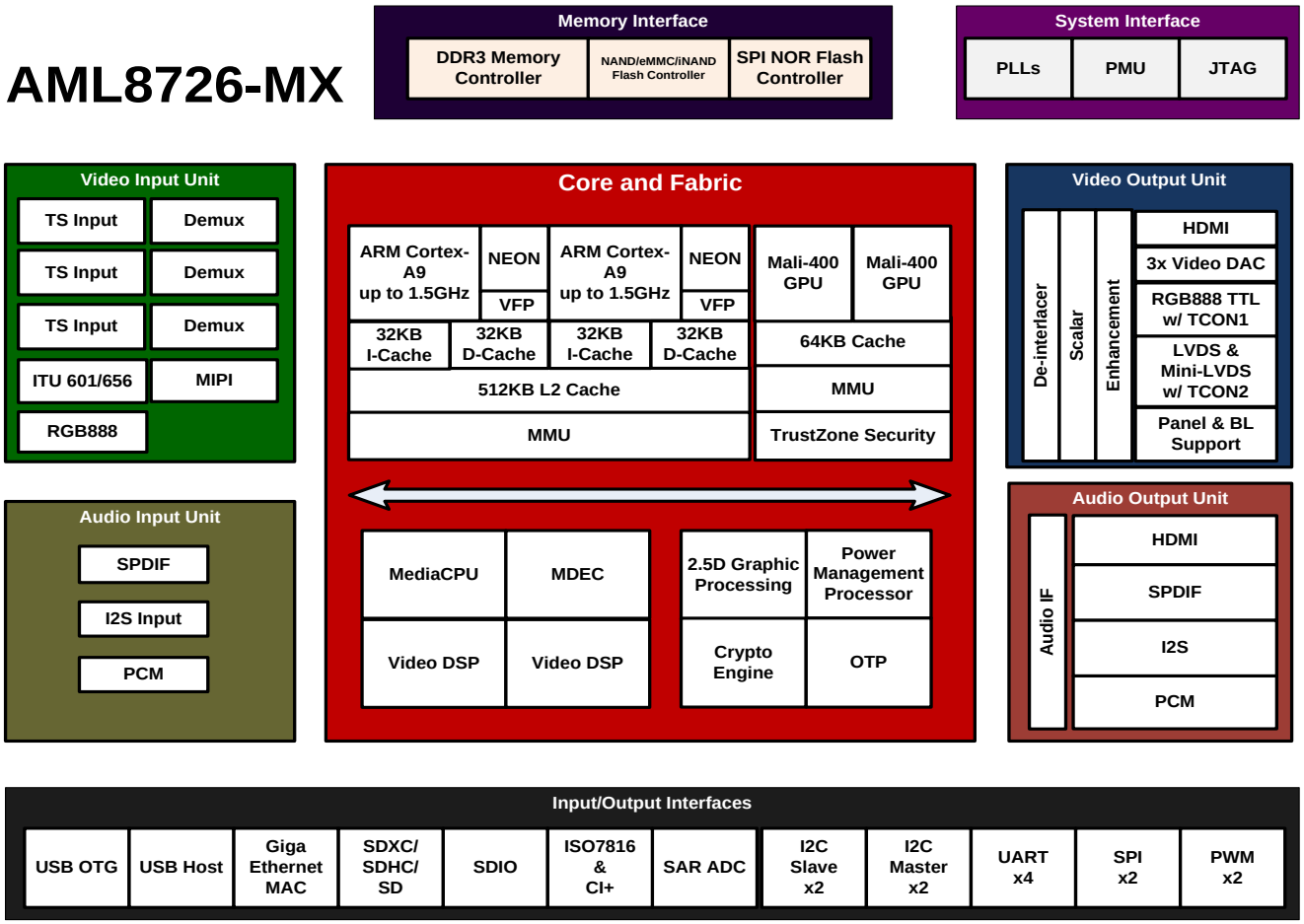
AML8726-MX integrates complete audio/video input/output interfaces including LVDS/mini-LVDS panel interface with TCON, RGB888 TTL panel interface with TCON, an HDMI1.4a transmitter with 3D support, CEC and PHY, three video DAC supporting composites, CVBS, YPbPr and VGA outputs, I2S and SPDIF digital audio input/output interfaces, a PCM audio interface, a MIPI and a ITU601/656 camera input interfaces.

AML8726-MX integrates a set of functional blocks for digital TV broadcasting streams. The build-in three demux can process the TV streams from three transport stream input interfaces, which can connect to tuner/demodulator. An ISO7816 smart card interface and a crypto-processor build in to help handling encrypted traffic and media streams.

The processor has rich advanced network and peripheral interfaces, including a Gigabit Ethernet MAC with RMII/RGMII interface, dual USB 2.0 high-speed ports (one OTG and one HOST), two SDIOs with multi-standard memory card controller, four UART interfaces, four I2C interfaces, two high-speed SPI interfaces and two PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

2. Features Summary



CPU Sub-system

- Dual core ARM Cortex-A9 CPU up to 1.5GHz frequency and 7500DMIPS
- ARMv7 instruction set, multi-issue superscalar, out-of-order architecture
- 32KB instruction cache and 32KB data cache
- 512KB Unified L2 cache
- Advanced NEON and VFP co-processor
- Memory Management Unit
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3D Graphics Processing Unit

- Unified 64KB cache to reduce graphic data bandwidth
- 800Mpix/sec and 40Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- Supports AES block cipher with 128/192/256 bits keys, standard 16 bytes block size and streaming
- Supports DES/3DES block cipher with Electronic Code Book (ECB) and Cipher Block Chaining (CBC) operation mode
- Supports standard 64 bits key for DES and 192 bits key for 3DES
- Support streaming decoder with standard 64 bits block size
- Build-in LSFR Random number generator

Video/Picture Decoder

- Dual programmable DSP engines at 200MHz with DSP instructions
- Dedicated hardware video decoder
- H.264 HP@L4.1 up to 1080P, MVC at 30Hz
- MPEG-4 Part 2 ASP up to 1080P (ISO-14496-2)
- WMV/VC-1 SP/MP/AP up to 1080P
- AVS JiZhun Profile up to 1080P
- MPEG-2 MP/HL up to 1080P (ISO-13818)
- MPEG-1 MP/HL up to 1080P (ISO-11172)
- RealVideo 8/9/10 up to 720P
- WebM up to VGA
- Multiple language and multiple format sub-title video support
- Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4, *.rm and *.jpg file formats
- MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
- Supports JPEG thumbnail, scaling, rotation and transition effects

Video Post-Processing Controller

- Motive adaptive 3D noise reduction filter
- Advanced motion adaptive edge enhancing de-interlacing engine
- 3:2 pull-down support
- Programmable poly-phase scalar for both horizontal and vertical dimension for zoom and windowing
- Programmable color management filter (to enhance blue, green, red, face and other colors)
- Chroma coring and black extension processing
- Dynamic Non-Linear Luma filter
- Programmable color matrix pipeline
- Video mixer: 2 video planes and 2 graphics planes

Digital LCD Panel Output

- TTL, LVDS and mini-LVDS panel supporting
- Single port LVDS/mini-LVDS with TCON supporting both single and dual-gate panels up to 1366x768 resolution
- RGB888 TTL interface with TCON supporting digital panel up to 1920x1200 resolution
- LED BL PWM and VGHL PWM build-in
- Three independent Gamma table for LCD panel tuning
- Dithering logic for mapping to different LCD panel color depth

Video Output

- Build-in HDMI 1.4a transmitter with CEC, both controller and PHY
- Programmable 3 channels high speed video DACs for analog video output including CVBS, S-Video, YPbPr and VGA
- Supports all standard SD/HD video output formats: 480i/p, 576i/p, 720p and 1080i/p
- Supports dual video output with combination of LCD+HDMI, TTL+LVDS or CVBS+HDMI
- Supports 3D LCD panel and 3D HDMI display

Audio Decoder and Input/Output

- MediaCPU with DSP audio processing
- Supports MP3, AAC, WMA, RM, FLAC, Ogg and programmable with 7.1 down-mixing
- I2S , SPDIF/IEC958 and PCM serial digital audio output
- Supports concurrent dual audio stereo channel output with combination of I2S+PCM

Other Digital Audio/Video Input/Output Interfaces

- ITU 601/656 parallel video input with down-scalar
- MIPI camera interface with 4 lanes and 1GHz per lane
- Supports camera input as YUV422, RGB565, 10bit rawRGB ,16bit RGB or JPEG

Memory and Storage Interface

- Supports DDR3-1066 SDRAM with 32-bit data bus
- Supports up to 2GB DDR3/DDR3L/DDR3U/LPDDR2 memory
- TrustZone protected DRAM memory region and internal SRAM
- Supports SLC/MLC/TLC NAND Flash with 4 chip enable pins with BCH60
- Supports serial NOR Flash via SPI interface
- Build-in 4kbits One-Time-Programming ROM for key storage
- SDIO with memory card controller with 8-bit data bus supporting SD/SDHC/SDXC/MMC/MS/MS-Pro memory cards

Network

- Integrated IEEE 802.3 10/100/1000 Gigabit Ethernet controller with RMII/RGMII interface.
- Supports Energy Efficiency Ethernet (EEE) mode
- Optional 50MHz and 125MHz clock output to Ethernet PHY
- WiFi/IEEE802.11 supporting via SDIO/USB

Digital Television Interface

- Three transport stream(TS) input interfaces with three build-in demux processor for connecting to external digital TV tuner/demodulator and one output TS interface
- Build-in PWM, I2C and SPI interfaces to control tuner and demodulator
- CI+ PCMCIA controller and interface
- Integrated ISO 7816 smart card controller

Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- Four UART Interfaces with RTS/CTS
- Two I2C master interfaces and two I2C slave interfaces
- Two high speed bi-directional SPI interfaces
- Dual PWM channels with feedback control logic
- Programmable IR remote controller
- Build-in 10bit SAR ADC with 8 input channels with resistive touch panel controller
- A set of General Purpose IO interfaces

System, Peripherals and Misc. Interfaces

- Multiple power domains
- Dedicated always-on (AO) power domain to communicate with external PMIC
- Integrated general purpose timers, counters, DMA controllers
- Integrated RTC with battery backup option
- Single 24 MHz crystal oscillator input
- Embedded debug interface using ICE/JTAG
- AMPOWER power management circuits supporting multiple sleep and suspend operating modes
- Optional encrypted secure boot

Software

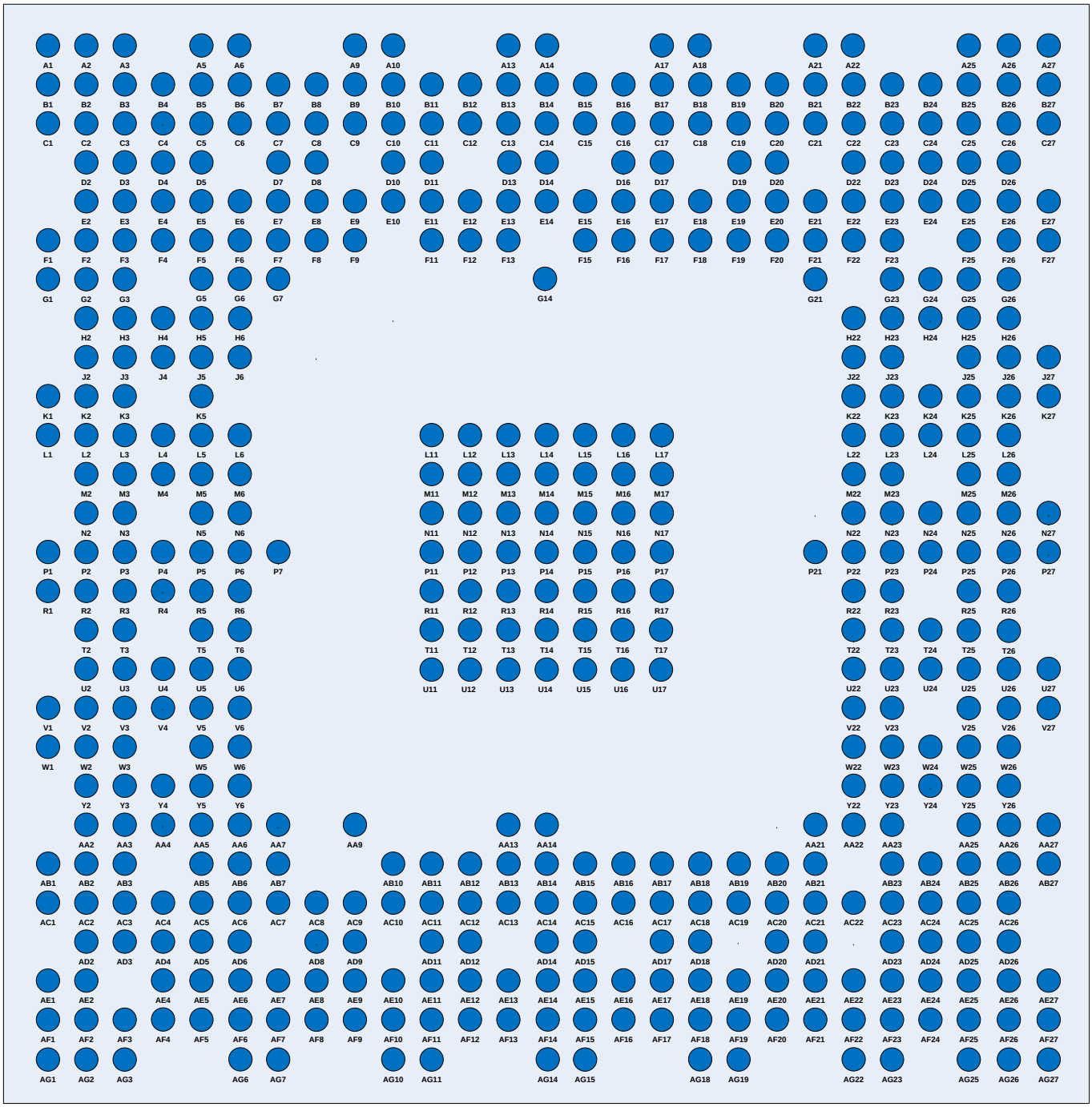
- Supports Android and Linux operating systems
- GNU/GCC Android tools chain

Package

- 487-ball LFBGA, RoHS compliant

3. Pin Out Specification

3.1 Pin-Out Diagram (top view)



3.2 Pin Assignments

The AML8726-MX A/V processor pin assignment is described in the following table.

Table 1. Pin Name assignments

BGA Ball	Pin Name	Group	Pull-up/down	Description	Type
B2	GPIOX_0	GPIOX	PU	General purpose input/output bank X signal 0. Please refer to following Table5 for functional multiplex information.	I/O
B1	GPIOX_1	GPIOX	PU	General purpose input/output bank X signal 1. Please refer to following Table5 for functional multiplex information.	I/O
D4	GPIOX_2	GPIOX	PU	General purpose input/output bank X signal 2. Please refer to following Table5 for functional multiplex information.	I/O
C1	GPIOX_3	GPIOX	PU	General purpose input/output bank X signal 3. Please refer to following Table5 for functional multiplex information.	I/O
C2	GPIOX_4	GPIOX	PU	General purpose input/output bank X signal 4. Please refer to following Table5 for functional multiplex information.	I/O
D3	GPIOX_5	GPIOX	PU	General purpose input/output bank X signal 5. Please refer to following Table5 for functional multiplex information.	I/O
D2	GPIOX_6	GPIOX	PU	General purpose input/output bank X signal 6. Please refer to following Table5 for functional multiplex information.	I/O
E3	GPIOX_7	GPIOX	PU	General purpose input/output bank X signal 7. Please refer to following Table5 for functional multiplex information.	I/O
E2	GPIOX_8	GPIOX	PU	General purpose input/output bank X signal 8. Please refer to following Table5 for functional multiplex information.	I/O
E4	GPIOX_9	GPIOX	PU	General purpose input/output bank X signal 9. Please refer to following Table5 for functional multiplex information.	I/O
F4	GPIOX_10	GPIOX	PU	General purpose input/output bank X signal 10. Please refer to following Table5 for functional multiplex information.	I/O
F5	GPIOX_11	GPIOX	PU	General purpose input/output bank X signal 11. Please refer to following Table5 for functional multiplex information.	I/O
G5	GPIOX_12	GPIOX	PU	General purpose input/output bank X signal 12. Please refer to following Table5 for functional multiplex information.	I/O
G6	GPIOX_13	GPIOX	PU	General purpose input/output bank X signal 13. Please refer to following Table5 for functional multiplex information.	I/O
F3	GPIOX_14	GPIOX	PU	General purpose input/output bank X signal 14. Please refer to following Table5 for functional multiplex information.	I/O
F2	GPIOX_15	GPIOX	PU	General purpose input/output bank X signal 15. Please refer to following Table5 for functional multiplex information.	I/O
F1	GPIOX_16	GPIOX	PU	General purpose input/output bank X signal 16. Please refer to following Table5 for functional multiplex information.	I/O
G3	GPIOX_17	GPIOX	PU	General purpose input/output bank X signal 17. Please refer to following Table5 for functional multiplex information.	I/O
G1	GPIOX_18	GPIOX	PU	General purpose input/output bank X signal 18. Please refer to following Table5 for functional multiplex information.	I/O
G2	GPIOX_19	GPIOX	PU	General purpose input/output bank X signal 19. Please refer to following Table5 for functional multiplex information.	I/O
H5	GPIOX_20	GPIOX	PU	General purpose input/output bank X signal 20. Please refer to following Table5 for functional multiplex information.	I/O
H4	GPIOX_21	GPIOX	PU	General purpose input/output bank X signal 21. Please refer to following Table5 for functional multiplex information.	I/O
H3	GPIOX_22	GPIOX	PU	General purpose input/output bank X signal 22. Please refer to following Table5 for functional multiplex information.	I/O
H2	GPIOX_23	GPIOX	PU	General purpose input/output bank X signal 23. Please refer to following Table5 for functional multiplex information.	I/O
J5	GPIOX_24	GPIOX	PU	General purpose input/output bank X signal 24. Please refer to following Table5 for functional multiplex information.	I/O
J4	GPIOX_25	GPIOX	PU	General purpose input/output bank X signal 25. Please refer to following Table5 for functional multiplex information.	I/O
J3	GPIOX_26	GPIOX	PU	General purpose input/output bank X signal 26. Please refer to following Table5 for functional multiplex information.	I/O
J2	GPIOX_27	GPIOX	PU	General purpose input/output bank X signal 27. Please refer to following Table5 for functional multiplex information.	I/O
K5	GPIOX_28	GPIOX	PU	General purpose input/output bank X signal 28. Please refer to following Table5 for functional multiplex information.	I/O
K3	GPIOX_29	GPIOX	PU	General purpose input/output bank X signal 29. Please refer to following Table5 for functional multiplex information.	I/O

K2	GPIOX_30	GPIOX	PU	General purpose input/output bank X signal 30. Please refer to following Table5 for functional multiplex information.	I/O
K1	GPIOX_31	GPIOX	PU	General purpose input/output bank X signal 31. Please refer to following Table5 for functional multiplex information.	I/O
L5	GPIOX_32	GPIOX	PU	General purpose input/output bank X signal 32. Please refer to following Table5 for functional multiplex information.	I/O
L4	GPIOX_33	GPIOX	PU	General purpose input/output bank X signal 33. Please refer to following Table5 for functional multiplex information.	I/O
M4	GPIOX_34	GPIOX	PU	General purpose input/output bank X signal 34. Please refer to following Table5 for functional multiplex information.	I/O
M5	GPIOX_35	GPIOX	PU	General purpose input/output bank X signal 35. Please refer to following Table5 for functional multiplex information.	I/O
L3	GPIOY_0	GPIOY	PU	General purpose input/output bank Y signal 0. Please refer to following Table6 for functional multiplex information.	I/O
L1	GPIOY_1	GPIOY	PU	General purpose input/output bank Y signal 1. Please refer to following Table6 for functional multiplex information.	I/O
L2	GPIOY_2	GPIOY	PU	General purpose input/output bank Y signal 2. Please refer to following Table6 for functional multiplex information.	I/O
M3	GPIOY_3	GPIOY	PU	General purpose input/output bank Y signal 3. Please refer to following Table6 for functional multiplex information.	I/O
M2	GPIOY_4	GPIOY	PU	General purpose input/output bank Y signal 4. Please refer to following Table6 for functional multiplex information.	I/O
N3	GPIOY_5	GPIOY	PU	General purpose input/output bank Y signal 5. Please refer to following Table6 for functional multiplex information.	I/O
N2	GPIOY_6	GPIOY	PU	General purpose input/output bank Y signal 6. Please refer to following Table6 for functional multiplex information.	I/O
P3	GPIOY_7	GPIOY	PU	General purpose input/output bank Y signal 7. Please refer to following Table6 for functional multiplex information.	I/O
N5	GPIOY_8	GPIOY	PU	General purpose input/output bank Y signal 8. Please refer to following Table6 for functional multiplex information.	I/O
P2	GPIOY_9	GPIOY	PU	General purpose input/output bank Y signal 9. Please refer to following Table6 for functional multiplex information.	I/O
P1	GPIOY_10	GPIOY	PU	General purpose input/output bank Y signal 10. Please refer to following Table6 for functional multiplex information.	I/O
R3	GPIOY_11	GPIOY	PU	General purpose input/output bank Y signal 11. Please refer to following Table6 for functional multiplex information.	I/O
R1	GPIOY_12	GPIOY	PU	General purpose input/output bank Y signal 12. Please refer to following Table6 for functional multiplex information.	I/O
P6	GPIOY_13	GPIOY	PU	General purpose input/output bank Y signal 13. Please refer to following Table6 for functional multiplex information.	I/O
P5	GPIOY_14	GPIOY	PU	General purpose input/output bank Y signal 14. Please refer to following Table6 for functional multiplex information.	I/O
R5	GPIOY_15	GPIOY	PU	General purpose input/output bank Y signal 15. Please refer to following Table6 for functional multiplex information.	I/O
R2	CARD_0	SDIO	PU	Card reader multiplexing pin 0. Please refer to following Table9 for functional multiplex information.	I/O
R4	CARD_1	SDIO	PU	Card reader multiplexing pin 1. Please refer to following Table9 for functional multiplex information.	I/O
T5	CARD_2	SDIO	PU	Card reader multiplexing pin 2. Please refer to following Table9 for functional multiplex information.	I/O
T3	CARD_3	SDIO	PU	Card reader multiplexing pin 3. Please refer to following Table9 for functional multiplex information.	I/O
T2	CARD_4	SDIO	PU	Card reader multiplexing pin 4. Please refer to following Table9 for functional multiplex information.	I/O
U5	CARD_5	SDIO	PU	Card reader multiplexing pin 5. Please refer to following Table9 for functional multiplex information.	I/O
U4	CARD_6	SDIO	PU	Card reader multiplexing pin 6. Please refer to following Table9 for functional multiplex information.	I/O
U3	CARD_7	SDIO	PU	Card reader multiplexing pin 7. Please refer to following Table9 for functional multiplex information	I/O
U2	CARD_8	SDIO	PU	Card reader multiplexing pin 8. Please refer to following Table9 for functional multiplex information.	I/O
V6	AVDD25_DPLL	Power		Analog power supply 2.5V for Digital PLL	AP
V5	DPLL_LDO_EXTCAP	DPLL		External capacitor connection for digital PLL	AIO
V4	AVSS25_DPLL	Power		Analog power ground for Digital PLL	AP

Y5	AVSS25_LVDS	Power		Analog power ground for LVDS	AP
V3	LVDS_5N	LVDS		miniLVDS/LVDS data5 negative output	AO
W6	AVDD25_LVDS	Power		Analog power supply 2.5V for LVDS	AP
V2	LVDS_5P	LVDS		miniLVDS/LVDS data5 positive output	AO
W5	AVDD25_LVDS	Power		Analog power supply 2.5V for LVDS	AP
V1	LVDS_4N	LVDS		miniLVDS/LVDS data4 negative output	AO
AC3	VSS	Power		Power ground	P
W1	LVDS_4P	LVDS		miniLVDS/LVDS data4 positive output	AO
Y4	AVSS25_LVDS	LVDS		Analog power ground for LVDS	AP
W2	LVDS_3N	LVDS		miniLVDS/LVDS data3 negative output	AO
Y3	LVDS_3P	LVDS		miniLVDS/LVDS data3 positive output	AO
Y2	MINILVDS_CKN	LVDS		miniLVDS Clock negative output (Note: not LVDS Clock)	AO
AA3	MINILVDS_CKP	LVDS		miniLVDS Clock positive output (Note: not LVDS Clock)	AO
AA2	LVDS_2N	LVDS		miniLVDS/LVDS data2 negative output	AO
AB3	LVDS_2P	LVDS		miniLVDS/LVDS data2 positive output	AO
AB2	LVDS_1N	LVDS		miniLVDS/LVDS data1 negative output	AO
AB1	LVDS_1P	LVDS		miniLVDS/LVDS data1 positive output	AO
AC1	LVDS_0N	LVDS		miniLVDS/LVDS data 0 negative output	AO
AC2	LVDS_0P	LVDS		miniLVDS LVDS data 0 positive output	AO
W3	LVDS_REXT_600	LVDS		LVDS port compensative resister output pin	AIO
Y6	AVSS25_HDPLL	Power		Analog power ground	AP
AA5	AVDD25_HDPLL	Power		Analog power supply 2.5V	P
AA6	AVDD25_HDMI	Power		Analog power supply 2.5V for HDMI	AP
AA4	HDMIREXT_600	HDMI		LVDS port compensative resister output pin	AIO
AC5	AVSS25_HDMI	Power		Analog power ground for HDMI	AP
AD3	HDMITX_CKN	HDMI		HDMI TMDS clock- signal	AO
AD2	HDMITX_CKP	HDMI		HDMI TMDS clock+ signal	AO
AC4	AVDD33_HDMI	HDMI		Analog power supply 3.3V for HDMI	AP
AE1	HDMITX_0N	HDMI		HDMI TMDS data0-	AO
AE2	HDMITX_0P	HDMI		HDMI TMDS data0+	AO
U17	VSS	Power		Power ground	P
AF1	HDMITX_1N	HDMI		HDMI TMDS data1-	AO
AG1	HDMITX_1P	HDMI		HDMI TMDS data1+	AO
AB5	AVDD33_HDMI	HDMI		Analog power supply 3.3V for HDMI	AP
AF2	HDMITX_2N	HDMI		HDMI TMDS data2-	AO
AG2	HDMITX_2P	HDMI		HDMI TMDS data2+	AO
AB6	AVSS25_HDMI	Power		Analog power supply 2.5V for HDMI	AP
AE4	GPIOC_7	GPIOC	PD	General purpose input/output bank C signal 7. Please refer to following Table3 for functional multiplex information.	I/O
AF4	GPIOC_8	GPIOC	PD	General purpose input/output bank C signal 8. Please refer to following Table3 for functional multiplex information.	I/O
AD4	GPIOC_9	GPIOC	PD	General purpose input/output bank C signal 9. Please refer to following Table3 for functional multiplex information.	I/O
AE5	GPIOC_10	GPIOC	Z	General purpose input/output bank C signal 10. Please refer to following Table3 for functional multiplex information.	I/O
AF5	GPIOC_11	GPIOC	Z	General purpose input/output bank C signal 11. Please refer to following Table3 for functional multiplex information.	I/O
AE6	GPIOC_12	GPIOC	Z	General purpose input/output bank C signal 12. Please refer to following Table3 for functional multiplex information.	I/O
AF6	GPIOC_13	GPIOC	Z	General purpose input/output bank C signal 13. Please refer to following Table3 for functional multiplex information.	I/O
AD5	GPIOC_14	GPIOC	Z	General purpose input/output bank C signal 14. Please refer to following Table3 for functional multiplex information.	I/O
AG6	GPIOC_15	GPIOC	Z	General purpose input/output bank C signal 15. Please refer to following Table3 for functional multiplex information.	I/O
AG3	SYS_OSCIN	System		24MHz crystal oscillator input	AI

AF3	SYS_OSCOUT	System		24MHz crystal oscillator output	AO
AC6	DQ4	DDR		DDR3 SDRAM data Bus bit 4	I/O
AD6	DQ6	DDR		DDR3 SDRAM data Bus bit 6	I/O
AC7	DQ2	DDR		DDR3 SDRAM data Bus bit 2	I/O
AC8	DQ0	DDR		DDR3 SDRAM data Bus bit 0	I/O
AC9	DM0	DDR		DDR3 SDRAM data mask 0	O
AD8	DQS0	DDR		DDR3 SDRAM data Strobe 0	I/O
AD9	DQS0_n	DDR		DDR3 SDRAM Data Strobe Complementary 0	I/O
AD11	DQ5	DDR		DDR3 SDRAM data Bus bit 5	I/O
AC10	DQ7	DDR		DDR3 SDRAM data Bus bit 7	I/O
AC11	DQ3	DDR		DDR3 SDRAM data Bus bit 3	I/O
AC12	DQ1	DDR		DDR3 SDRAM data Bus bit 1	I/O
AC19	VREF1	DDR		DDR3 SDRAM reference voltage	AP
AF7	DQ11	DDR		DDR3 SDRAM data Bus bit 11	I/O
AE7	DQ9	DDR		DDR3 SDRAM data Bus bit 9	I/O
AG7	DQ13	DDR		DDR3 SDRAM data Bus bit 13	I/O
AF10	DM1	DDR		DDR3 SDRAM data mask 1	O
AE8	DQ15	DDR		DDR3 SDRAM data Bus bit 15	I/O
AE9	DQS1	DDR		DDR3 SDRAM data Strobe 1	I/O
AF9	DQS1_n	DDR		DDR3 SDRAM Data Strobe Complementary 1	I/O
AE11	DQ12	DDR		DDR3 SDRAM data Bus bit 2	I/O
AE10	DQ14	DDR		DDR3 SDRAM data Bus bit 2	I/O
AG10	DQ10	DDR		DDR3 SDRAM data Bus bit 2	I/O
AG11	DQ8	DDR		DDR3 SDRAM data Bus bit 2	I/O
AB12	PZQ	DDR		Reference pin for ZQ calibration	A
AF11	CK	DDR		DDR3 SDRAM Port A clock output	O
AE12	CK_N	DDR		DDR3 SDRAM Port A clock output complementary	O
AC13	RAS_N	DDR		Row Address Strobe	O
AB14	ODT1	DDR		On-die termination 1	O
AD14	ODT0	DDR		On-die termination 0	O
AC14	CAS_N	DDR		Column Address Strobe	O
AB15	CS1_N	DDR		DDR3 SDRAM port B chip select output 1	O
AD15	WE_n	DDR		Write Enable	O
AC16	BA2	DDR		DDR3 SDRAM bank address 2	O
AF13	A2	DDR		DDR3 SDRAM address bus bit 2	O
AF14	A9	DDR		DDR3 SDRAM address bus bit 9	O
AG14	A7	DDR		DDR3 SDRAM address bus bit 7	O
AE15	A13	DDR		DDR3 SDRAM address bus bit 13	O
AE14	A5	DDR		DDR3 SDRAM address bus bit 5	O
AF12	A0	DDR		DDR3 SDRAM address Bus bit 0	O
AB16	VDDQ_AO	DDR		DDR3 IO power supply for DDR retention pins (Always On)	P
AD18	CKE0	DDR		DDR3 SDRAM clock enable output 0	O
AC18	VREF0	DDR		DDR3 SDRAM reference voltage	AP
AB17	VDDQ	DDR		DDR3 IO power supply	P
AB13	CKE1	DDR		DDR3 SDRAM clock enable output 1	O
AE13	A3	DDR		DDR3 SDRAM address bus bit 3	O
AC17	BA0	DDR		DDR3 SDRAM bank address 0	O
AC15	CS0_N	DDR		DDR3 SDRAM port B chip select output 0	O
AE19	A8	DDR		DDR3 SDRAM address bus bit 8	O
AF18	A14	DDR		DDR3 SDRAM address bus bit 14	O
AG18	A6	DDR		DDR3 SDRAM address bus bit 6	O
AE18	A11	DDR		DDR3 SDRAM address bus bit 11	O
AE17	A1	DDR		DDR3 SDRAM address bus bit 1	O

AF17	A4	DDR		DDR3 SDRAM address bus bit 4	O
AE16	A12	DDR		DDR3 SDRAM address bus bit 12	O
AF16	BA1	DDR		DDR3 SDRAM bank address 1	O
AF15	A15	DDR		DDR3 SDRAM address bus bit 15	O
AG15	A10	DDR		DDR3 SDRAM address bus bit 10	O
AE24	CK1	DDR		DDR3 SDRAM Port B clock output	O
AF24	CK1_N	DDR		DDR3 SDRAM Port B clock output 1 complementary	O
AC20	DQ20	DDR		DDR3 SDRAM data bus bit 20	I/O
AD20	DQ22	DDR		DDR3 SDRAM data bus bit 22	I/O
AD21	DQ18	DDR		DDR3 SDRAM data bus bit 18	I/O
AC21	DQ16	DDR		DDR3 SDRAM data bus bit 16	I/O
AC23	DM2	DDR		DDR3 SDRAM data mask 2	O
AC22	DQS2	DDR		DDR3 SDRAM data strobe 2	I/O
AD23	DQS2_N	DDR		DDR3 SDRAM data strobe 2 complementary	I/O
AB24	DQ21	DDR		DDR3 SDRAM data bus bit 21	I/O
AC24	DQ23	DDR		DDR3 SDRAM data bus bit 23	I/O
AB23	DQ19	DDR		DDR3 SDRAM data bus bit 19	I/O
AA23	DQ17	DDR		DDR3 SDRAM data bus bit 17	I/O
AF19	DQ27	DDR		DDR3 SDRAM data bus bit 27	I/O
AF20	DQ25	DDR		DDR3 SDRAM data bus bit 25	I/O
AE20	DQ29	DDR		DDR3 SDRAM data bus bit 29	I/O
AE22	DM3	DDR		DDR3 SDRAM data mask 3	O
AG19	DQ31	DDR		DDR3 SDRAM data bus bit 31	I/O
AE21	DQS3	DDR		DDR3 SDRAM data strobe 3	I/O
AF21	DQS3_N	DDR		DDR3 SDRAM data strobe 3 complementary	I/O
AF22	DQ28	DDR		DDR3 SDRAM data bus bit 28	I/O
AG23	DQ30	DDR		DDR3 SDRAM data bus bit 30	I/O
AF23	DQ26	DDR		DDR3 SDRAM data bus bit 26	I/O
AE23	DQ24	DDR		DDR3 SDRAM data bus bit 24	I/O
AG25	RTC_GPO	RTC		RTC timer controlled output	OD
AE25	RTC_VBAT	RTC		RTC battery power supply input	AP
AF26	RTC_AVSS	RTC		RTC analog power ground	AP
AG26	RTC_XIN	RTC		RTC 32K crystal input	AI
AG27	RTC_XOUT	RTC		RTC 32K crystal output	AO
AF25	GPIOAO_0	GPIOAO	PU	General purpose input/output bank AO signal 0. Please refer to following Table8 for functional multiplex information.	I/O
AF27	GPIOAO_1	GPIOAO	PU	General purpose input/output bank AO signal 1. Please refer to following Table8 for functional multiplex information.	I/O
AD24	GPIOAO_2	GPIOAO	Z	General purpose input/output bank AO signal 2. Please refer to following Table8 for functional multiplex information.	I/O
AE27	VDD_IO_AO	Power		Power supply for IO	P
AE26	GPIOAO_3	GPIOAO	Z	General purpose input/output bank AO signal 3. Please refer to following Table8 for functional multiplex information.	I/O
AD25	GPIOAO_4	GPIOAO	PU	General purpose input/output bank AO signal 4. Please refer to following Table8 for functional multiplex information.	I/O
AD26	GPIOAO_5	GPIOAO	PU	General purpose input/output bank AO signal 5. Please refer to following Table8 for functional multiplex information.	I/O
AC25	VDD_AO	Power		Power supply for always-on domain	P
AC26	GPIOAO_6	GPIOAO	Z	General purpose input/output bank AO signal 6. Please refer to following Table8 for functional multiplex information.	I/O
AB25	GPIOAO_7	GPIOAO	Z	General purpose input/output bank AO signal 7. Please refer to following Table8 for functional multiplex information.	I/O
AB26	GPIOAO_8	GPIOAO	PU	General purpose input/output bank AO signal 8. Please refer to following Table8 for functional multiplex information.	I/O
AB27	GPIOAO_9	GPIOAO	PU	General purpose input/output bank AO signal 9. Please refer to following Table8 for functional multiplex information.	I/O

AA25	GPIOAO_10	GPIOAO	PU	General purpose input/output bank AO signal 10. Please refer to following Table8 for functional multiplex information.	I/O
AA26	GPIOAO_11	GPIOAO	PU	General purpose input/output bank AO signal 11. Please refer to following Table8 for functional multiplex information.	I/O
Y22	TEST_N	System	PU	Reserved	I
AA27	RESET_N	System	PD	Master reset input	I
W22	BSD_EN	System	PD	Boundary Scan Enable signal. Should be type low during normal operation.	I
Y25	BOOT_0	NAND	PU	Boot device multiplexing pin 0. Please refer to following Table10 for functional multiplex information.	I/O
Y26	BOOT_1	NAND	PU	Boot device multiplexing pin 1. Please refer to following Table10 for functional multiplex information.	I/O
W25	BOOT_2	NAND	PU	Boot device multiplexing pin 2. Please refer to following Table10 for functional multiplex information.	I/O
W26	BOOT_3	NAND	PU	Boot device multiplexing pin 3. Please refer to following Table10 for functional multiplex information.	I/O
V25	BOOT_4	NAND	PU	Boot device multiplexing pin 4. Please refer to following Table10 for functional multiplex information.	I/O
V26	BOOT_5	NAND	PU	Boot device multiplexing pin 5. Please refer to following Table10 for functional multiplex information.	I/O
V27	BOOT_6	NAND	PU	Boot device multiplexing pin 6. Please refer to following Table10 for functional multiplex information.	I/O
U25	BOOT_7	NAND	PU	Boot device multiplexing pin 7. Please refer to following Table10 for functional multiplex information.	I/O
Y24	BOOT_8	NAND	PU	Boot device multiplexing pin 8. Please refer to following Table10 for functional multiplex information.	I/O
W24	BOOT_9	NAND	PU	Boot device multiplexing pin 9. Please refer to following Table10 for functional multiplex information.	I/O
W23	BOOT_10	NAND	PU	Boot device multiplexing pin 10. Please refer to following Table10 for functional multiplex information.	I/O
V23	BOOT_11	NAND	PU	Boot device multiplexing pin 11. Please refer to following Table10 for functional multiplex information.	I/O
U23	BOOT_12	NAND	PD	Boot device multiplexing pin 12. Please refer to following Table10 for functional multiplex information.	I/O
U24	BOOT_13	NAND	PU	Boot device multiplexing pin 13. Please refer to following Table10 for functional multiplex information.	I/O
U27	BOOT_14	NAND	PU	Boot device multiplexing pin 14. Please refer to following Table10 for functional multiplex information.	I/O
U26	BOOT_15	NAND	PU	Boot device multiplexing pin 15. Please refer to following Table10 for functional multiplex information.	I/O
T26	BOOT_16	NAND	PU	Boot device multiplexing pin 16. Please refer to following Table10 for functional multiplex information.	I/O
T25	BOOT_17	NAND	PU	Boot device multiplexing pin 17. Please refer to following Table10 for functional multiplex information.	I/O
T24	GPIOC_0	GPIOC	PD	General purpose input/output bank C signal 0. Please refer to following Table3 for functional multiplex information.	I/O
T23	GPIOC_1	GPIOC	PD	General purpose input/output bank C signal 1. Please refer to following Table3 for functional multiplex information.	I/O
R22	GPIOC_2	GPIOC	PD	General purpose input/output bank C signal 2. Please refer to following Table3 for functional multiplex information.	I/O
R23	GPIOC_3	GPIOC	PD	General purpose input/output bank C signal 3. Please refer to following Table3 for functional multiplex information.	I/O
R25	GPIOC_4	GPIOC	PD	General purpose input/output bank C signal 4. Please refer to following Table3 for functional multiplex information.	I/O
R26	GPIOC_5	GPIOC	PD	General purpose input/output bank C signal 5. Please refer to following Table3 for functional multiplex information.	I/O
N25	GPIOC_6	GPIOC	PD	General purpose input/output bank C signal 6. Please refer to following Table3 for functional multiplex information.	I/O
N22	EFUSE_VDD25	Power		Analog power supply 2.5V for eFuse	AP
P23	AVSS25_MIPI	Power		Analog power ground 2.5V for MIPI	AP
P25	MIPI_DATAN0	MIPI		MIPI line 0 negative signal	I
P26	MIPI_DATAP0	MIPI		MIPI line 0 positive signal	I
N23	AVDD25_MIPI	MIPI		Analog power supply 2.5V for MIPI	AP

N27	MIPI_DATAN1	MIPI		MIPI line 1 negative signal	I
N26	MIPI_DATAP1	MIPI		MIPI line 1 positive signal	I
P24	AVSS25_MIPI	MIPI		Analog power ground for MIPI	AP
M25	MIPI_CLKN	MIPI		MIPI Clock negative input	I
M26	MIPI_CLKP	MIPI		MIPI Clock positive output	I
N24	AVDD25_MIPI	MIPI		Analog power supply 2.5V for MIPI	AP
L25	MIPI_DATAN2	MIPI		MIPI line 2 negative signal	I
L26	MIPI_DATAP2	MIPI		MIPI line 2 positive signal	I
K25	MIPI_DATAN3	MIPI		MIPI line 3 negative signal	I
K26	MIPI_DATAP3	MIPI		MIPI line 3 positive signal	I
K27	MIPI_REXT	MIPI		MIPI external resistor connection	AIO
M22	MIPI_CEXT	MIPI		MIPI external capacitor connection	AIO
L22	USBA_VSSA	USB		USB ground	AP
M23	USB_VDD25	USB		USB 2.5V power	AP
J25	USBA_TXRTUNE	USB		USB Port B external compensation resistor connection	AIO
J26	USBA_DM	USB		USB host negative data signal	AIO
J27	USBA_DP	USB		USB host positive data signal	AIO
L24	USB_VDD33	USB		USB 3.3V power	AP
L23	USBA_VBUS	USB		USB OTG cable power detection	AI
K24	USB_DVDD	USB		USB Core power supply 1.1V	P
K23	USBA_ID	USB		USB OTG mini-receptacle identifier between mini-A/mini-B plug	AI
H25	USBB_VBUS	USB		USB ground	AP
H26	USBB_DP	USB		USB host positive data signal	AIO
J22	USBB_VSSA	USB		USB ground	AP
G25	USBB_DM	USB		USB host negative data signal	AIO
G26	USBB_TXRTUNE	USB		USB Port B external compensation resistor connection	AIO
F27	AH_DHVDD	VDAC		Video DAC power supply 2.5V	P
J23	AH_DVDD	VDAC		Video DAC core power supply 1.1V	P
F26	VREFOUT	VDAC		Video DAC voltage reference output	AO
T17	VSS	VDAC		Power ground	P
H23	AHVSS	VDAC		Video DAC power ground	P
F25	RSET	VDAC		Video DAC external resistor connection for adjusting DAC full-scale output current magnitude	AIO
E26	COMP	VDAC		Video DAC external compensation capacitor connection	AO
E27	VREFIN	VDAC		Video DAC voltage reference input	AI
G23	AHVSSR	VDAC		Video DAC analog ground for channel R	AP
G24	AHVDDRGB	VDAC		Video DAC analog power supply 2.5V for channel RGB and bias circuits	AP
E25	IOR	VDAC		Video DAC channel R current output	AO
H24	AHVSSG	VDAC		Video DAC analog ground for channel G	AP
D26	IOG	VDAC		Video DAC channel G current output	AO
F23	AHVSSB	VDAC		Video DAC analog ground for channel B	AP
E24	AHVDDRGB	VDAC		Video DAC analog power supply 2.5V for channel RGB and bias circuits	AP
D25	IOB	VDAC		Video DAC channel B current output	AO
F22	AVSS25_ADC	Power		Analog power ground for ADC	AP
E23	AVDD25_ADC	Power		Analog power supply 2.5V for ADC	AP
A27	SARADC_CH0	ADC		ADC channel 0 input	AI
B27	SARADC_CH1	ADC		ADC channel 1 input	AI
C27	SARADC_CH2	ADC		ADC channel 2 input	AI
A26	SARADC_CH3	ADC		ADC channel 3 input	AI
B26	SARADC_CH4	ADC		ADC channel 4 input	AI
C26	SARADC_CH5	ADC		ADC channel 5 input	AI
A25	SARADC_CH6	ADC		ADC channel 6 input	AI

B25	SARADC_CH7	ADC		ADC channel 7 input	AI
E22	ANALOG_OUT	System		Reserved	AO
C25	VGHL_CS1	LCD Panel		LCD VGHL current feedback	AI
D24	LED_CS0	LCD Panel		LED backlight current feedback	AO
C24	GPIOA_0	GPIOA	PU	General purpose input/output bank A signal 0. Please refer to following Table2 for functional multiplex information.	I/O
B24	GPIOA_1	GPIOA	PU	General purpose input/output bank A signal 1. Please refer to following Table2 for functional multiplex information.	I/O
C23	GPIOA_2	GPIOA	PU	General purpose input/output bank A signal 2. Please refer to following Table2 for functional multiplex information.	I/O
B23	GPIOA_3	GPIOA	PU	General purpose input/output bank A signal 3. Please refer to following Table2 for functional multiplex information.	I/O
C22	GPIOA_4	GPIOA	PU	General purpose input/output bank A signal 4. Please refer to following Table2 for functional multiplex information.	I/O
B22	GPIOA_5	GPIOA	PU	General purpose input/output bank A signal 5. Please refer to following Table2 for functional multiplex information.	I/O
A22	GPIOA_6	GPIOA	PU	General purpose input/output bank A signal 6. Please refer to following Table2 for functional multiplex information.	I/O
C21	GPIOA_7	GPIOA	PU	General purpose input/output bank A signal 7. Please refer to following Table2 for functional multiplex information.	I/O
D23	GPIOA_8	GPIOA	PU	General purpose input/output bank A signal 8. Please refer to following Table2 for functional multiplex information.	I/O
D22	GPIOA_9	GPIOA	PU	General purpose input/output bank A signal 9. Please refer to following Table2 for functional multiplex information.	I/O
E21	GPIOA_10	GPIOA	PU	General purpose input/output bank A signal 10. Please refer to following Table2 for functional multiplex information.	I/O
G21	GPIOA_11	GPIOA	PU	General purpose input/output bank A signal 11. Please refer to following Table2 for functional multiplex information.	I/O
E20	GPIOA_12	GPIOA	PU	General purpose input/output bank A signal 12. Please refer to following Table2 for functional multiplex information.	I/O
F21	GPIOA_13	GPIOA	PU	General purpose input/output bank A signal 13. Please refer to following Table2 for functional multiplex information.	I/O
D20	GPIOA_14	GPIOA	PU	General purpose input/output bank A signal 14. Please refer to following Table2 for functional multiplex information.	I/O
E19	GPIOA_15	GPIOA	PU	General purpose input/output bank A signal 15. Please refer to following Table2 for functional multiplex information.	I/O
A21	GPIOA_16	GPIOA	PU	General purpose input/output bank A signal 16. Please refer to following Table2 for functional multiplex information.	I/O
B21	GPIOA_17	GPIOA	PU	General purpose input/output bank A signal 17. Please refer to following Table2 for functional multiplex information.	I/O
C19	GPIOA_18	GPIOA	PU	General purpose input/output bank A signal 18. Please refer to following Table2 for functional multiplex information.	I/O
B20	GPIOA_19	GPIOA	PU	General purpose input/output bank A signal 19. Please refer to following Table2 for functional multiplex information.	I/O
C20	GPIOA_20	GPIOA	PU	General purpose input/output bank A signal 20. Please refer to following Table2 for functional multiplex information.	I/O
B19	GPIOA_21	GPIOA	PU	General purpose input/output bank A signal 21. Please refer to following Table2 for functional multiplex information.	I/O
C18	GPIOA_22	GPIOA	PU	General purpose input/output bank A signal 22. Please refer to following Table2 for functional multiplex information.	I/O
B18	GPIOA_23	GPIOA	PU	General purpose input/output bank A signal 23. Please refer to following Table2 for functional multiplex information.	I/O
A18	GPIOA_24	GPIOA	PU	General purpose input/output bank A signal 24. Please refer to following Table2 for functional multiplex information.	I/O
C17	GPIOA_25	GPIOA	PU	General purpose input/output bank A signal 25. Please refer to following Table2 for functional multiplex information.	I/O
A17	GPIOA_26	GPIOA	PU	General purpose input/output bank A signal 26. Please refer to following Table2 for functional multiplex information.	I/O
B17	GPIOA_27	GPIOA	PU	General purpose input/output bank A signal 27. Please refer to following Table2 for functional multiplex information.	I/O
E18	GPIOB_0	GPIOB	PD	General purpose input/output bank B signal 0. Please refer to following Table2 for functional multiplex information.	I/O
E17	GPIOB_1	GPIOB	PD	General purpose input/output bank B signal 1. Please refer to following Table2 for functional multiplex information.	I/O
D17	GPIOB_2	GPIOB	PD	General purpose input/output bank B signal 2. Please refer to following Table2 for functional multiplex information.	I/O
D16	GPIOB_3	GPIOB	PD	General purpose input/output bank B signal 3. Please refer to following	I/O

				Table2 for functional multiplex information.	
E16	GPIOB_4	GPIOB	PD	General purpose input/output bank B signal 4. Please refer to following Table2 for functional multiplex information.	I/O
E15	GPIOB_5	GPIOB	PD	General purpose input/output bank B signal 5. Please refer to following Table2 for functional multiplex information.	I/O
F15	GPIOB_6	GPIOB	PD	General purpose input/output bank B signal 6. Please refer to following Table2 for functional multiplex information.	I/O
E14	GPIOB_7	GPIOB	PD	General purpose input/output bank B signal 7. Please refer to following Table2 for functional multiplex information.	I/O
C16	GPIOB_8	GPIOB	PD	General purpose input/output bank B signal 8. Please refer to following Table2 for functional multiplex information.	I/O
B16	GPIOB_9	GPIOB	PD	General purpose input/output bank B signal 9. Please refer to following Table2 for functional multiplex information.	I/O
C15	GPIOB_10	GPIOB	PD	General purpose input/output bank B signal 10. Please refer to following Table2 for functional multiplex information.	I/O
B15	GPIOB_11	GPIOB	PD	General purpose input/output bank B signal 11. Please refer to following Table2 for functional multiplex information.	I/O
C14	GPIOB_12	GPIOB	PD	General purpose input/output bank B signal 12. Please refer to following Table2 for functional multiplex information.	I/O
B14	GPIOB_13	GPIOB	PD	General purpose input/output bank B signal 13. Please refer to following Table2 for functional multiplex information.	I/O
A14	GPIOB_14	GPIOB	PD	General purpose input/output bank B signal 14. Please refer to following Table2 for functional multiplex information.	I/O
C13	GPIOB_15	GPIOB	PD	General purpose input/output bank B signal 15. Please refer to following Table2 for functional multiplex information.	I/O
A13	GPIOB_16	GPIOB	PD	General purpose input/output bank B signal 16. Please refer to following Table2 for functional multiplex information.	I/O
B13	GPIOB_17	GPIOB	PD	General purpose input/output bank B signal 17. Please refer to following Table2 for functional multiplex information.	I/O
C12	GPIOB_18	GPIOB	PD	General purpose input/output bank B signal 18. Please refer to following Table2 for functional multiplex information.	I/O
B12	GPIOB_19	GPIOB	PD	General purpose input/output bank B signal 19. Please refer to following Table2 for functional multiplex information.	I/O
C11	GPIOB_20	GPIOB	PD	General purpose input/output bank B signal 20. Please refer to following Table2 for functional multiplex information.	I/O
B11	GPIOB_21	GPIOB	PD	General purpose input/output bank B signal 21. Please refer to following Table2 for functional multiplex information.	I/O
C10	GPIOB_22	GPIOB	PD	General purpose input/output bank B signal 22. Please refer to following Table2 for functional multiplex information.	I/O
B10	GPIOB_23	GPIOB	PD	General purpose input/output bank B signal 23. Please refer to following Table2 for functional multiplex information.	I/O
D14	GPIOD_0	GPIOD	PD	General purpose input/output bank D signal 0. Please refer to following Table2 for functional multiplex information.	I/O
D13	GPIOD_1	GPIOD	PD	General purpose input/output bank D signal 1. Please refer to following Table2 for functional multiplex information.	I/O
E13	GPIOD_2	GPIOD	PD	General purpose input/output bank D signal 2. Please refer to following Table2 for functional multiplex information.	I/O
E12	GPIOD_3	GPIOD	PD	General purpose input/output bank D signal 3. Please refer to following Table2 for functional multiplex information.	I/O
E11	GPIOD_4	GPIOD	PD	General purpose input/output bank D signal 4. Please refer to following Table2 for functional multiplex information.	I/O
D10	GPIOD_5	GPIOD	PD	General purpose input/output bank D signal 5. Please refer to following Table2 for functional multiplex information.	I/O
E10	GPIOD_6	GPIOD	PD	General purpose input/output bank D signal 6. Please refer to following Table2 for functional multiplex information.	I/O
E9	GPIOD_7	GPIOD	PD	General purpose input/output bank D signal 7. Please refer to following Table2 for functional multiplex information.	I/O
E8	GPIOD_8	GPIOD	PD	General purpose input/output bank D signal 8. Please refer to following Table2 for functional multiplex information.	I/O
D8	GPIOD_9	GPIOD	PD	General purpose input/output bank D signal 9. Please refer to following Table2 for functional multiplex information.	I/O
A10	GPIOE_0	GPIOE	PU	General purpose input/output bank E signal 0. Please refer to following Table2 for functional multiplex information.	I/O
A9	GPIOE_1	GPIOE	PU	General purpose input/output bank E signal 1. Please refer to following Table2 for functional multiplex information.	I/O
B9	GPIOE_2	GPIOE	PU	General purpose input/output bank E signal 2. Please refer to following Table2 for functional multiplex information.	I/O
C9	GPIOE_3	GPIOE	PU	General purpose input/output bank E signal 3. Please refer to following	I/O

				Table2 for functional multiplex information.	
B8	GPIOE_4	GPIOE	PU	General purpose input/output bank E signal 4. Please refer to following Table2 for functional multiplex information.	I/O
C8	GPIOE_5	GPIOE	PU	General purpose input/output bank E signal 5. Please refer to following Table2 for functional multiplex information.	I/O
B7	GPIOE_6	GPIOE	PU	General purpose input/output bank E signal 6. Please refer to following Table2 for functional multiplex information.	I/O
C7	GPIOE_7	GPIOE	PU	General purpose input/output bank E signal 7. Please refer to following Table2 for functional multiplex information.	I/O
D7	GPIOE_8	GPIOE	PU	General purpose input/output bank E signal 8. Please refer to following Table2 for functional multiplex information.	I/O
E7	GPIOE_9	GPIOE	PU	General purpose input/output bank E signal 9. Please refer to following Table2 for functional multiplex information.	I/O
E6	GPIOE_10	GPIOE	PU	General purpose input/output bank E signal 10. Please refer to following Table2 for functional multiplex information.	I/O
D5	GPIOE_11	GPIOE	PU	General purpose input/output bank E signal 11. Please refer to following Table2 for functional multiplex information.	I/O
C6	GPIOZ_0	GPIOZ	PU	General purpose input/output bank E signal 0. Please refer to following Table2 for functional multiplex information.	I/O
B6	GPIOZ_1	GPIOZ	PU	General purpose input/output bank E signal 1. Please refer to following Table2 for functional multiplex information.	I/O
A6	GPIOZ_2	GPIOZ	PU	General purpose input/output bank E signal 2. Please refer to following Table2 for functional multiplex information.	I/O
C5	GPIOZ_3	GPIOZ	PU	General purpose input/output bank E signal 3. Please refer to following Table2 for functional multiplex information.	I/O
A5	GPIOZ_4	GPIOZ	PU	General purpose input/output bank E signal 4. Please refer to following Table2 for functional multiplex information.	I/O
B5	GPIOZ_5	GPIOZ	PU	General purpose input/output bank E signal 5. Please refer to following Table2 for functional multiplex information.	I/O
C4	GPIOZ_6	GPIOZ	PU	General purpose input/output bank E signal 6. Please refer to following Table2 for functional multiplex information.	I/O
B4	GPIOZ_7	GPIOZ	PU	General purpose input/output bank E signal 7. Please refer to following Table2 for functional multiplex information.	I/O
B3	GPIOZ_8	GPIOZ	PU	General purpose input/output bank E signal 8. Please refer to following Table2 for functional multiplex information.	I/O
A3	GPIOZ_9	GPIOZ	PU	General purpose input/output bank E signal 9. Please refer to following Table2 for functional multiplex information.	I/O
C3	GPIOZ_10	GPIOZ	PU	General purpose input/output bank E signal 10. Please refer to following Table2 for functional multiplex information.	I/O
A2	GPIOZ_11	GPIOZ	PU	General purpose input/output bank E signal 11. Please refer to following Table2 for functional multiplex information.	I/O
A1	GPIOZ_12	GPIOZ	PU	General purpose input/output bank E signal 12. Please refer to following Table2 for functional multiplex information.	I/O
F16	VDD_IO1	Power		Power supply for IO1	P
F12	VDD_IO2	Power		Power supply for IO2	P
F8	VDD_IO3	Power		Power supply for IO3	P
H6	VDD_IO4	Power		Power supply for IO4	P
P7	VDD_IO5	Power		Power supply for IO5	P
AA7	VDD_IO6	Power		Power supply for IO6	P
V22	VDD_IO7	Power		Power supply for IO7	P
K22	VDD_IO8	Power		Power supply for IO8	P
L13	VDD_CPU	Power		Power supply for CPU	P
F6	VSS	Power		Power ground	P
J6	VDD_CPU	Power		Power supply for CPU	P
M6	VDD_CPU	Power		Power supply for CPU	P
N6	VDD_CPU	Power		Power supply for CPU	P
T6	VDD_CPU	Power		Power supply for CPU	P
R6	VDD_CPU	Power		Power supply for CPU	P
P22	VDD_CPU	Power		Power supply for CPU	P
P21	VDD_CPU	Power		Power supply for CPU	P
L17	VDD_CPU	Power		Power supply for CPU	P
F18	VDD_CPU	Power		Power supply for CPU	P

F17	VDD_CPU	Power		Power supply for CPU	P
L11	VDD_CPU	Power		Power supply for CPU	P
G14	VDD_CPU	Power		Power supply for CPU	P
F13	VDD_CPU	Power		Power supply for CPU	P
U11	VSS	Power		Power ground	P
F9	VDD_CPU	Power		Power supply for CPU	P
F7	VDD_CPU	Power		Power supply for CPU	P
L15	VDD_CPU	Power		Power supply for CPU	P
L6	VDD_EE	Power		Core power supply 1.1V	P
U6	VDD_EE	Power		Core power supply 1.1V	P
AB10	VDD_EE	Power		Core power supply 1.1V	P
AA14	VDD_EE	Power		Core power supply 1.1V	P
AB18	VDD_EE	Power		Core power supply 1.1V	P
AA22	VDD_EE	Power		Core power supply 1.1V	P
U22	VDD_EE	Power		Core power supply 1.1V	P
T22	VDD_EE	Power		Core power supply 1.1V	P
F20	VDD_EE	Power		Core power supply 1.1V	P
D19	VDD_EE	Power		Core power supply 1.1V	P
F11	VDD_EE	Power		Core power supply 1.1V	P
AB11	VDDQ	DDR		DDR IO power supply	P
AA9	VDDQ	DDR		DDR IO power supply	P
AA13	VDDQ	DDR		DDR IO power supply	P
AB19	VDDQ	DDR		DDR IO power supply	P
R17	VSS	Power		Power ground	P
AB21	VDDQ	DDR		DDR IO power supply	P
AA21	VDDQ	DDR		DDR IO power supply	P
Y23	VSS	Power		Power ground	P
AG22	VSS	Power		Power ground	P
F19	VSS	Power		Power ground	P
E5	VSS	Power		Power ground	P
P4	VSS	Power		Power ground	P
AD12	VSS	Power		Power ground	P
P27	VSS	Power		Power ground	P
D11	VDD_EE	Power		Core power supply 1.1V	P
AF8	VSS	Power		Power ground	P
AB7	VSS	Power		Power ground	P
AD17	VSS	Power		Power ground	P
AB20	VSS	Power		Power ground	P
M11	VSS	Power		Power ground	P
N11	VSS	Power		Power ground	P
P11	VSS	Power		Power ground	P
R11	VSS	Power		Power ground	P
T11	VSS	Power		Power ground	P
L12	VSS	Power		Power ground	P
M12	VSS	Power		Power ground	P
N12	VSS	Power		Power ground	P
P12	VSS	Power		Power ground	P
R12	VSS	Power		Power ground	P
T12	VSS	Power		Power ground	P
U12	VSS	Power		Power ground	P
G7	VDD_EE	Power		Core power supply 1.1V	P

M13	VSS	Power		Power ground	P
N13	VSS	Power		Power ground	P
P13	VSS	Power		Power ground	P
R13	VSS	Power		Power ground	P
T13	VSS	Power		Power ground	P
U13	VSS	Power		Power ground	P
L14	VSS	Power		Power ground	P
M14	VSS	Power		Power ground	P
N14	VSS	Power		Power ground	P
P14	VSS	Power		Power ground	P
R14	VSS	Power		Power ground	P
T14	VSS	Power		Power ground	P
U14	VSS	Power		Power ground	P
H22	VDD_EE	Power		Core power supply 1.1V	P
M15	VSS	Power		Power ground	P
N15	VSS	Power		Power ground	P
P15	VSS	Power		Power ground	P
R15	VSS	Power		Power ground	P
T15	VSS	Power		Power ground	P
U15	VSS	Power		Power ground	P
L16	VSS	Power		Power ground	P
M16	VSS	Power		Power ground	P
N16	VSS	Power		Power ground	P
P16	VSS	Power		Power ground	P
R16	VSS	Power		Power ground	P
T16	VSS	Power		Power ground	P
U16	VSS	Power		Power ground	P
M17	VSS	Power		Power ground	P
N17	VSS	Power		Power ground	P
P17	VSS	Power		Power ground	P

Abbreviations:

- I = Digital input pin
- O = Digital output pin
- I/O = Digital input/output pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- PU=Pull-Up
- PD=Pull-down
- Z=Tri-State

3.3 Pin Multiplexing Tables

Multiple usage pins are used to converse pin consumption for different features. The AML8726-MX devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin also.

Table 2. GPIOA_x and GPIOB_x Multi-Function Pin

Pin#	Pin Name	LCD Input	FEC/ENC
C24	GPIOA_0	LCDin_R0	FEC_D0_A
B24	GPIOA_1	LCDin_R1	FEC_D1_A
C23	GPIOA_2	LCDin_R2	FEC_D2_A
B23	GPIOA_3	LCDin_R3	FEC_D3_A/ FEC_D0_C
C22	GPIOA_4	LCDin_R4	FEC_D4_A/ FEC_CLK_C
B22	GPIOA_5	LCDin_R5	FEC_D5_A/ FEC_SOP_C
A22	GPIOA_6	LCDin_R6	FEC_D6_A/ FEC_D_VALID_C
C21	GPIOA_7	LCDin_R7	FEC_D7_A/ FEC_FAIL_C
D23	GPIOA_8	LCDin_G0	FEC_CLK_A
D22	GPIOA_9	LCDin_G1	FEC_SOP_A
E21	GPIOA_10	LCDin_G2	FEC_D_VALID_A
G21	GPIOA_11	LCDin_G3	FEC_FAIL_A
E20	GPIOA_12	LCDin_G4	ENC_0
F21	GPIOA_13	LCDin_G5	ENC_1
D20	GPIOA_14	LCDin_G6	ENC_2
E19	GPIOA_15	LCDin_G7	ENC_3
A21	GPIOA_16	LCDin_B0	ENC_4
B21	GPIOA_17	LCDin_B1	ENC_5
C19	GPIOA_18	LCDin_B2	ENC_6
B20	GPIOA_19	LCDin_B3	ENC_7
C20	GPIOA_20	LCDin_B4	ENC_8
B19	GPIOA_21	LCDin_B5	ENC_9
C18	GPIOA_22	LCDin_B6	ENC_10
B18	GPIOA_23	LCDin_B7	ENC_11
A18	GPIOA_24	LCDin_CLK	ENC_12
C17	GPIOA_25	LCDin_HS	ENC_13
A17	GPIOA_26	LCDin_VS	ENC_14
B17	GPIOA_27	LCDin_DE	ENC_15
E18	GPIOB_0	LCD_R0	FEC_D0_B
E17	GPIOB_1	LCD_R1	FEC_D1_B
D17	GPIOB_2	LCD_R2	FEC_D2_B
D16	GPIOB_3	LCD_R3	FEC_D3_B
E16	GPIOB_4	LCD_R4	FEC_D4_B
E15	GPIOB_5	LCD_R5	FEC_D5_B
F15	GPIOB_6	LCD_R6	FEC_D6_B
E14	GPIOB_7	LCD_R7	FEC_D7_B
C16	GPIOB_8	LCD_G0	FEC_CLK_B
B16	GPIOB_9	LCD_G1	FEC_SOP_B
C15	GPIOB_10	LCD_G2	FEC_D_VALID_B
B15	GPIOB_11	LCD_G3	FEC_FAIL_B
C14	GPIOB_12	LCD_G4	FEC_FAIL_OUT
B14	GPIOB_13	LCD_G5	FEC_D_VALID_OUT
A14	GPIOB_14	LCD_G6	FEC_SOP_OUT
C13	GPIOB_15	LCD_G7	FEC_CLK_OUT
A13	GPIOB_16	LCD_B0	FEC_D0_OUT
B13	GPIOB_17	LCD_B1	FEC_D1_OUT
C12	GPIOB_18	LCD_B2	FEC_D2_OUT
B12	GPIOB_19	LCD_B3	FEC_D3_OUT
C11	GPIOB_20	LCD_B4	FEC_D4_OUT
B11	GPIOB_21	LCD_B5	FEC_D5_OUT
C10	GPIOB_22	LCD_B6	FEC_D6_OUT
B10	GPIOB_23	LCD_B7	FEC_D7_OUT

Table 3. GPIOC_x and GPIOD_x Multi-Function pins

Pin#	Pin Name	LCD/LED	FEC/ENC	TCON	SPDIF	HDMI	CLK	PCM/PWM	VGA
D14	GPIOD_0	LCD_VGHL_PWM						PWM_C	
D13	GPIOD_1	LED_BL_PWM						PWM_D	
E13	GPIOD_2			TCON_0_B (LCD) / TCON_STH1_B					
E12	GPIOD_3			TCON_1_B/ TCON_STV1_B					
E11	GPIOD_4			TCON_2_B/ TCON_OEH_B					
D10	GPIOD_5			TCON_3_B / TCON_CPV1_B					
E10	GPIOD_6			TCON_4_B/ TCON_OEV1_B					
E9	GPIOD_7			TCON_5_B/ TCON_CPH50_B/ TCON_CPH1_B/ TCON_CPH2_B/ TCON_CPH3_B					
E8	GPIOD_8			TCON_6_B / TCON_VCOM_B					
D8	GPIOD_9		ENC_16	TCON_7_B				PWM_A	
T24	GPIOC_0	LCD_VGHL_PWM						PWM_A	VGA_HS
T23	GPIOC_1	LED_BL_PWM						PWM_B	VGA_VS
R22	GPIOC_2			TCON_0_A (mLVDS)/ TCON_STH1					
R23	GPIOC_3			TCON_1_A/ TCON_STV1					
R25	GPIOC_4			TCON_2_A/ TCON_OEH					
R26	GPIOC_5			TCON_3_A/ TCON_CPV1					
N25	GPIOC_6			TCON_4_A/ TCON_OEV1					
AE4	GPIOC_7			TCON_5_A/ TCON_CPH50/ TCON_CPH1/ TCON_CPH/ TCON_CPH3					
AF4	GPIOC_8			TCON_6_A/ TCON_VCOM	SPDIF_IN				
AD4	GPIOC_9		ENC_17	TCON_7_A	SPDIF_OUT			PWM_C	
AE5	GPIOC_10					HDMI_HPD (5V)			
AF5	GPIOC_11					HDMI_SDA (5V)			
AE6	GPIOC_12					HDMI_SCL (5V)			
AF6	GPIOC_13					HDMI_CEC			
AD5	GPIOC_14	-	-	-	-	-	-	-	-
AG6	GPIOC_15						CLK_OUT1 (XTAL, RTC, PLL)		

Table 4. GPIOE_x Multi-Function pins

Pin#	Pin Name	I2S	SPDIF
A10	GPIOE_0	I2S_AUDIN_CH01	
A9	GPIOE_1	I2S_OUT_LR_CLK / AUDIN_LR_CLK	
B9	GPIOE_2	I2S_OUT_AM_CLK	
C9	GPIOE_3	I2S_OUT_AO_CLK / AUDIN_AO_CLK	
B8	GPIOE_4	I2S_OUT_CH01	
C8	GPIOE_5	I2S_OUT_CH23 / I2S_OUT_LR_CLK	
B7	GPIOE_6	I2S_OUT_CH45 / I2S_OUT_AM_CLK	
C7	GPIOE_7	I2S_OUT_CH67 / I2S_OUT_AO_CLK	
D7	GPIOE_8		SPDIF_OUT
E7	GPIOE_9	-	-
E6	GPIOE_10	-	-
D5	GPIOE_11	-	-

Table 5. GPIOX_x Multi-Function pins

Pin#	Pin Name	SPI	UART	I2C/I2S	SD	ISO7816	PCM/PWM	CLK
B2	GPIOX_0				SDXC_D0_A / SD_D0_A			
B1	GPIOX_1				SDXC_D1_A / SD_D1_A			
D4	GPIOX_2				SDXC_D2_A / SD_D2_A			
C1	GPIOX_3				SDXC_D3_A / SD_D3_A			
C2	GPIOX_4				SDXC_D4_A		PCM_OUT	
D3	GPIOX_5				SDXC_D5_A		PCM_IN	
D2	GPIOX_6				SDXC_D6_A		PCM_FS	
E3	GPIOX_7				SDXC_D7_A		PCM_CLK	
E2	GPIOX_8				SDXC_CLK_A / SD_CLK_A			
E4	GPIOX_9				SDXC_CMD_A / SD_CMD_A			
F4	GPIOX_10	-	-	-	-	-	-	-
F5	GPIOX_11	-	-	-	-	-	-	-
G5	GPIOX_12							CLK_OUT2 (XTAL, RTC, PLL)
G6	GPIOX_13		UART_TX_A					
F3	GPIOX_14		UART_RX_A					
F2	GPIOX_15		UART_CTS_A					
F1	GPIOX_16		UART_RTS_A					
G3	GPIOX_17		UART_TX_B	I2S_AM_CLK		ISO7816_DET	PCM_CLK	
G1	GPIOX_18		UART_RX_B	I2S_AO_CLK		ISO7816_RESET	PCM_FS	
G2	GPIOX_19		UART_CTS_B	I2S_LR_CLK		ISO7816_CLK		
H5	GPIOX_20		UART_RTS_B	I2S_IN_CH01/ I2S_OUT_CH01		ISO7816_DATA	PCM_IN	
H4	GPIOX_21		UART_TX_C			ISO7816_DET		
H3	GPIOX_22		UART_RX_C			ISO7816_RESET		
H2	GPIOX_23		UART_CTS_C / UART_TX_B			ISO7816_CLK		
J5	GPIOX_24		UART_RTS_C / UART_RX_B			ISO7816_DATA		
J4	GPIOX_25			I2C_SDA_A				
J3	GPIOX_26			I2C_SCK_A				
J2	GPIOX_27			I2C_SDA_B				
K5	GPIOX_28			I2C_SCK_B				
K3	GPIOX_29	SPI_SS2		I2C_SCK_C				
K2	GPIOX_30	SPI_RDYn		I2C_SDA_C				
K1	GPIOX_31	SPI_SS0						
L5	GPIOX_32	SPI_SS1						
L4	GPIOX_33	SPI_SCLK						
M4	GPIOX_34	SPI_MOSI						
M5	GPIOX_35	SPI_MISO						

Table 6. GPIOY_x Multi-Function pins

Pin#	Pin Name	ETH
L3	GPIOY_0	ETH_PHY_REF_CLK
L1	GPIOY_1	ETH_TX_CLK
L2	GPIOY_2	ETH_TX_EN
M3	GPIOY_3	ETH_TXD3
M2	GPIOY_4	ETH_TXD2
N3	GPIOY_5	ETH_TXD1
N2	GPIOY_6	ETH_TXD0
P3	GPIOY_7	ETH_RX_CLK
N5	GPIOY_8	ETH_RX_DV
P2	GPIOY_9	ETH_RXD3
P1	GPIOY_10	ETH_RXD2
R3	GPIOY_11	ETH_RXD1
R1	GPIOY_12	ETH_RXD0
P6	GPIOY_13	ETH_MDIO
P5	GPIOY_14	ETH_MDC
R5	GPIOY_15	-

Table 7. GPIOZ_x Multi-Function pins

Pin#	Pin Name	ITU601	CLK
C6	GPIOZ_0	ITU601_FIR / ITU601_IDQ	
B6	GPIOZ_1	ITU601_HS	
A6	GPIOZ_2	ITU601_VS	
C5	GPIOZ_3	ITU601_D0	
A5	GPIOZ_4	ITU601_D1	
B5	GPIOZ_5	ITU601_D2	
C4	GPIOZ_6	ITU601_D3	
B4	GPIOZ_7	ITU601_D4	
B3	GPIOZ_8	ITU601_D5	
A3	GPIOZ_9	ITU601_D6	-
C3	GPIOZ_10	ITU601_D7	-
A2	GPIOZ_11	ITU601_CLK	
A1	GPIOZ_12	-	CLK_OUT0(XTAL, RTC, PLL)

Table 8. GPIOAO_x Multi-Function pins

Pin#	Pin Name	UART	I2C/I2S	JTAG	CLK	Remote
AF25	GPIOAO_0	UART_TX_AO		JTAG_TDO		
AF27	GPIOAO_1	UART_RX_AO		JTAG_TDI		
AD24	GPIOAO_2	UART_CTS_AO/ UART_TX_PMIC	I2C_SCK_AO/ I2C_CLK_SLAVE_AO	JTAG_TMS		
AE26	GPIOAO_3	UART_RTS_AO UART_RX_PMIC	I2C_SDA_AO / I2C_SDA_SLAVE_AO	JTAG_TCK		
AD25	GPIOAO_4	UART_TX_PMIC	I2C_SCK_AO/ I2C_SCK_SLAVE_AO			
AD26	GPIOAO_5	UART_RX_PMIC	I2C_SDA_AO/ I2C_SDA_SLAVE_AO			
AC26	GPIOAO_6				CLK_OUT2(XTAL, RTC, PLL)	
AB25	GPIOAO_7					REMOTE_INPUT
AB26	GPIOAO_8	UART_TX_PMIC		JTAG_TCK		
AB27	GPIOAO_9	UART_RX_PMIC		JTAG_TMS		
AA25	GPIOAO_10	UART_CTS_PMIC		JTAG_TDI		
AA26	GPIOAO_11	UART_RTS_PMIC		JTAG_TDO	CLK_OUT2(XTAL, RTC, PLL)	

Table 9. CARD_x Multi-Function Pin

Pin#	Pin Name	SDXC	SDIO
R2	CARD_0	SDXC_D0_B	SD_D0_B
R4	CARD_1	SDXC_D1_B	SD_D1_B
T5	CARD_2	SDXC_D2_B	SD_D2_B
T3	CARD_3	SDXC_D3_B	SD_D3_B
T2	CARD_4	SDXC_CLK_B	SD_CLK_B
U5	CARD_5	SDXC_CMD_B	SD_CMD_B
U4	CARD_6	-	-
U3	CARD_7	-	-
U2	CARD_8	-	-

Table 10. BOOT_x Multi-Function Pin

Pin#	Pin Name	NAND	SDXC	SDIO	NOR_SPI
Y25	BOOT_0	NAND_IO_0	SDXC_D0_C	SD_D0_C	
Y26	BOOT_1	NAND_IO_1	SDXC_D1_C	SD_D1_C	
W25	BOOT_2	NAND_IO_2	SDXC_D2_C	SD_D2_C	
W26	BOOT_3	NAND_IO_3	SDXC_D3_C	SD_D3_C	
V25	BOOT_4	NAND_IO_4	SDXC_D4_C	-	
V26	BOOT_5	NAND_IO_5	SDXC_D5_C	-	
V27	BOOT_6	NAND_IO_6	SDXC_D6_C	-	
U25	BOOT_7	NAND_IO_7	SDXC_D7_C	-	
Y24	BOOT_8	NAND_CE0（boot）	-	-	
W24	BOOT_9	NAND_CE1	-	-	
W23	BOOT_10	NAND_CE2/NAND_RB0	SDXC_CMD_C	SD_CMD_C	
V23	BOOT_11	NAND_CE3/NAND_BR1	SDXC_CLK_C(bootable)	SD_CLK_C	
U23	BOOT_12	NAND_ALE	-	-	SPI_NOR_D_A
U24	BOOT_13	NAND_CLE	-	-	SPI_NOR_Q_A
U27	BOOT_14	NAND_WEn_CLK	-	-	SPI_NOR_C_A
U26	BOOT_15	NAND_REn_WR	-	-	-
T26	BOOT_16	NAND_DQS	-	-	-
T25	BOOT_17	-	-	-	SPI_NRO_CS_n_A

3.4 Signal Descriptions

Table 11. LCD/LED Signal Description

Signal Name	Type	Description
LCDin_R0	I	Digital video input red bit 0 (LSB)
LCDin_R1	I	Digital video input red bit 1
LCDin_R2	I	Digital video input red bit 2
LCDin_R3	I	Digital video input red bit 3
LCDin_R4	I	Digital video input red bit 4
LCDin_R5	I	Digital video input red bit 5
LCDin_R6	I	Digital video input red bit 6
LCDin_R7	I	Digital video input red bit 7 (MSB)
LCDin_G0	I	Digital video input green bit 0 (LSB)
LCDin_G1	I	Digital video input green bit 1
LCDin_G2	I	Digital video input green bit 2
LCDin_G3	I	Digital video input green bit 3
LCDin_G4	I	Digital video input green bit 4
LCDin_G5	I	Digital video input green bit 5
LCDin_G6	I	Digital video input green bit 6
LCDin_G7	I	Digital video input green bit 7 (MSB)
LCDin_B0	I	Digital video input blue bit 0 (LSB)
LCDin_B1	I	Digital video input blue bit 1
LCDin_B2	I	Digital video input blue bit 2
LCDin_B3	I	Digital video input blue bit 3
LCDin_B4	I	Digital video input blue bit 4
LCDin_B5	I	Digital video input blue bit 5
LCDin_B6	I	Digital video input blue bit 6
LCDin_B7	I	Digital video input blue bit 7 (MSB)
LCDin_CLK	I	Digital video input clock
LCDin_HS	I	Digital video input horizontal sync
LCDin_VS	I	Digital video input vertical sync
LCDin_DE	I	Digital video input data enable
LCD_R0	O	TTL LCD data output red bit 0 (LSB)
LCD_R1	O	TTL LCD data output red bit 1
LCD_R2	O	TTL LCD data output red bit 2
LCD_R3	O	TTL LCD data output red bit 3
LCD_R4	O	TTL LCD data output red bit 4
LCD_R5	O	TTL LCD data output red bit 5
LCD_R6	O	TTL LCD data output red bit 6
LCD_R7	O	TTL LCD data output red bit 7 (MSB)
LCD_G0	O	TTL LCD data output green bit 0 (LSB)
LCD_G1	O	TTL LCD data output green bit 1
LCD_G2	O	TTL LCD data output green bit 2
LCD_G3	O	TTL LCD data output green bit 3
LCD_G4	O	TTL LCD data output green bit 4
LCD_G5	O	TTL LCD data output green bit 5
LCD_G6	O	TTL LCD data output green bit 6
LCD_G7	O	TTL LCD data output green bit 7 (MSB)
LCD_B0	O	TTL LCD data output blue bit 0 (LSB)
LCD_B1	O	TTL LCD data output blue bit 1
LCD_B2	O	TTL LCD data output blue bit 2

Signal Name	Type	Description
LCD_B3	O	TTL LCD data output blue bit 3
LCD_B4	O	TTL LCD data output blue bit 4
LCD_B5	O	TTL LCD data output blue bit 5
LCD_B6	O	TTL LCD data output blue bit 6
LCD_B7	O	TTL LCD data output blue bit 7 (MSB)
LCD_VGHL_PWM	O	LCD panel VGHL tuning pulse width modulation signal output
LED_BL_PWM	O	LED backlight tuning pulse width modulation signal output

Table 12. FEC/ENC Interface Signal Description

Signal Name	Type	Description
FEC_D0_A	I	TS input port A data bus bit 0 (LSB)
FEC_D1_A	I	TS input port A data bus bit 1
FEC_D2_A	I	TS input port A data bus bit 2
FEC_D3_A/ FEC_D0_C	I	TS input port A data bus bit 3 Serial TS input data
FEC_D4_A/ FEC_CLK_C	I	TS input port A data bus bit 4 Serial TS input clock
FEC_D5_A/ FEC_SOP_C	I	TS input port A data bus bit 5 Serial TS start of stream signal
FEC_D6_A/ FEC_D_VALID_C	I	TS input port A data bus bit 6 Serial TS data valid signal
FEC_D7_A/ FEC_FAIL_C	I	TS input port A data bus bit 7 (MSB) Serial TS data failure signal
FEC_CLK_A	I	TS input port A clock
FEC_SOP_A	I	TS input port A start of stream signal
FEC_D_VALID_A	I	TS input port A date valid signal
FEC_FAIL_A	I	TS input port A data failure signal
FEC_D0_B	I	TS input port B data bus bit 0 (LSB)
FEC_D1_B	I	TS input port B data bus bit 1
FEC_D2_B	I	TS input port B data bus bit 2
FEC_D3_B	I	TS input port B data bus bit 3
FEC_D4_B	I	TS input port B data bus bit 4
FEC_D5_B	I	TS input port B data bus bit 5
FEC_D6_B	I	TS input port B data bus bit 6
FEC_D7_B	I	TS input port B data bus bit 7 (MSB)
FEC_CLK_B	I	TS input port B clock
FEC_SOP_B	I	TS input port B start of stream signal
FEC_D_VALID_B	I	TS input port B date valid signal
FEC_FAIL_B	I	TS input port B data failure signal
FEC_D0_OUT	O	TS output data bus bit 0 (LSB)
FEC_D1_OUT	O	TS output data bus bit 1
FEC_D2_OUT	O	TS output data bus bit 2
FEC_D3_OUT	O	TS output data bus bit 3
FEC_D4_OUT	O	TS output data bus bit 4
FEC_D5_OUT	O	TS output data bus bit 5
FEC_D6_OUT	O	TS output data bus bit 6
FEC_D7_OUT	O	TS output data bus bit 7 (MSB)
FEC_FAIL_OUT	O	TS output data failure signal
FEC_D_VALID_OUT	O	TS output data valid signal
FEC_SOP_OUT	O	TS output start of stream signal
FEC_CLK_OUT	O	TS output clock
ENC_0	I/O	Programmable interface signal 0

Signal Name	Type	Description
ENC_1	I/O	Programmable interface signal 1
ENC_2	I/O	Programmable interface signal 2
ENC_3	I/O	Programmable interface signal 3
ENC_4	I/O	Programmable interface signal 4
ENC_5	I/O	Programmable interface signal 5
ENC_6	I/O	Programmable interface signal 6
ENC_7	I/O	Programmable interface signal 7
ENC_8	I/O	Programmable interface signal 8
ENC_9	I/O	Programmable interface signal 9
ENC_10	I/O	Programmable interface signal 10
ENC_11	I/O	Programmable interface signal 11
ENC_12	I/O	Programmable interface signal 12
ENC_13	I/O	Programmable interface signal 13
ENC_14	I/O	Programmable interface signal 14
ENC_15	I/O	Programmable interface signal 15
ENC_16	I/O	Programmable interface signal 16
ENC_17	I/O	Programmable interface signal 17

Table 13. TCON Interface Signal Description

Signal Name	Type	Description
TCON_0_A	O	Programmable TCON port A signal 0 for LVDS and mini-LVDS
TCON_1_A	O	Programmable TCON port A signal 1 for LVDS and MINILVDS
TCON_2_A	O	Programmable TCON port A signal 2 for LVDS and MINILVDS
TCON_3_A	O	Programmable TCON port A signal 3 for LVDS and MINILVDS
TCON_4_A	O	Programmable TCON port A signal 4 for LVDS and MINILVDS
TCON_5_A	O	Programmable TCON port A signal 5 for LVDS and MINILVDS
TCON_6_A	O	Programmable TCON port A signal 6 for LVDS and MINILVDS
TCON_7_A	O	Programmable TCON port A signal 7 for LVDS and MINILVDS
TCON_0_B	O	Programmable TCON port B signal 0 for TTL LCD
TCON_1_B	O	Programmable TCON port B signal 1 for TTL LCD
TCON_2_B	O	Programmable TCON port B signal 2 for TTL LCD
TCON_3_B	O	Programmable TCON port B signal 3 for TTL LCD
TCON_4_B	O	Programmable TCON port B signal 4 for TTL LCD
TCON_5_B	O	Programmable TCON port B signal 5 for TTL LCD
TCON_6_B	O	Programmable TCON port B signal 6 for TTL LCD
TCON_7_B	O	Programmable TCON port B signal 7 for TTL LCD
TCON_STH1	O	Port A TCON 1st source driver start pulse for LVDS and mini-LVDS
TCON_STV1	O	Port A TCON 1st gate driver start pulse for LVDS and mini-LVDS
TCON_OEH	O	Port A TCON output enable signal for source driver for LVDS and mini-LVDS
TCON_CPV1	O	Port A TCON 1st gate driver shift clock output for LVDS and mini-LVDS
TCON_OEV1	O	Port A TCON output enable signal for 1st gate driver for LVDS and mini-LVDS
TCON_CPH50/ TCON_CPH1/ TCON_CPH/ TCON_CPH3	O	Port A TCON source driver shift clock output for LVDS and mini-LVDS
TCON_VCOM	O	Port A TCON POL driving signal for LVDS and mini-LVDS
TCON_STH1_B	O	Port B TCON 1st source driver start pulse for TTL LCD
TCON_STV1_B	O	Port B TCON 1st gate driver start pulse for TTL LCD
TCON_OEH_B	O	Port B TCON output enable signal for source driver for TTL LCD
TCON_CPV1_B	O	Port B TCON 1st gate driver shift clock output for TTL LCD
TCON_OEV1_B	O	Port B TCON output enable signal for 1st gate driver for TTL LCD
TCON_CPH50_B/ TCON_CPH1_B/ TCON_CPH2_B/ TCON_CPH3_B	O	Port B TCON source driver shift clock output for TTL LCD
TCON_VCOM_B	O	Port B TCON POL driving signal for TTL LCD

Table 14. SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	I	SPDIF input signal
SPDIF_OUT	O	SPDIF output signal

Table 15. SPI Interface Signal Description

Signal Name	Type	Description
SPI_SS2	O	SPI slave select 2
SPI_RDYn	I	SPI Ready signal, low active
SPI_SS0	O	SPI slave select 0
SPI_SS1	O	SPI slave select 1
SPI_SCLK	O	SPI Serial Clock
SPI_MOSI	O	SPI Master Output, Slave Input
SPI_MISO	I	SPI Master Input, Slave Output

Table 16. UART Interface Signal Description

Signal Name	Type	Description
UART_TX_AO	O	UART Port AO data output
UART_RX_AO	I	UART Port AO data input
UART_CTS_AO	I	UART Port AO Clear To Send Signal
UART_RTS_AO	O	UART Port AO Ready To Send Signal
UART_TX_PMIC	O	UART Port PMIC data output
UART_RX_PMIC	I	UART Port PMIC data input
UART_CTS_PMIC	I	UART Port PMIC Clear To Send Signal
UART_RTS_PMIC	O	UART Port PMIC Ready To Send Signal
UART_TX_A	O	UART Port A data output
UART_RX_A	I	UART Port A data input
UART_CTS_A	I	UART Port A Clear To Send Signal
UART_RTS_A	O	UART Port A Ready To Send Signal
UART_TX_B	O	UART Port B data output
UART_RX_B	I	UART Port B data input
UART_CTS_B	I	UART Port B Clear To Send Signal
UART_RTS_B	O	UART Port B Ready To Send Signal
UART_TX_C	O	UART Port C data output
UART_RX_C	I	UART Port C data input
UART_CTS_C	I	UART Port C Clear To Send Signal
UART_RTS_C	O	UART Port C Clear To Send Signal

Table 17. I2S Interface Signal Description

Signal Name	Type	Description
I2S_OUT_CH67	O	I2S Audio Data Output channel 6 and 7
I2S_OUT_CH45	O	I2S Audio Data Output channel 4 and 5
I2S_OUT_CH23	O	I2S Audio Data Output channel 2 and 3
I2S_OUT_CH01	O	I2S Audio Data Output channel 0 and 1
I2S_IN_CH01	I	I2S Audio Data Input channel 0 and 1
I2S_LR_CLK	O	I2S Left/Right Clock Out
I2S_AM_CLK	O	I2S master clock output
I2S_AO_CLK	O/I	I2S data clock input/output

Table 18. I2C Interface Signal Description

Signal Name	Type	Description
I2C_SCK_AO/ I2C_SCK_SLAVE_AO	I/O	Always-on I2C serial clock line , Master or Slave, need pull high
I2C_SDA_AO/ I2C_SDA_SLAVE_AO	I/O	Always-on I2C serial data line, Master or Slave, need pull high
I2C_SDA_A	I/O	I2C bus port A data input/output, Master or Slave, need pull high
I2C_SCK_A	I/O	I2C bus port A clock input/output, Master or Slave, need pull high
I2C_SDA_B	I/O	I2C bus port B data input/output, Master or Slave, need pull high
I2C_SCK_B	I/O	I2C bus port B clock input/output, Master or Slave, need pull high
I2C_SCK_C	I/O	I2C bus port C clock input/output, Master or Slave, need pull high
I2C_SDA_C	I/O	I2C bus port C clock input/output, Master or Slave, need pull high

Table 19. HDMI Interface Signal Description

Signal Name	Type	Description
HDMI_HPD (5V)	I/O	HDMI hot plug in detection signal input
HDMI_SDA (5V)	I/O	HDMI I2C control interface data signal, need pull high
HDMI_SCL (5V)	I/O	HDMI I2C control interface clock signal, need pull high
HDMI_CEC	I/O	HDMI CEC (Consumer electronics control)

Table 20. SD Interface Signal Description

Signal Name	Type	Description
SDXC_D0_A /SD_D0_A	I/O	SDXC/SDIO Port A data bus bit 0 signal
SDXC_D1_A /SD_D1_A	I/O	SDXC/SDIO Port A data bus bit 1 signal
SDXC_D2_A /SD_D2_A	I/O	SDXC/SDIO Port A data bus bit 2 signal
SDXC_D3_A / SD_D3_A	I/O	SDXC/SDIO Port A data bus bit 3 signal
SDXC_D4_A	I/O	SDXC Port A data bus bit 4 signal
SDXC_D5_A	I/O	SDXC Port A data bus bit 5 signal
SDXC_D6_A	I/O	SDXC Port A data bus bit 6 signal
SDXC_D7_A	I/O	SDXC Port A data bus bit 7 signal
SDXC_CLK_A /SD_CLK_A	O	SDXC/SDIO Port A clock signal
SDXC_CMD_A / SD_CMD_A	I/O	SDXC/SDIO Port A command signal
SDXC_GPIO0_A	I/O	SDXC Port A GPIO bit 0 signal
SDXC_GPIO1_A	I/O	SDXC Port A GPIO bit 1 signal
SDXC_GPIO2_A	I/O	SDXC Port A GPIO bit 2 signal

Table 21. ISO7816 Interface Signal Description

Signal Name	Type	Description
ISO7816_DET	I	ISO 7816 detect signal
ISO7816_RESET	O	ISO 7816 reset signal
ISO7816_CLK	O	ISO 7816 clock signal
ISO7816_DATA	I/O	ISO 7816 serial data signal

Table 22. RMII/RGMII Interface Signal Description

Signal Name	Type	Description
ETH_PHY_REF_CLK	I/O	Ethernet RMII interface reference clock input /output
ETH_TX_CLK	O	Ethernet RMII/RGMII transmit clock
ETH_TX_EN	O	Ethernet RMII/RGMII Interface transmit enable
ETH_TXD3	O	Ethernet RGMII interface transmit data 3
ETH_TXD2	O	Ethernet RGMII interface transmit data 2
ETH_TXD1	O	Ethernet RMII/RGMII interface transmit data 1
ETH_TXD0	O	Ethernet RMII/RGMII interface transmit data 0
ETH_RX_CLK	I	Ethernet RMII/RGMII receive clock

Signal Name	Type	Description
ETH_RX_DV	I	Ethernet RMII/RGMII interface receive data valid signal
ETH_RXD3	I	Ethernet RGMII interface receive data 3
ETH_RXD2	I	Ethernet RGMII interface receive data 2
ETH_RXD1	I	Ethernet RMII/RGMII interface receive data 1
ETH_RXD0	I	Ethernet RMII/RGMII interface receive data 0
ETH_MDIO	I/O	Ethernet RMII/RGMII interface management data input/output
ETH_MDC	O	Ethernet RMII/RGMII interface management data clock

Table 23. ITU601 Interface Signal Description

Signal Name	Type	Description
ITU601_FIR / ITU601_IDQ	I	ITU 601 Video Input Field Signal
ITU601_HS	I	ITU 601 Video Input Horizontal Sync Signal
ITU601_VS	I	ITU 601 Video Input Vertical Sync Signal
ITU601_D0	I	ITU 601 Video Input Data Bus bit 0 (LSB)
ITU601_D1	I	ITU 601 Video Input Data Bus bit 1
ITU601_D2	I	ITU 601 Video Input Data Bus bit 2
ITU601_D3	I	ITU 601 Video Input Data Bus bit 3
ITU601_D4	I	ITU 601 Video Input Data Bus bit 4
ITU601_D5	I	ITU 601 Video Input Data Bus bit 5
ITU601_D6	I	ITU 601 Video Input Data Bus bit 6
ITU601_D7	I	ITU 601 Video Input Data Bus bit 7 (MSB)
ITU601_CLK	I/O	ITU 601 Video Input Master Clock

Table 24. JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_TDO	O	JTAG Scan data output
JTAG_TDI	I	JTAG Scan data input
JTAG_TMS	I	JTAG Test mode select input
JTAG_TCK	I	JTAG Test clock input

Table 25. CLK Interface Signal Description

Signal Name	Type	Description
CLK_OUT3	O	XTAL, RTC CLK, PLL clock output 3
CLK_OUT2	O	XTAL, RTC CLK, PLL clock output 2
CLK_OUT1	O	XTAL, RTC CLK, PLL clock output 1
CLK_OUT0	O	XTAL, RTC CLK, PLL clock output 0

Note：all 4 CLK_OUT pin share same source, they will output same frequency signal if they are all set to clk_out function.

Table 26. Remote Interface Signal Description

Signal Name	Type	Description
REMOTE_INPUT	I	IR Remote controller input signal

Table 27. PWM Interface Signal Description

Signal Name	Type	Description
PWM_A	O	PWM channel A output signal
PWM_B	O	PWM channel B output signal
PWM_C	O	PWM channel C output signal
PWM_D	O	PWM channel D output signal

Table 28. PCM Interface Signal Description

Signal Name	Type	Description
PCM_OUT	O	PCM output data stream
PCM_IN	I	PCM input data stream
PCM_FS	O	PCM frame synchronization
PCM_CLK	O	PCM master clock input

Table 29. VGA Interface Signal Description

Signal Name	Type	Description
VGA_HS	O	VGA output horizontal sync signal
VGA_VS	O	VGA output vertical sync signal

4. Operating Conditions

4.1 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Characteristic	Value	Unit
1.1V Core Supply Voltage	1.3	V
1.5V Supply Voltage	1.65	V
2.5V Supply Voltage	2.85	V
3.3V Supply Voltage	3.6	V
Input voltage, V_I	-0.5 ~ VDD+0.3	V
Junction Temperature		°C

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_CPU	Voltage For A9/Mali CPU core logic	0.85*	1.2	1.265	V
VDD_EE/AO	Voltage For other core logic	0.85*	1.1	1.21	V
VDDQ	DDR2/DDR3 SSTL Supply Voltage	1.14	1.2/1.25/1.35/1.5	1.575	V
AVDD25	2.5V AVDD for Analog/PLL	2.38	2.5	2.75	V
AVDD33	3.3V AVDD for USB/HDMI	3.0	3.3	3.45	V
VDD33_EE/AO	Digital IO Supply Voltage	2.38	3.0	3.45	V
RTC_VBAT	Supply voltage for RTC	2.38		3.45	
T_J	Junction Temperature	0		125	°C

Note:

1) Minimal VDD_CPU/VDD_EE/VDD_AO voltage is for sleep mode only while system runs at 32KHz. Higher clock will need higher voltage.

2) Voltage of VDD_CPU will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power.

3) Typical SSTL voltage: 1.5V for DDR3, 1.35V for DDR3L, 1.25V for DDR3U and 1.2V for LPDDR2.

4.3 DDR3/LPDDR2 SDRAM Timing Specifications

4.3.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core supply voltage	0.99	1.10	1.21	V
VDDQ	SSTL supply voltage(DDR3)	1.425	1.50	1.575	V
VDDQ	SSTL supply voltage(DDR3L)	1.28	1.35	1.45	V
VDDQ	SSTL supply voltage(LPDDR2)	1.14	1.20	1.30	V
Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

4.3.2 DC specifications - DDR3 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ-0.3		Vref-0.100	V
VOH	DC output logic high	0.8*VDDQ			V
VOL	DC output logic low			0.2*VDDQ	V
RTT	Input termination resistance to VDDQ/2	100 54 36	120 60 40	140 66 44	ohm

4.3.3 DC Specifications - LPDDR2 mode

Symbol	Parameter	Min	Nom	Max	Unit
VIH	DC input voltage high	Vref + 0.13		VDDQ	V
VIL	DC input voltage low	VSSQ-0.3		Vref-0.13	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V

4.3.4 AC specifications - DDR3 mode

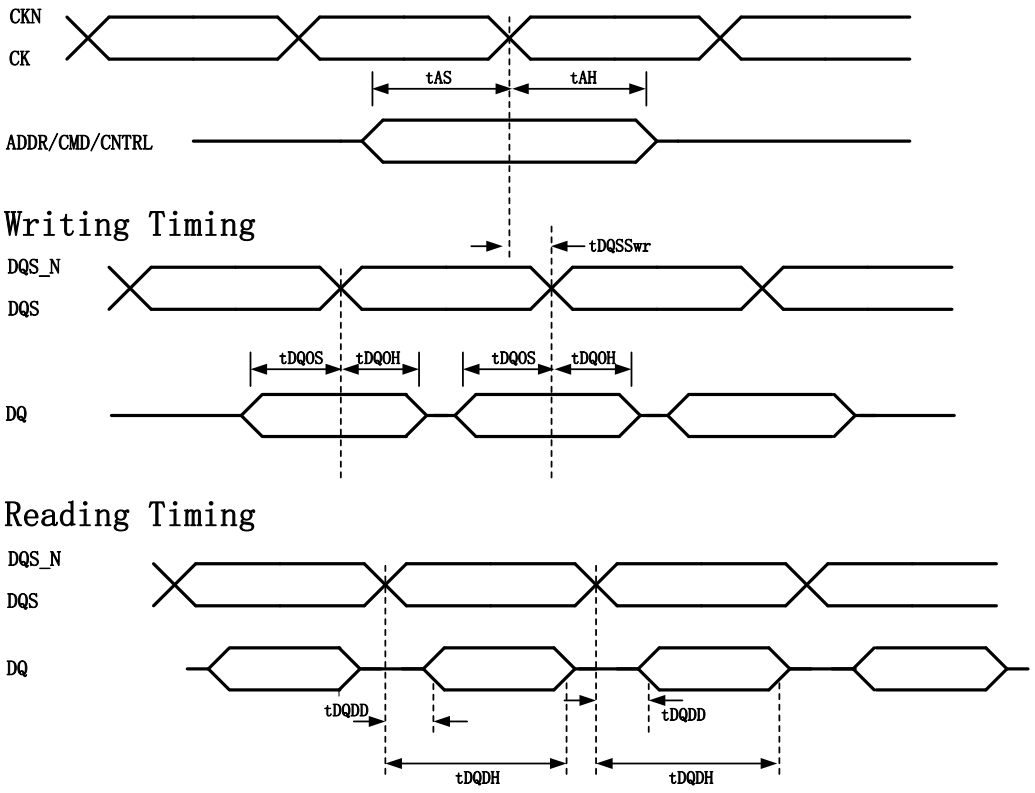
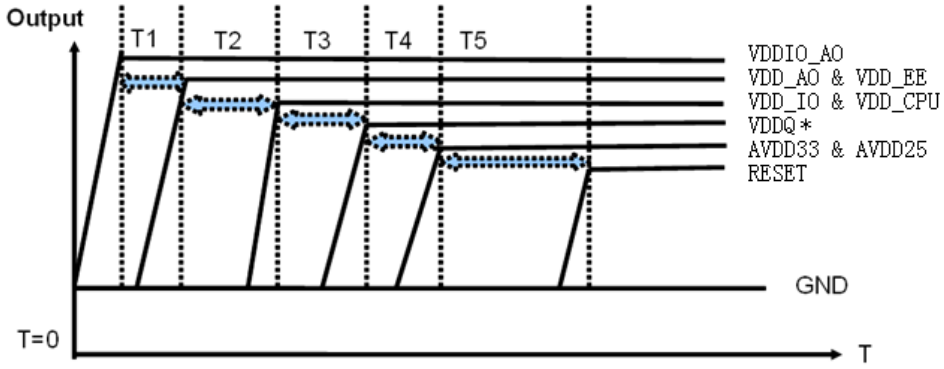


Table 30. DDR3 Timing Specification for 533Mhz(VDDQ = 1.5v)

Symbol	Description	Min.	Max.	Unit	Notes
tCK	Clock period	TBD	TBD	ns	
tCKL	Clock low level width	0.47	0.53	tCK	
tCKH	Clock high level width	0.47	0.53	tCK	
tAS	Addr/cmd/cntrl valid time before CK	0.8	-	ns	
tAH	Addr/cmd /cntl valid time after CK	0.8	-	ns	
tDQSSwr	When write, skew between CK and DQS/DQS_N.	-0.15	0.15	ns	
tDQOS	When write, DQ valid time before DQS .	0.4	-	ns	
tDQOH	When write, DQ valid time after DQS.	0.4		ns	
tDQDD	When read, the maximum setup skew allowed between DQ and DQS.	-	0.4	ns	
tDQDH	When read, the minimum hold time requirement	0.9	-	ns	
tDQSOH	When write, DQS output high width	0.47	0.53	tCK	
tDQSOL	When write DQS output low width	0.47	0.53	tCK	

4.4 Recommended Power on sequence



Note:

1) The diagram shows only power-on sequence, where higher output does not mean higher voltage.

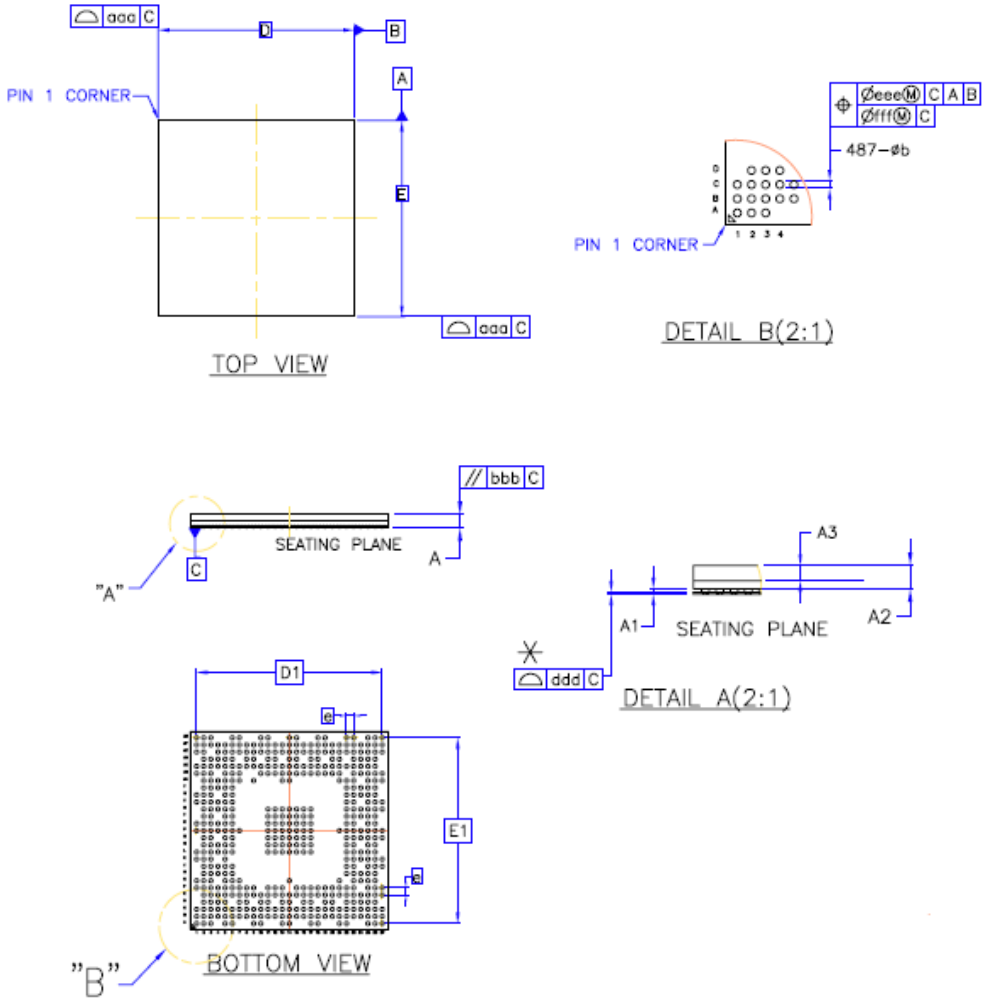
2) T1/T2/T3/T4 should be 0-3ms, T5 should > 40ms.

3) If VDD12_AO & VDD12_EE are not powered up at the same time, VDD12_AO should be powered up first.

4) Make sure SSTL_VDD is powered up after VDD12_AO & VDD12_EE. It's also possible to power up VDDQ after uBoot startup.

5. Mechanical Dimensions

The AML8726-MX processor comes in a 487 balls LFBGA RoHS package. The mechanical dimensions are given in millimeters as below:



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.41	---	---	0.056
A1	0.20	0.25	0.30	0.0079	0.0098	0.0118
A2	1.02	1.06	1.10	0.0401	0.0417	0.0433
A3	0.70 BASIC			0.0276 BASIC		
D	17.90	18.00	18.10	0.7047	0.7087	0.7126
D1	16.90 BASIC			0.6654 BASIC		
E	17.90	18.00	18.10	0.7047	0.7087	0.7126
E1	16.90 BASIC			0.6653 BASIC		
e	0.65 BASIC			0.0256 BASIC		
b	0.30	0.35	0.40	0.0118	0.0138	0.0157
aaa	0.10			0.0039		
bbb	0.10			0.0039		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		