AMN2120/2/3 WHDI™ Transmitter Family

Data Sheet

Version 0.1

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Revision History

Version	Date	Description
0.1	-	Initial Release

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Chapter 1

Introduction

The AMN2120/2/3 family is the second generation of WHDI technology baseband transmitters. This product family is the first to become fully WHDI 1.0 compliant, supporting wireless uncompressed Full HD video up to 1080p60 and UXGA resolutions. The ultimate quality and robustness of the HD video and audio achieved by AMN2120/2/3 are unmatched by any other wireless technology and offers a true alternative to cable.

The WHDI system transmits **uncompressed** video and audio streams wirelessly and thus simplifies and eliminates system issues experienced with other known wireless-based solutions, such as: lip-sync, large buffers and other burdens like retransmissions or error propagation.

The AMN2120/2/3 incorporates a standard digital audio and video interface. An integrated color space converter enables a direct connection to all major video sources. An industry standard S/PDIF and I^2S accepts the audio source in various digital formats.

The AMN2120/2/3 is based on MIMO technology transmitting downstream video and audio through up to four RF output channels and receiving a control data stream from one RF channel. Four digital-to-analog converters and one analog-to-digital converter are embedded within the chip.

The AMN2120/2/3 is controlled by an embedded MIPS M4K microcontroller for which AMIMON supplies the FW code. The system is designed to automatically identify the video source parameters in order to reduce to a minimum the system management requirements.

1.1 Features

- **Uncompressed and uncompromised FHD video quality**
- WHDI 1.0 compliance, including HDCP 2.0
- **Supports 20 and 40 MHz channels for supreme video quality and high rate video/audio signals**
- **Supports any uncompressed video resolutions with a pixel clock rate of up to 162 MHz, including:**
  - **HD:** 480i, 480p, 576i, 576p, 720p, 1080i, 1080p
  - **PC:** VGA (640x480), SVGA (800x600), XGA (1024x768), UGA(1600x1200)
  - **Panel:** 854x800, 1280x768, 1366x768, 1920x1080
- **Integrated MIPS M4K Core**
  - **Flexible system level control with up to 8 GPIO**
  - **Built in support of 2 Pulse Width Modulations (PWM) for IR and CEC support**
- **Static Video Recognition**

- **High Definition Interface:**
  - Digital video:
    - 36-bit RGB or YCrCb (4:4:4)
    - 24 YCrCb (4:2:2)
  - Enhanced syncs recovery mechanism
    - Enables the support of non-standard resolutions
- **Audio:**
  - Up to 18 Mbps throughput of audio stream:
    - **I^2S:** Up to eight PCM channels (sampled up to 192 KHz x 24 bit)
    - **SPDIF:** Including AC-3, DTS
- **Strong 128/256-bit AES based encryption**
- **User-defined downlink channel with up to 1 Mbps for data and control**
- **User-defined uplink channel with up to 100 Kbps for data and control**
- **Less than 1mSec latency between video source and video sink**
- **Supports MIMO technology:**
  - Four output RF channels with optional support of only two RF channels for price or mechanical sensitive applications
  - One input channel with optional antenna switching
- **169 Balls LBGA package**

1.2 Family of Products

AMN2120/2/3 is a family of devices as specified below:

- **AMN2120:** A **professional** WHDI Transmitter baseband device with high performance, low power consumption and a high ambient temperature range, suitable for medical and professional applications.
- **AMN2122:** A **consumer electronic** WHDI Transmitter baseband device, enabling low power consumption and high ambient temperature range, suitable for CE environmental requirements. This device is NOT suitable for medical applications.
- **AMN2123:** Is designed for **low** cost **applications** with lower ambient temperature capabilities and a non-tight power regime. This device is NOT suitable for medical applications.

1.3 System Level Description

The following section provides a general description of the AMIMON Video Source Unit (VSU) system which contains the Baseband Transmitter chip.

The baseband chip is the heart of the WHDI VSU, which is designed to modulate and transmit downstream video and audio content over a wireless medium and to receive a control channel over the wireless upstream. The modulation uses an 18 MHz or 40Mhz bandwidth and is carried over a 5 GHz unlicensed band. Figure 1 below shows a conceptual block diagram of the AMIMON VSU. The inputs to the VSU are digital uncompressed video, digital audio and control, all are through the WHDI connector. The block diagram shows a MIMO design of four wireless output channels and a slow rate data input wireless channel. The MAC uC is responsible for control and management.

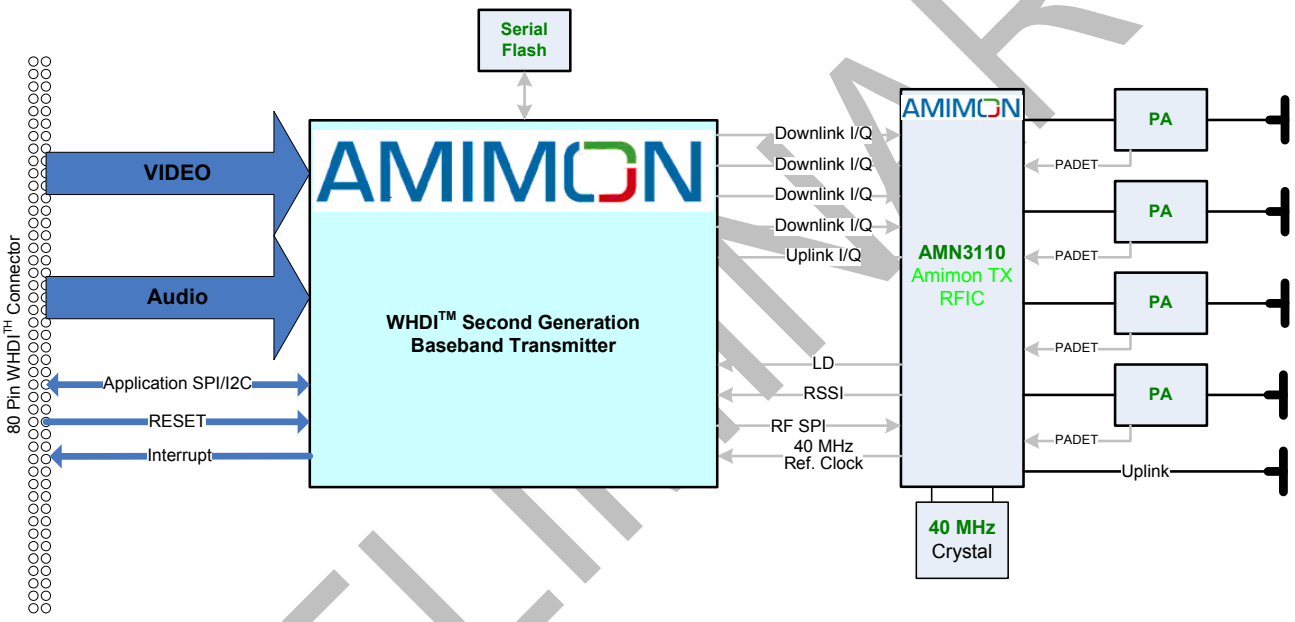

Figure 1: System Level Block Diagram (VSU)

The main building blocks of the VSU module (which is a board) are as follows:

- Serial Flash for the internal CPU code and data storage
- AMN3110 WHDI Baseband Transmitter
- RF Power Amplifier
- 40 MHz crystal

Serial Flash

The serial flash contains the firmware and the system data required for the system operation. The size of the flash is 4 Mbit and the operating frequency is up to 50 MHz.

AMN3110 - 5 GHz Transceiver

The RF section of the VSU contains AMN3110 which is embedded in it. The AMN3110 is a single-chip, with four RF transmitters and one RF receiver IC designed specifically for single-band 4.9 GHz to 5.875 GHz WHDI applications. It includes all the circuitry necessary to implement the RF transceiver function, and provides a fully integrated receive path, transmit path, VCO, frequency synthesizer and baseband/control interface. Only the PA, RF switches, RF band-pass filters (BPF), RF BALUNs and a small number of passive components are required to form the complete RF front-end solution.

Power Amplifier (PA)

In order to extend the operating range for the VSU, the RF transmitter uses power amplifiers. Each power amplifier has an output power detector for power management purposes.

Chapter 2

Pin Assignment

The following diagram is a graphical representation of the balls assignment listed in the following tables:

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	iref1	iref0	ioutnq0	ioutpi0	vinni	vinpq	vainp0	clkin_pad	PA_ENABLE	RF_LD	RF_SPI_CLK	I2CM_CLK	I2CM_DATA
B	ioutpi1	ioutni1	ioutpq0	ioutni0	vinpi	vinnq	vainp1	dvdd33_pad	UL_RX_ANT_SEL_N	RF_SPI_CS	APP_REF_CLK	APP_SPI_MISO_I2CS_DATA	APP_SPI_CLK
C	ioutnq1	ioutpq1	avddhv_iqadc	vbg	agnd_iqadc	avddhv_pllsys	avdd_pllsys	dvdd_pad	UL_RX_ANT_SEL_P	RF_SPI_DOUT	APP_SPI_CS_I2CS_CLK	APP_SPI_MOSI	UC_UART_TXD
D	ioutpi2	ioutni2	agnd_iqdac3210	agndref	avdd_iqadc	agnd_pllsys	agndhv_pllsys	dgnd_pad	VDD	VDD_IO	UC_UART_RXD	UC_GPIO_0_PHY_UART_TXD	UC_GPIO_1_PHY_UART_RXD
E	ioutnq2	ioutpq2	avdd_iqadc3210	anatest	VSS	VSS	VSS	VSS	VDD	VDD_IO	UC_GPIO_2_RESET_O	UC_GPIO_3_RF_MAXIM	UC_GPIO_4
F	ioutpi3	ioutni3	iref2	VDD_GR	VSS	VSS	VSS	VSS	VSS	VDD	UC_GPIO_5	UC_GPIO_6	UC_GPIO_7
G	ioutnq3	ioutpq3	iref3	VSS_GR	VSS	VSS	VSS	VSS	VSS	VDD	FLASH_SPI_CLK	FLASH_SPI_SS	FLASH_SPI_MISO
H	AGND_POR	AVDD_POR	VREF_NVM	VDD	VSS	VSS	VDD_IO	VSS	VSS	VDD_IO	FLASH_SPI_MOSI	SPDIF_D	I2S_SCK
J	VPP_NVM	RESET_B_IN	TEST_CFG_0	VDD_IO	VDD	VDD	VDD_IO	VDD	VDD	VDD_IO	I2S_SD_2	I2S_SD_1	I2S_SD_0
K	TEST_SE	TEST_CFG_2	TEST_CFG_1	VD_33	VD_29	VD_25	VD_21	VD_17	VD_13	VD_9	VD_5	I2S_SD_3	I2S_WS
L	TAP_SEL	TCK	TDI	VD_34	VD_30	VD_26	VD_22	VD_18	VD_14	VD_10	VD_6	VD_2	I2S_MCK

M	TDO	TMS	HSYNC_I	VD_35	VD_31	VD_27	VD_23	VD_19	VD_15	VD_11	VD_7	VD_3	VD_0
N	TRST	DCLK_I	VSYNC_I	DE_I	VD_32	VD_28	VD_24	VD_20	VD_16	VD_12	VD_8	VD_4	VD_1

Figure 2: Ball Diagram

2.1 Video Input Pins

Table 1: Video Input Pins

PIN Name	Ball #	I/O	Description
D_0	M13	Input	36-bit Input Pixel Data Bus – bit 0
D_1	N13	Input	
D_2	L12	Input	
D_3	M12	Input	
D_4	N12	Input	
D_5	K11	Input	
D_6	L11	Input	
D_7	M11	Input	
D_8	N11	Input	
D_9	K10	Input	
D_10	L10	Input	
D_11	M10	Input	
D_12	N10	Input	
D_13	K9	Input	
D_14	L9	Input	
D_15	M9	Input	
D_16	N9	Input	
D_17	K8	Input	
D_18	L8	Input	
D_19	M8	Input	
D_20	N8	Input	
D_21	K7	Input	
D_22	L7	Input	
D_23	M7	Input	
D_24	N7	Input	

PIN Name	Ball #	I/O	Description
D_25	K6	Input	
D_26	L6	Input	
D_27	M6	Input	
D_28	N6	Input	
D_29	K5	Input	
D_30	L5	Input	
D_31	M5	Input	
D_32	N5	Input	
D_33	K4	Input	
D_34	L4	Input	
D_35	M4	Input	
HSYNC	M3	Input	Horizontal Sync input control signal
VSYNC	N3	Input	Vertical Sync input control signal
DE	N4	Input	Data Enable
DCLK	N2	Input	Input Data Clock

2.2 Audio Input Pins

Table 2: Audio Input Pins

PIN Name	Ball #	I/O	Description
SCK	H13	Input	I^2S Serial Clock
SD_0	J13	Input	I^2S Serial Data – Channel 1
SD_1	J12	Input	I^2S Serial Data – Channel 2
SD_2	J11	Input	I^2S Serial Data – Channel 3
SD_3	K12	Input	I^2S Serial Data – Channel 4
WS	K13	Input	I^2S Word Select
SPDIF	H12	Input	S/PDIF Audio Input
MCK	L13	Input	Audio Master Clock

2.3 Application Microcontroller Interface Pins

Table 3: Application Microcontroller Interface

PIN Name	Ball #	I/O	Description
APP_SPI_MISO/ APP_I2S_SDA	B12	Output	Application SPI MISO line. Shared with an Application I2C Serial Data line when the chip is in I2C mode
APP_SPI_CLK	B13	Input	Application SPI clock

APP_SPI_CS/ APP_I2CS_CLK	C11	Input	Application SPI Chip Select line. Shared with an Application I2C Serial Clock line when the chip is in I2C mode
APP_SPI_MOSI	C12	Input	Application SPI MISO line Application SPI clock
UC_UART_TXD	C13	Output	Embedded microcontroller UART transmit data line
UC_UART_RXD	D11	Input	Embedded microcontroller UART receive data line
UC_GPIO_0/ PHY_UART_TXD	D12	I/O	Embedded microcontroller GPIO 0. Shared with an additional UART port for direct communication of the chip registers.
UC_GPIO_1/ PHY_UART_RXD	D13	I/O	Embedded microcontroller GPIO 1. Shared with an additional UART port for direct communication of the chip registers
UC_GPIO_2	E11	I/O	Embedded microcontroller GPIO 2
UC_GPIO_3	E12	I/O	Embedded microcontroller GPIO 3
UC_GPIO_4	E13	I/O	Embedded microcontroller GPIO 4
UC_GPIO_5	F11	I/O	Embedded microcontroller GPIO 5
UC_GPIO_6	F12	I/O	Embedded microcontroller GPIO 6
UC_GPIO_7	F13	I/O	Embedded microcontroller GPIO 7
APP_REF_CLK	B11	Output	Optional 10 MHz reference clock. Internally generated from the input clock.

For the above signal connections between the baseband chip and the application microcontroller, refer to AMIMON's appropriate reference design file.

2.4 Configuration/Programming Pins

Table 4: Control Pins

PIN Name	Ball #	I/O	Description
RESET_N	J2	Input	Chip Reset Pin (Active Low)
I2CM_SCL	A12	Output	On-chip Two-wire serial clock line. Used to control external components
I2CM_SDA	A13	I/O	On-chip Two-wire serial data line
FLASH_SPI_CLK	G11	Output	Serial Flash SPI clock
FLASH_SPI_SS	G12	Output	Serial Flash SPI Slave Select. Add a pull-up resistor to ensure that the flash is not selected during power-up
FLASH_SPI_MISO	G13	Input	Slave Flash Master Input Slave Output
FLASH_SPI_MOSI	H11	Output	Slave Flash Master Output Slave Input

2.5 JTAG Pins

Table 5: JTAG Pins

PIN Name	Ball #	I/O	Description
TCK	L2	Input	Test Clock Input, connected to Pull-Up resistor
TDI	L3	Input	Test Data Input line, connected to Pull-Up resistor
TDO	M1	Output	Test Data Output line
TMS	M2	Input	Test Mode Select Input, connected to Pull-Up resistor
TRST	N1	Input	Test-Reset Input, connected to Pull-Down resistor
TAP_SEL	L1	Input	Tap Select. Used to select between the embedded microcontroller JTAG chain and the chip JTAG chain

2.6 RF Interface Pins

Table 6: RF Analog Interface Pins

PIN Name	Ball #	I/O	Description
UL_I_P	B5	Analog Input	I Differential Voltage Input, Channel 0
UL_I_N	A5	Analog Input	I Differential Voltage Input, Channel 0
UL_Q_P	A6	Analog Input	Q Differential Voltage Input, Channel 0
UL_Q_N	B6	Analog Input	Q Differential Voltage Input, Channel 0
DL_I_P_0	A4	Analog Output	I current Output for Channel 0
DL_I_N_0	B4	Analog Output	I current Output for Channel 0
DL_Q_P_0	B3	Analog Output	Q current Output for Channel 0
DL_Q_N_0	A3	Analog Output	Q current Output for Channel 0
DL_IREF_0	A2	Analog Output	Channel 0 Current Reference. Connect a TBD ohm resistor from IREF to ground.
DL_I_P_1	B1	Analog Output	I current Output for Channel 1
DL_I_N_1	B2	Analog Output	I current Output for Channel 1
DL_Q_P_1	C2	Analog Output	Q current Output for Channel 1
DL_Q_N_1	C1	Analog Output	Q current Output for Channel 1
DL_IREF_1	A1	Analog Output	Channel 1 Current Reference. Connect a TBD ohm resistor from IREF to ground.
DL_I_P_2	D1	Analog Output	I current Output for Channel 2
DL_I_N_2	D2	Analog Output	I current Output for Channel 2
DL_Q_P_2	E2	Analog Output	Q current Output for Channel 2
DL_Q_N_2	E1	Analog Output	Q current Output for Channel 2
DL_IREF_2	F3	Analog Output	Channel 2 Current Reference. Connect a TBD ohm resistor from IREF to ground.
DL_I_P_3	F1	Analog Output	I current Output for Channel 3
DL_I_N_3	F2	Analog Output	I current Output for Channel 3
DL_Q_P_3	G2	Analog Output	Q current Output for Channel 3

PIN Name	Ball #	I/O	Description
DL_Q_N_3	G1	Analog Output	Q current Output for Channel 3
DL_IREF_3	G3	Analog Output	Channel 3 Current Reference. Connect a TBD ohm resistor from IREF to ground
ANL_AUX_0	A7	Analog Input	RSSI Detect input signal, see Table 24 for analog characteristics.
ANL_AUX_1	B7	Analog Input	Reserved for future use

Table 7: RFIC Digital Interface Pins

PIN Name	Ball #	I/O	Description
RF_LD	A10	Input	RFIC Lock-Detect Digital Output of Frequency Synthesizer
PA_ENABLE	A9	Output	Power Amplifier Enable/Disable (high for enable)
RFSPI_CLK	A11	Output	RF SPI Clock Output
RFSPI_CS	B10	Output	RF SPI Chip-Select.
RFSPI_DOUT	C10	Output	RF SPI Data Output
UL_ANT_SEL_N	B9	Output	UL Antenna Diversity Switch control - negative
UL_ANT_SEL_P	C9	Output	UL Antenna Diversity Switch control - positive
CLK_IN	A8	Input	RF 40 MHz Clock Input

2.7 Sample On Reset Pins

Several pins are used for chip configuration and are sampled on reset. Immediately after the reset, these pins are returned to normal operation mode. The board design should allow both pull-up and pull-down options.

Table 8: Sample On Reset Pins

PIN Name	Ball #	I/O	Description
CFG_0			
CFG_1			
CFG_2			
CFG_3			
CFG_4			
CFG_5			
CFG_6			
CFG_7			
CFG_8			
CFG_9			

2.8 Power and Ground Pins

Table 9: Power and Ground Pins

PIN Name	Ball #	I/O	Description
AVDD1_0	E3, D5, C7	Analog Power	1.0 V Analog power supply
AVDD3_3	C3, C6	Analog Power	3.3 V Analog power supply
AGND	D3, D4, C5, D6, D7	Analog Ground	Analog ground
VDD1_0	D9, E9, F4, F10, G10, H4, J5, J6, J8, J9, C8	Digital Power	1.0 V core power supply pins
VDD_IO_3_3	D10, E10, H7, H10, J4, J7, J10,B8	Digital Power	3.3 V I/O power supply pins
DGND	E5, E6, E7, E8, F5, F6, F7, F8, F9, G4, G5, G6, G7, G8, G9, H5, H6, H8, H9,D8	Digital Ground	Digital Ground
AVDD_POR	H2	Power	Dedicated power supply pin for Power-On-Reset circuit. Connect to 3.3 V power supply
AGND_POR	H1	Ground	Dedicated ground pin for Power-On-Reset circuit

2.9 Test and Not Connected Pins

Table 10: Test and N.C. Pins

PIN Name	Ball #	I/O	Description
VBG	C4	I/O	Band gap voltage
AMN_TST0	J3	I/O	Reserved for internal testing, connect to ground
AMN_TST1	K3	I/O	
AMN_TST2	K2	I/O	
AMN_TST3	K1	I/O	
AMN_TST4	E4	I/O	

Table 11: Non Volatile Memory Pins

PIN Name	Ball #	I/O	Description
VREF_NVM	H3	Power	
VPP_NVM	J1	Power	High voltage for NVM programming. Connect to ground on the

PIN Name	Ball #	I/O	Description
			product board

Chapter 3

Functional Description

3.1 Functional Description

The AMN212X provides a WHDI transmitter baseband solution receiving digital HD video and audio from a source device and transmits it wirelessly through two or four RF channels. It also receives wireless upstream control and data channel, which can be output to the application via the standard digital control channel. Control and communication with external entities is performed by the embedded M4K MIPS processor. In addition to the main functionality, the chip enables various calibration loops to improve overall RF performance.

Figure 3 below shows the functional blocks of the chip.

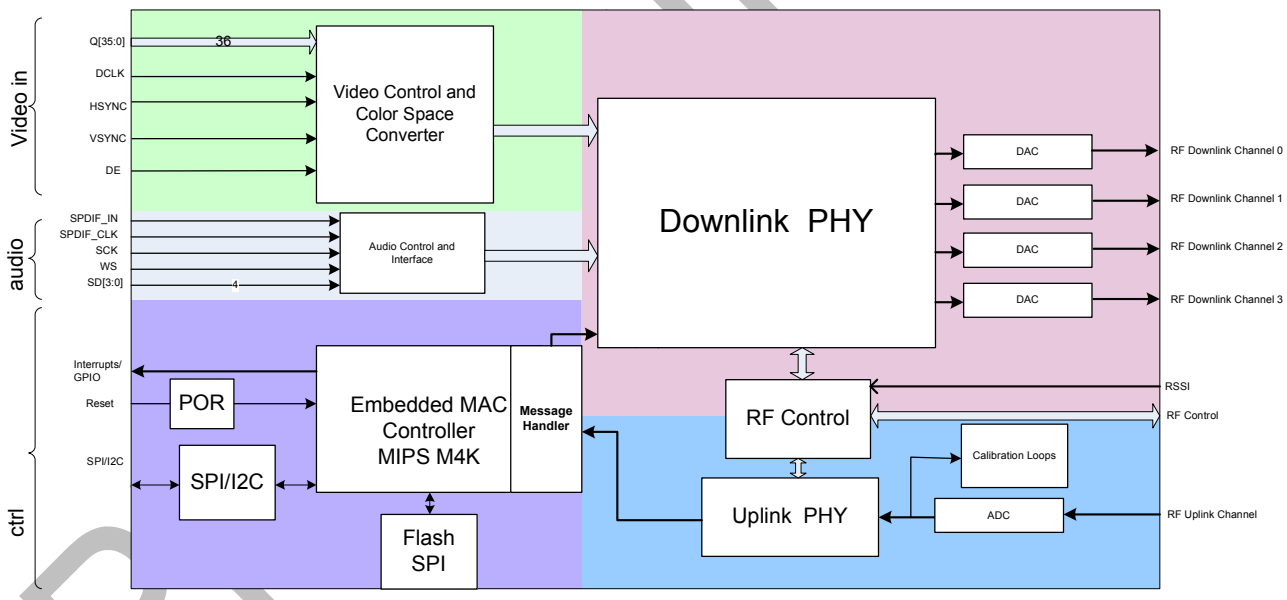

Figure 3: Functional Block Diagram

The entire chip configuration and control is managed by an embedded MIPS M4K microcontroller for which AMIMON supplies the FW code. The code is located on the external flash which is loaded to the on-chip RAM upon power up. This system level solution enables easy integration into source devices with minimum adjustments. A control interface enables communication with the external application microcontroller for user dependent features. For system level management and details regarding the interface with the embedded MAC, please refer to the appropriate AMIMON documentation.

Chapter 4

Interfaces

This chapter describes the interfaces of the AMN212X and provides examples of how to use them.

4.1 Video Data Input and Conversions

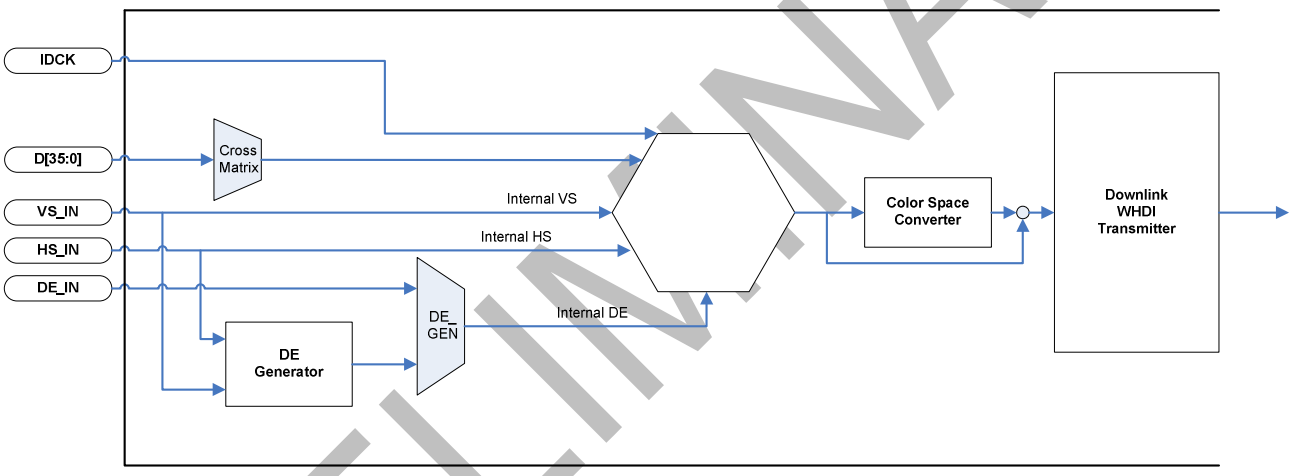

Figure 4: Video Data Processing Path

Figure 4 shows the stages for processing video data through the AMN212X. The HSYNC and the VSYNC input signals are mandatory. The DE input signal is optional and can be created with the DE generator using the HSYNC and the VSYNC pulses.

The video input data is uncompressed digital video up to 3*12 bits in width. The AMN212X enables the multiplexing of any video bit to any other video bit in order to ease the routing constraint of the PCB solution.

Important: *For default configuration of video interface configuration, when connected to a 3*8 or 3*10-bits source, connect the appropriate LSBs to the GND.*

The video interface provides a direct connection to the outputs from the video source device, HDMI receiver or any other video interface device. The appropriate registers must be configured to describe which video format type to input into the AMN212X. (Refer to the appropriate programmer's reference guide for more details.)

DDR

The AMN212X enables dual data rate, meaning that the video bus is sampled on both rising and falling clock edges. This enables halving the speed of the pixel clock in order to reduce high speed signal risks.

Optional Interlacer

The AMN212X includes logic for converting a progressive video stream into an interlaced video stream. This feature can be used in the case of an incoming high speed signal when there are no available 40 MHz channels.

DATA Enable (DE) Generator

The AMN212X includes logic for constructing the DE signal from the incoming HSYNC, VSYNC and clock. Registers are programmed to enable the DE signal to define the size of the active display region.

Color Space Converter

The AMN212X can receive either RGB or YCbCr color space. For more details, you may refer to the MAC Programmer's Reference Guide.

Common Video Input Format

Table 12 below describes the common supported video input resolutions.

Table 12: Supported Video Input Resolutions

Color Space	Video Format	Bus Width	Input Pixel Clock (MHz)						
			480i	480p	XGA	720p	1080i	1080p*	UGA*
RGB/YCbCr	4:4:4	24	27	27	65	74.25	74.25	148.5	162
RGB/YCbCr	4:4:4	30	27	27	65	74.25	74.25	148.5	162
RGB/YCbCr	4:4:4	36	27	27	65	74.25	74.25	148.5	162
YCbCr	4:2:2	24	27	27		74.25	74.25	148.5	

*Supported by AMN2120 and AMN2122 only

Video Channel Mapping

The 36-bit video input signals are mapped to the RGB and YCbCr color space according to the internal programmable switch matrix configuration. The default configuration is shown below:

Table 13: Video Channel Mapping

Data Line	RGB 36 bit	YCbCr 4:4:4 36 bit	YCbCr 4:2:2 24 bit
D0	B0	CB0	C0
D1	B1	CB1	C1
D2	B2	CB2	C2
D3	B3	CB3	C3
D4	B4	CB4	C4

Data Line	RGB 36 bit	YCbCr 4:4:4 36 bit	YCbCr 4:2:2 24 bit
D5	B5	CB5	C5
D6	B6	CB6	C6
D7	B7	CB7	C7
D8	B8	CB8	C8
D9	B9	CB9	C9
D10	B10	CB10	C10
D11	B11	CB11	C11
D12	G0	Y0	Y0
D13	G1	Y1	Y1
D14	G2	Y2	Y2
D15	G3	Y3	Y3
D16	G4	Y4	Y4
D17	G5	Y5	Y5
D18	G6	Y6	Y6
D19	G7	Y7	Y7
D20	G8	Y8	Y8
D21	G9	Y9	Y9
D22	G10	Y10	Y10
D23	G11	Y11	Y11
D24	R0	CR0	N.U.
D25	R1	CR1	N.U.
D26	R2	CR2	N.U.
D27	R3	CR3	N.U.
D28	R4	CR4	N.U.
D29	R5	CR5	N.U.
D30	R6	CR6	N.U.
D31	R7	CR7	N.U.
D32	R8	CR8	N.U.
D33	R9	CR9	N.U.
D34	R10	CR10	N.U.
D35	R11	CR11	N.U.

In order to change the video channel mapping, please refer to the appropriate programmer's reference guide.

4.1.1 Video Interface Input Timing Diagram

4.1.1.1 Timing Requirements

Table 14: Video Interface*

Symbol	Parameter	MIN	TYP	MAX AMN2123	MAX AMN2120 AMN2122	Units
T_{DCKCYC}	DCLK period	12.5		74.1	6.17	ns
$T_{DCKFREQ}$	DCLK frequency	13.5		80	162	MHz
$T_{DCKDUTY}$	DCLK duty cycle	40%		60%		ns
T_{DCKSUR}	Setup time to DCLK rising edge	0.7				ns
T_{DCKHDR}	Hold time to DCLK rising edge	1.1				ns
T_{DCKSUF}	Setup time to DCLK falling edge	1.5				ns
T_{DCKHDF}	Hold time to DCLK falling edge	0.5				ns

*The data presented in this table is preliminary and subject to change.

4.1.1.2 Timing Diagram

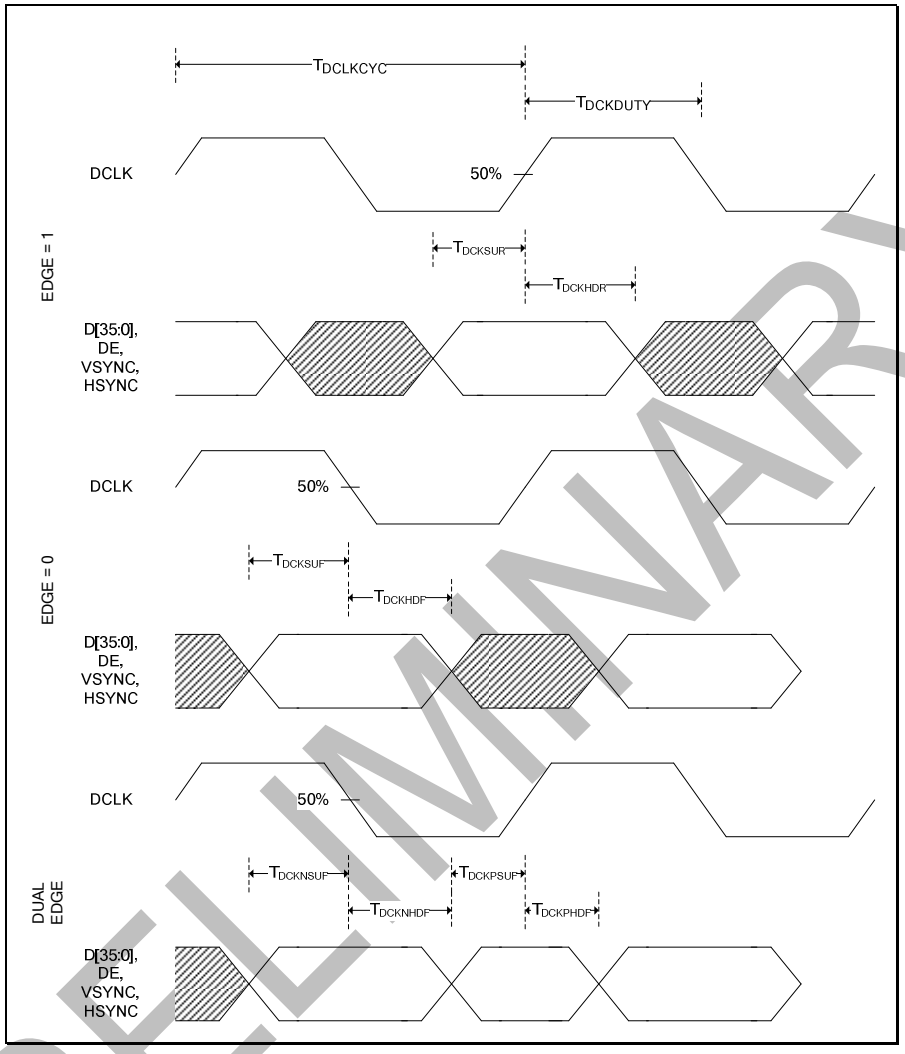

Figure 5: Timing Diagram

4.2 Audio Data Capture

AMN212X transports an explicit audio master clock with the appropriate data over the wireless link. No constraints exist for a coherent video and audio clock, where coherent means that the audio and the video clock must have been created from the same clock source. The AMN212X can accept digital audio from either SPDIF or I2S inputs. The AMN212X supports up to four synchronized IIS channels (each channel is composed of two audio streams) with sampling frequencies of up to 192 KHz and up to 32 bits per sample.

Audio Signal Down-sampling

The audio signal can be down-sampled by the factor 2 or 4 to reduce the required bandwidth in the case of a lack of an available 40 MHz channel.

Audio Channel Mapping

The AMN212X enables the selection and multiplexing of any I2S input channel to any audio channel.

4.2.1 I2S Bus Specification

The AMN212X supports a standardized communication structure inter-IC sound (I^2S) bus. As shown in Figure 6, the bus has three lines: continuous serial clock (SCK), word select (WS) and four serial data lines (SD). The external audio source device generates SCK and WS.

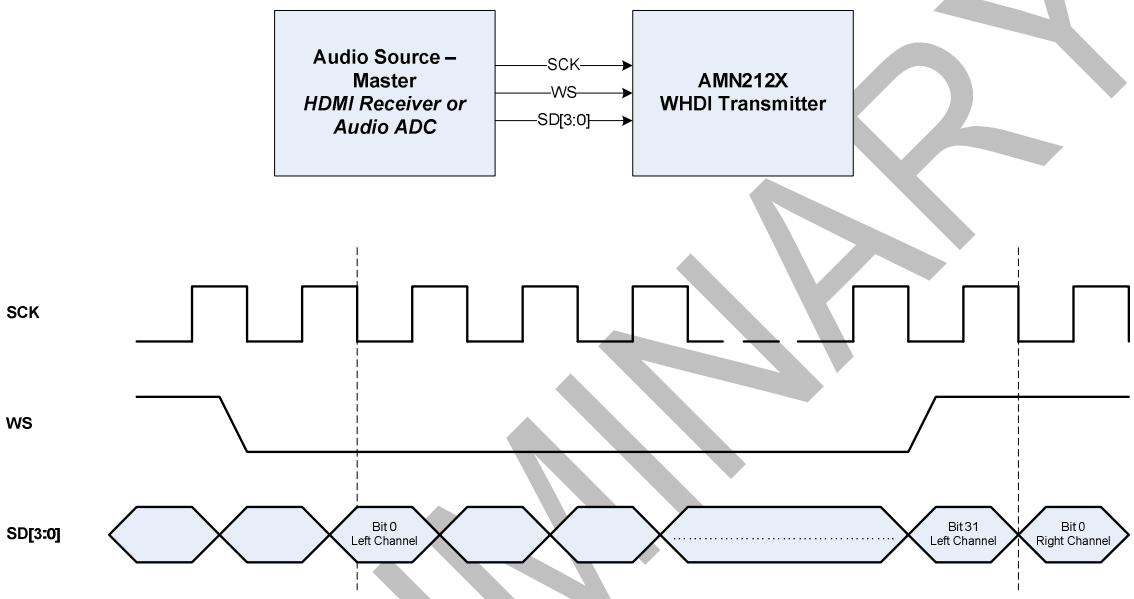

Figure 6: I^2S Simple System Configurations and Basic Interface Timing

The AMN212X supports an I^2S format of up to 32 bits for each channel (left and right). The serial data is latched into the AMN212X on the leading (LOW to HIGH) edge of the clock signal. The WS is also latched on the leading edge of the clock signal. The WS line must change one clock period before the first bit of the channel is transmitted.

The AMN212X transmits explicit clock SD and WS and does not process the audio content. The AMN212X includes an interleaver and RS encoder that operates on the audio samples to improve audio performance. The input audio at the transmitter end is mirrored to the receiver end. The source may have different word lengths of up to 32 bits. However, the AMN212X always samples and transmits 24 bits or 16 bits over the wireless link.

4.2.1.1 Timing Requirements

Table 15: I2S Audio Interface Timing Requirements

Symbol	Parameter	MIN	TYP	MAX	Units
T_{SCKCYC}	SCK period	325		81.38	ns
$T_{SCKFREQ}$	SCK frequency	1.024		12.288	MHz
$T_{SCKDUTY}$	SCK duty cycle	40		60	%
$T_{SCKSETUP}$	Setup time to SCK rising edge	25			ns
$T_{SCKHOLD}$	Hold time to SCK rising edge	25			ns

*The data presented in this table is preliminary and subject to change.

4.2.1.2 Timing Diagram

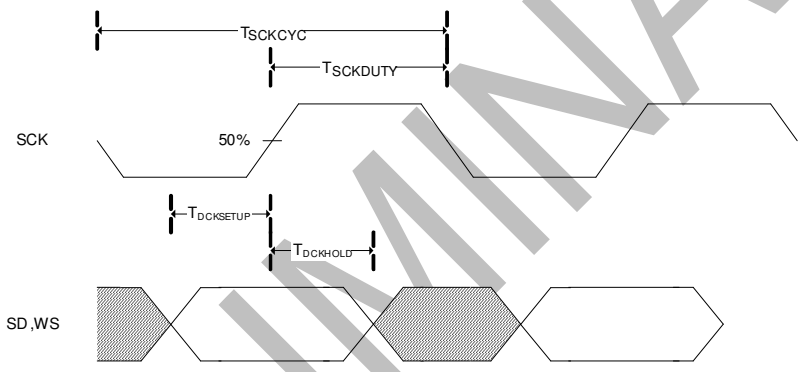

Figure 7: I²S Input Timings

4.2.2 S/PDIF Bus

4.2.2.1 Timing Requirements

The AMN212X does not require the SPDIF clock. The clock is produced internally by sampling the SPDIF data input at a high clock rate and processing it.

Table 16: Audio Interface Timing Requirements

Symbol	Parameter	Condition	MIN	TYP	MAX	Units
T_{SPCYC}	SPDIF data sampling rate		162		488	ns
T_{SPFREQ}	SPDIF data sampling frequency		2.048		6.144	MHz

*The data in this table is preliminary.

4.3 Application Microcontroller Interface

The AMN212X supports two possible interfaces to communicate with an external application microcontroller, over SPI or a Two-wire Bus. The SPI is used when the application requires a high speed interface to the AMN212X and the I2C is used for legacy devices and is compatible with the AMN11100/AMN12100 two-wire interface specification.

4.3.1 Application SPI

4.3.1.1 Clock Specification

The clock rate is provided by the master and must not exceed 20 MHz during the normal operation mode. When the system is in deep standby mode, meaning when it is waiting for a wake-up from an application, the maximum supported clock rate is 1 MHz.

The required clock duty cycle is 40-60 for active clock cycles. The clock can be stopped for TBD time.

4.3.1.2 Transaction Start and Stop

The transaction is started when the APP_SPI_SS is pulled low. After $T_{SS\_ACT\_CLK}$ ns, the first data bit may be sampled, as shown below:

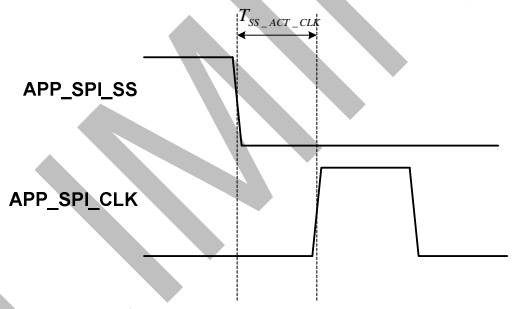

Figure 8: Timing of the SS Start to the First Active Clock

The transaction is ended when the APP_SPI_SS is pulled high, after the last bit of the transaction is sampled by the master after $T_{SS\_NACT\_CLK}$, as shown below:

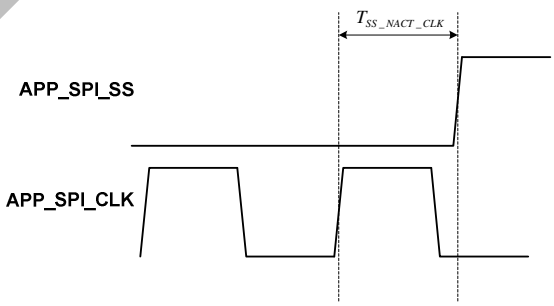

Figure 9: Timing of the SS End to the Last Active Clock

4.3.1.3 Data Sampling

The data must be stable on each rising edge of the clock, as shown below:

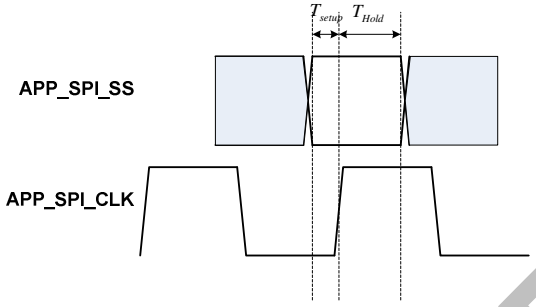

Figure 10: Timing of the Data Sampling

The following table provides a summary of the timing requirements of the interface:

Table 17: APP-MAC Timing

Symbol	Normal Mode			Sleep Mode			Units	Remarks
	MIN	TYP	MAX	MIN	TYP	MAX		
T_{CLK}	-	50	25		1000		ns	
T_{HOLD}								
T_{SU}								
$T_{SS\_ACT\_CLK}$	25		-		500		ns	There is no maximum limit
$T_{SS\_NACT\_CLK}$	40				700		ns	

4.3.1.4 Data Alignment

The communication between the MAC and the application is byte aligned, meaning that the transaction length is an integer multiplication of 8 bits. The data is always transmitted when the most significant bit is sent first, as shown below:

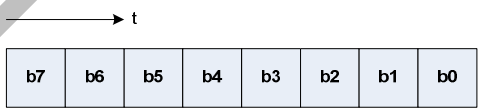

Figure 11: Bit Alignment

The bit count must be reset when the new transaction is started. In case of an illegal transaction, the appropriate interrupt is set.

4.3.1.5 Protocol General Structure

The general structure of a SPI transaction is comprised of a command, address and data which are sent in this order. The command is one byte that specifies the type of the transaction. The supported commands are as shown below:

Table 18: APP-MAC Timing

Command Code	Command Name	Explanation
0x01	WRITE	Write Transaction: Followed by an address and the data. See section *4.3.1.7 Write Transactions* for details.
0x11	READ	Read Transaction: Followed by an address and the response data from the slave. See section *4.3.1.8 Read Transactions* for details.
0x22	**TEST**	Test Transaction: Followed by the response data from the slave.

4.3.1.6 Start Condition

The master must not issue any transaction until the slave drives the WHDI interrupt to the active state.

4.3.1.7 Write Transactions

As previously mentioned, each write transaction is started with the WRITE command, followed by a 2 byte address (the least significant byte is sent first) and by N bytes of data. N is a function of the address and therefore there is no length field. After the mandatory fields are sent, the master continues to toggle the clock and keep the slave select low. When the slave processes the transaction it must respond with the ACK or NACK code.

- ACK – 0xAA
- NACK – 0xBB

After the master receives the response, the transaction can be completed. The master must process the response to determine whether the transaction must be repeated.

If the slave did not responded within the $T_{WR,TIMEOUT}$, the transaction is considered to be lost. The following diagram shows the successful write transaction:

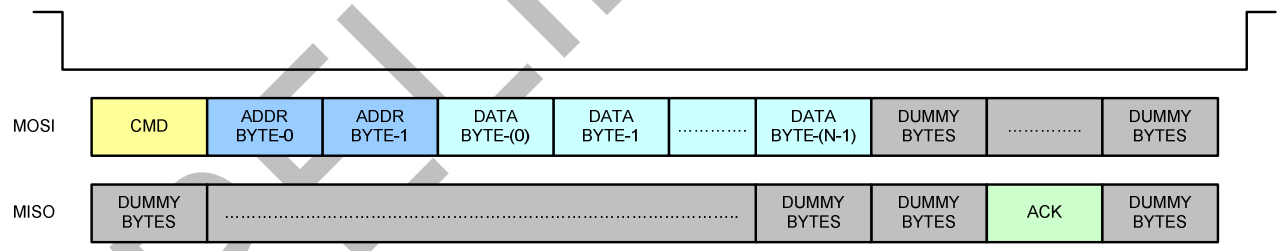

Figure 12: Write Transaction

4.3.1.8 Read Transactions

As mentioned before, each read transaction is started with the READ command, followed by a 2 byte address (the least significant byte is sent first) written by the master. The slave must respond with N bytes of data. The N is a function of the address and therefore there is no length field. The slave is not required to send the response immediately. However, once the response is started, the transaction cannot be stopped. When the response is not ready, the slave sends dummy bytes with the value of 0x00. The first byte of the transaction is the constant byte of ACK with the value 0xAA and only after this is the read data sent. After the master receives the response, the transaction can be completed. The master must process the response to determine whether the transaction must be repeated.

If the slave does not responded within the $T_{RD,TIMEOUT}$, the transaction is considered to be lost. The following diagram shows the successful read transaction:

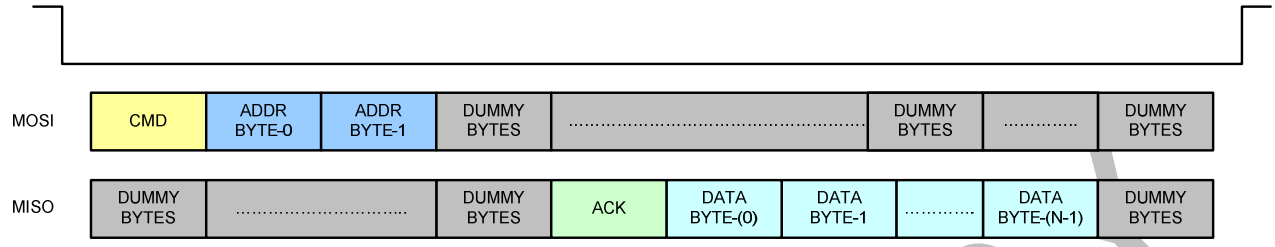

Figure 13: Read Transaction

4.3.1.9 Test Transaction

This transaction must be initiated by the application to ensure that the MAC is up and running. The master (application) sends one byte and waits for the response or timeout $T_{TST,TIMEOUT}$.

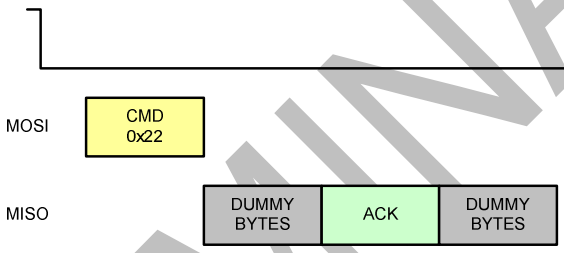

Figure 14: Test Transaction

4.3.1.10 Timing Constraints

The following table summarizes the constraints of protocol timing:

Table 19: APP-MAC Timing

Symbol	Normal Mode			Units	Remarks
	MIN	TYP	MAX		
$T_{TST,TIMEOUT}$		100		ms	
$T_{RD,TIMEOUT}$		100		ms	
$T_{WR,TIMEOUT}$		100		ms	

4.3.2 Application Two-wire Interface

The AMN212X devices support a Two-Wire Interface that behaves in a similar manner to the AMN11100/AMN12100. Please refer to the appropriate AMIMON documentation for further details.

4.3.3 Interrupts

The AMN212X devices have one mandatory interrupt which is mapped to the GPIOXXXX. The interrupt is used to indicate events to the application microcontroller. The polarity of the application interrupt is configurable in the MAC software. Please refer to the programmer guide for details.

Additionally, any GPIO port can be configured to be an interrupt towards an AMN212X embedded microcontroller to enable future enhancements of the system solution.

4.4 Serial Flash Interface

The AMN212X embedded MAC contains a ROM with the basic drivers and boot-loader. The rest of the code and data is located on the external serial flash. The AMN212X supports the following serial flashes:

Table 20: Supported Flashes

Manufacturer	Numonyx (former ST)	Atmel	Spansion (former AMD)	Macronix
Part number	M25PE40	AT25DF041A	S25FL040A	MX25L4005A
Density	4M bit	4M bit	4M bit	4M bit

For any other flash devices which are not specified above please contact AMIMON.

4.5 General Two-wire Master Interface

The AMN212X includes an additional two-wire interface when the AMN212X is a master on the interface. This interface is used for future enhancements and cost reduction of the entire system. For example direct control of the video/audio peripherals, EEPROM configuration and so on.

4.6 Reset Schema

The AMN212X includes a POR circuit that enables the devices to operate without external reset upon power up. However, the AMN212X also has an external $\overline{RESET}$ pin to enable the external application to reset the device.

The POR is designed to generate a reset pulse when the 3.3 V power supply reaches 2.7 V level. The $\overline{RESET}$ can be issued without any conditions and must be at least 100 ns.

When the device is reset, the AMN212X embedded MAC starts to fetch the code from the external flash and to initialize the device for operation.

Chapter 5

Electrical Specifications

5.1 Operating Conditions and Electrical Characteristics

The following tables describe the operating conditions and electrical characteristics required for working with the AMN2120, AMN2122 and AMN2123 devices.

Table 21: Absolute Maximum Ratings over Operating Ambient Temperature Range

Supply Input-voltage range, V_I	0 to 4 V
Ambient temperature range	
Storage temperature range, Tstg	-55°C to 150°C

Table 22: Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Core supply voltage		1.0		V
$V_{DD}IO$	IO supply voltage		3.3		V
P_V_{DD}	Core supply power consumption during video transmission				mW
$P\_V_{DD}IO$	IO supply power consumption during video transmission				mW
$P\_V_{DD}\_off$	Core supply power consumption during the off state				mW
$P\_V_{DD}IO\_$ off	IO supply power consumption during the off state				mW
$P\_V_{DD\_stdby}$	Core supply power consumption during video transmission				mW
$P\_V_{DD}IO\_$ stdby	IO supply power consumption during video transmission				mW
V_{SS}	Supply ground	0			V
V_{IH}	High-level input voltage	0.7 $V_{DD}IO$			V
V_{IL}	Low-level input voltage			0.3 $V_{DD}IO$	V
V_{OH}	High-level output voltage (DV_{DD} = MIN, I_{OH} = MAX)	0.8 $V_{DD}IO$			V
V_{OL}	Low-level output voltage (DV_{DD} = MIN, I_{OL} = MAX)			0.22 $V_{DD}IO$	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
T_j	Operating junction temperature – AMN2120				°C
	Operating junction temperature – AMN2122				
	Operating junction temperature – AMN2122				

Table 23: Electrical Characteristics over Recommended Range of Supply Voltage and Operating Conditions

Parameter		Test Conditions	MIN	TYP	MAX	Unit
I_I	Input current	$V_I = V_{SS}$ to $V_{DD}IO$			±20	µA
I_{OZ}	Off-state output current	$V_O = V_{DD}IO$ or 0 V			±20	µA
C_i	Input capacitance				10	pF
C_o	Output capacitance				10	pF

Table 24: Analog Front End Electrical Characteristics

Ball Number	Ball function	Characteristics	MIN	TYP	MAX	Unit
	RSSI_DETECT	Input voltage range	0		2	V
		Input impedance (not including IO pad)			0.5	pF
		Input resistance	10			Kohm
	I/Q outputs	Full scale output current		10		mA
		Single-ended output compliance range	0	0.5	1	V
		Differential output swing	0.8	1	1.5	Vpp
		Output resistance	100			Kohm
		Output capacitance		0.3	0.32	pF
	I/Q inputs	Input differential voltage range	±679	±697	±715	mV
		Input common mode voltage	0.6		1.65	V
		Input differential impedance		5.6 Kohm/ 50 fF		

Chapter 6

Marking and Mechanical Specifications

This chapter describes the mechanical specifications of the AMN2120, AMN2122 and AMN2123.

6.1 Package Marking Specifications

Figure 15: AMN2110 Package Marking

Manufacturer Name	AMIMON
Device Name	TX – AMN2120/2/3
Package Type	13x13 169 Ball L-BGA
Line Number:	**Description**
Line 1	AMIMON logo – Fixed
Line 2	TX – AMN2120/2/3 Ax – Fixed (Device name and revision)

Line 3	LLLLLL – Variable (wafer lot number)
Line 4	YY – Variable (year of molding) WW – Variable (week of molding)

6.2 169 Balls 13x13 LBGA

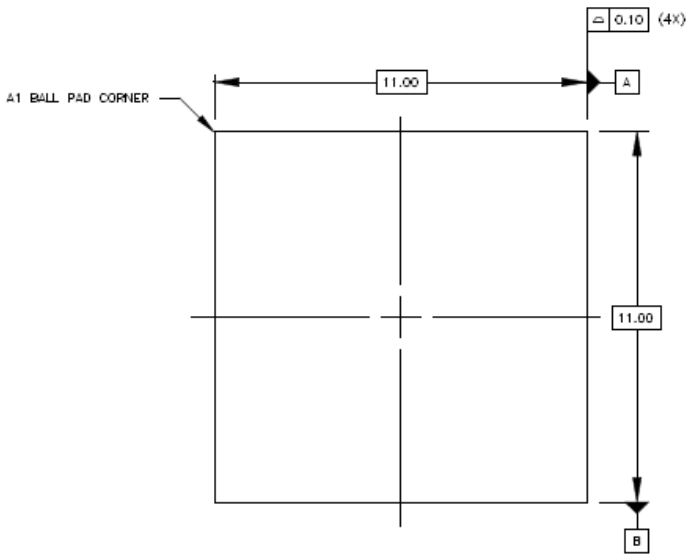

Figure 16: AMN2120/2/3 Package – Top View

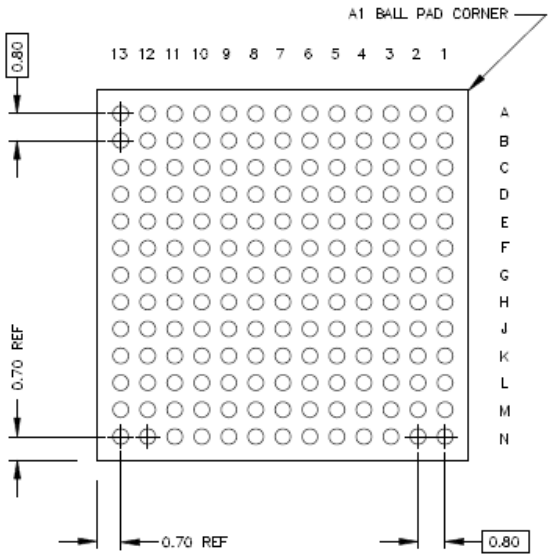

Figure 17: AMN2120/2/3 Package – Bottom View

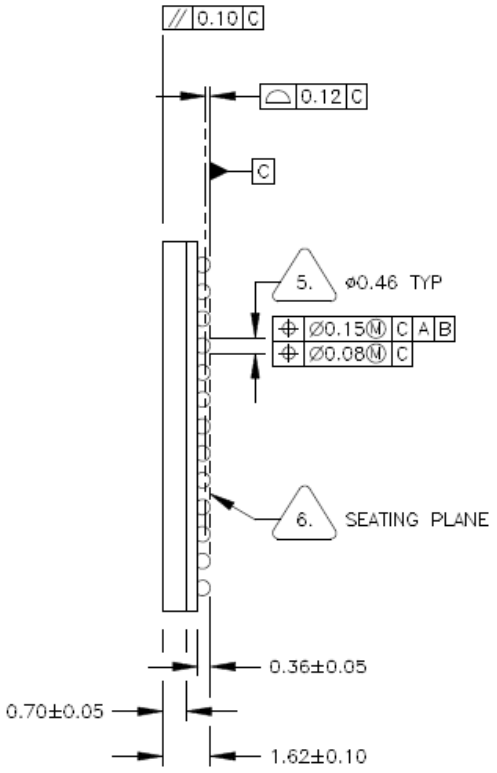

Figure 18: AMN2120/2/3 Package – Side View

Notes:

1. All dimensions are in millimeters.