

N-CH100V Fast Switching MOSFETs

❖ GENERAL DESCRIPTION

The AMS0026 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The AMS0026 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

FEATURES

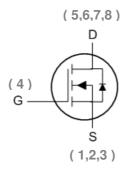
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Product Summery

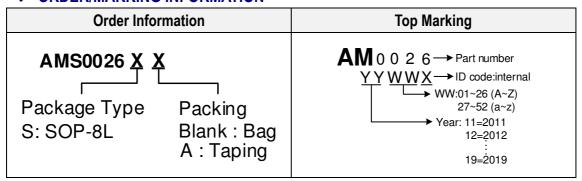
BVDSS	RDSON	ID
100V	$20 m\Omega$	7.5A

SOP8 Pin configuration





❖ ORDER/MARKING INFORMATION



❖ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current, V _{GS} @ 10V (Note 1)	I _D @T _A =25°C	7.5	Α
Continuous Drain Current, V _{GS} @ 10V (Note 1)	I _D @T _A =70°C	6	Α
Pulsed Drain Current (Note 2)	I _{DM}	40	Α
Single Pulse Avalanche Energy (Note 3)	EAS	16	mJ
Avalanche Current	I _{AS}	18	Α
Total Power Dissipation (Note 4)	P _D @T _A =25°C	2.5	W
Storage Temperature Range	T _{STG}	-55 to 150	°C
Operating Junction Temperature Range	TJ	-55 to 150	°C
Thermal Resistance Junction-ambient (Note 1) (t≤10S)	D	50	°C/W
Thermal Resistance Junction-ambient (Note 1) (Steady State)	$R_{\theta JA}$	85	°C/W

- Note 1: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- Note 2: The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
- Note 3: The EAS data shows Max. rating . The test condition is V_{DD} =25V, V_{GS} =10V, L=0.1mH
- Note 4: The power dissipation is limited by 150°C junction temperature
- Note 5: The Min. value is 100% EAS tested guarantee.
- Note 6: The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

*** ELECTRICAL CHARACTERISTICS**

(T_J=25 °C, unless otherwise noted)

Characteristics	Symbol	Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V_{GS} =0V , I_D =250uA	100	-	-	V
BVDSS Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA	-	0.098	-	V/°C
Static Drain-Source	Daggan	V_{GS} =10V , I_D =7A	-	16	20	mΩ
On-Resistance (Note 2)	INDS(ON)	$R_{DS(ON)}$ $V_{GS}=4.5V$, $I_D=5A$		19	25	11122
Gate Threshold Voltage	$V_{GS(th)}$	V _{GS} =V _{DS} , I _D =250uA		-	2.5	V
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}$			-5.5	-	mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =80V , V _{GS} =0V , T _J =25°C	-	-	10	uA
Brain-Source Leakage Gurrent		V _{DS} =80V , V _{GS} =0V , T _J =55°C	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V_{GS} =±20V , V_{DS} =0V	-	-	±100	
Forward Transconductance	gfs	V_{DS} =5 V , I_{D} =7 A	-	24	-	S
Gate Resistance	R_g	V_{DS} =0V , V_{GS} =0V , f=1MHz	-	1.6	-	Ω
Total Gate Charge (10V)	Q_g	-V _{DS} =80V , V _{GS} =10V , -I _D =7A		36	-	nC
Gate-Source Charge	Q_gs			95	-	
Gate-Drain Charge	Q_gd			10	-	
Turn-On Delay Time	$T_{d(on)}$			11.5	ı	
Rise Time	Tr	V _{DD} =50V , V _{GS} =10V,	-	29	ı	ns
Turn-Off Delay Time	$T_{d(off)}$	$R_G=3.3\Omega$, $I_D=7A$		42	ı	115
Fall Time	T _f			18	-	
Input Capacitance	C _{iss}	V_{DS} =15V , V_{GS} =0V , R_{G} =3.3 Ω , f=1MHz		1930	1	pF
Output Capacitance	Coss			245	-	
Reverse Transfer Capacitance	C_{rss}			125	1	
Diode Characteristics						
Continuous Source Current (Note 1, 6)	I _S	\\ _\\ _\\	ı	ı	7	Α
Pulsed Source Current (Note 2, 6)	I _{SM}	V _G =V _D =0V , Force Current		-	40	Α
Diode Forward Voltage (Note 2)	V_{SD}	V _{GS} =0V , I _S =1A , T _J =25°C	-	-	1.2	V
Reverse Recovery Time	t _{rr}	I _F =7A , dI/dt=100A/μs ,	-	48	-	nS
Reverse Recovery Charge	Qrr	T _J =25°C		29	-	nC

Note 1: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

Note 2: The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%

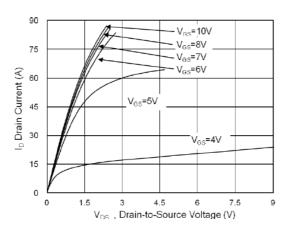
Note 3: The EAS data shows Max. rating . The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH

Note 4: The power dissipation is limited by 150°C junction temperature

Note 5: The Min. value is 100% EAS tested guarantee.

Note 6: The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

*** TYPICAL CHARACTERISTICS**



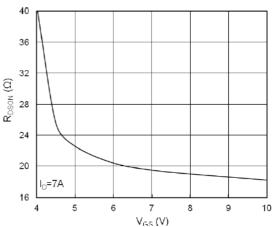


Fig.1 Typical Output Characteristics

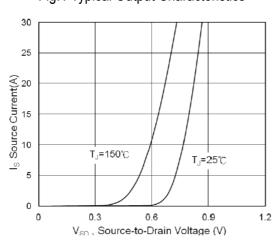


Fig.2 On-Resistance vs. Gate-Source

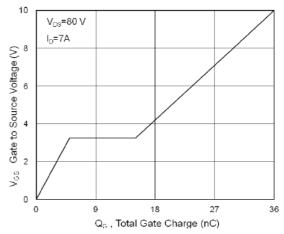


Fig.3 Forward Characteristics Of Reverse

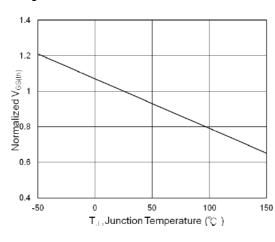


Fig.4 Gate-Charge Characteristics

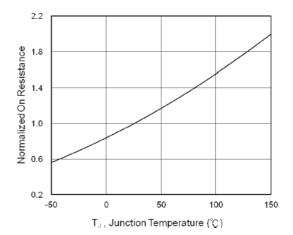
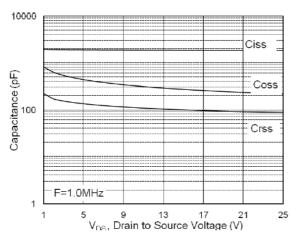


Fig.5 Normalized V_{GS(th)} vs. T_J

Fig.6 Normalized R_{DSON} vs. T_J



TYPICAL CHARACTERISTICS (COUNTINOUS)



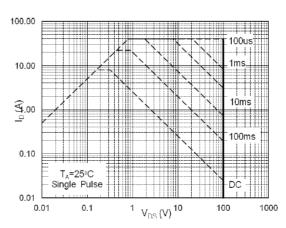


Fig.7 Capacitance

Fig.8 Safe Operating Area

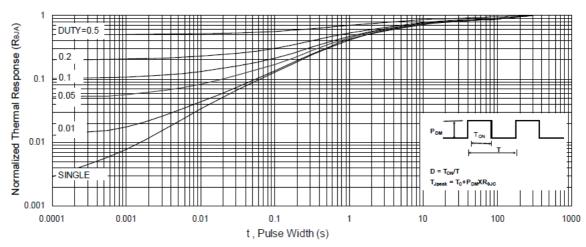
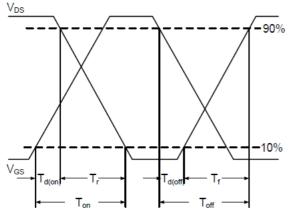
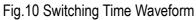


Fig.9 Normalized Maximum Transient Thermal Impedance





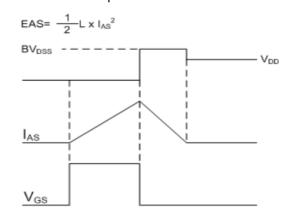


Fig.11 Unclamped Inductive Switching Waveform