Surface Mount Assembly and Handling of ANADIGICS LPCC Packages

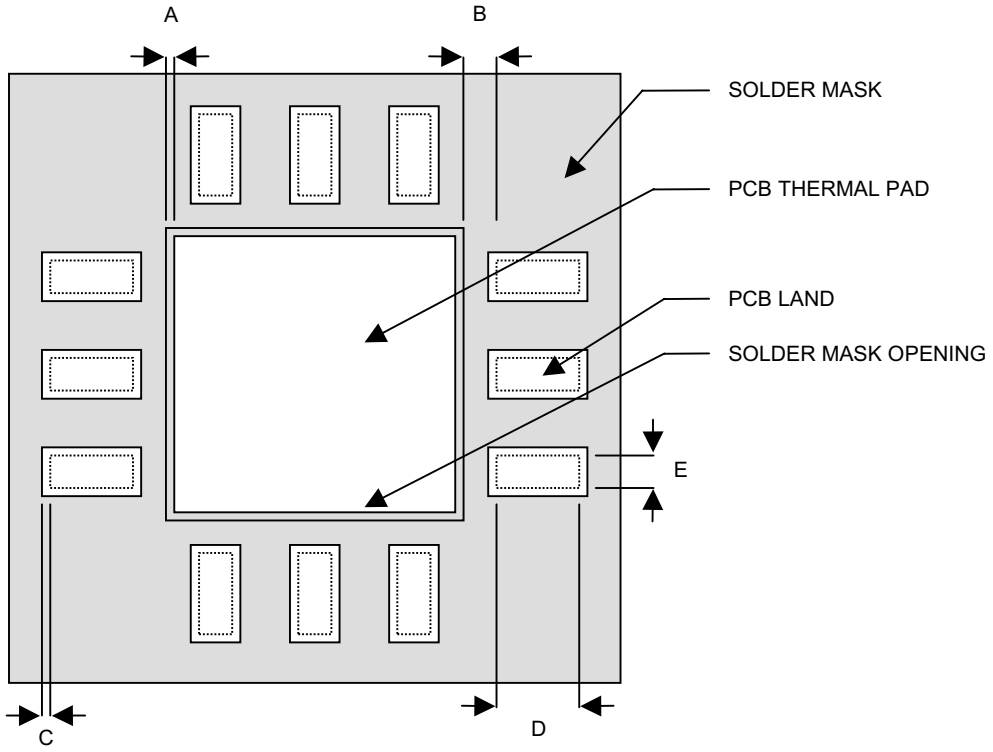
1.0 Overview

ANADIGICS power amplifiers are typically packaged in a Leadless Plastic Chip Carrier (LPCC) package. These LPCC packages have two types of pads, mounting pads and a thermal pad, both of which must be correctly soldered for proper electrical contact to the PCB. The appropriate steps should be taken during PCB design and assembly to guarantee optimum performance from the power amplifiers. This application note outlines the steps necessary for the handling and assembly of ANADIGICS power amplifiers.

2.0 Requirements

2.1 PCB Design Guidelines:

1. PCB land and solder masking recommendations are shown in Figure 1.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads
D = PCB land length = LPCC solder pad length + 0.1mm
E = PCB land width = LPCC solder pad width

Figure 1. PCB Land and Solder Mask Recommendations.

2. Plated-Through Holes or vias **should not** be used in the **mounting pads** for the IC circuit connections.
3. Thermal vias **should** be used on the **PCB thermal pad** (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
4. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.
5. For best thermal performance, provision should be made to provide a thermal path from the reverse side ground plane to an external heat sink.

2.2 Package Handling

1. ESD precautions must be observed at all times when handling these packages.
2. Packages should be used in accordance with their MSL (Moisture Sensitivity Level) rating found on the device datasheet.
3. MSL-3 packages should be used 168 hours after they have been removed from the sealed moisture barrier bag. After 168 hours, packages should be baked for 24 hours at 125 °C before usage or resealing in a sealed moisture barrier bag.
4. MSL-2 packages have a lifespan of 12 months after they have been removed from a sealed moisture barrier bag, after which they must be baked as above before usage.
5. MSL-1 packages have an infinite lifespan after initial baking in the factory.

3.0 Assembly Process

3.1 Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the LPCC thermal pad area as shown in Figure 2.
4. The aperture opening for the signal pads should be between 50-80% of the LPCC pad area as shown in Figure 3.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within $\pm$ 1 mil prior to application of the solder paste.
7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

3.2 Soldering Options & Package Placement

1. **Hand soldering of these devices is not recommended even for prototypes.**
2. Infrared or Convection mass reflow soldering is the preferred method of LPCC attachment.

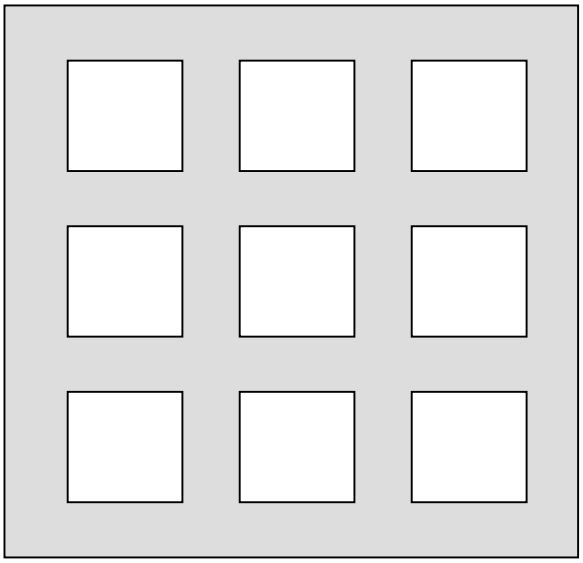
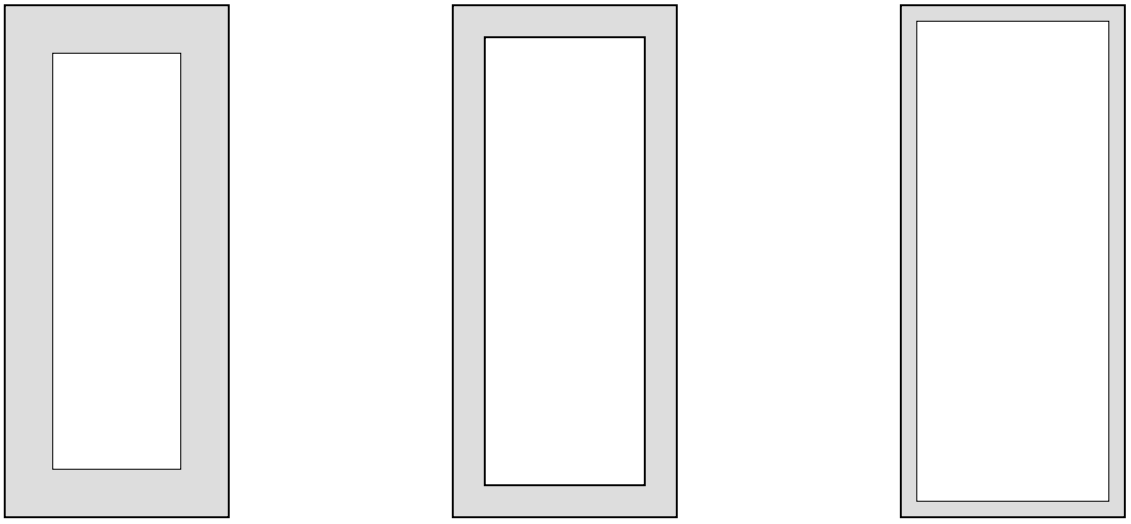


Figure 2. Solder Paste Application on Paddle:
Solder paste should be applied through an array of squares (or circles) which totals 50% of the total area of the paddle



Minimum 50% coverage

62 % coverage

Maximum 80% coverage

Figure 3. Solder Paste Application on Pins.

3. It is extremely difficult to supply proper reflow heating to the ground pad/thermal connection in a manual environment. Heat must be simultaneously applied to both the top and bottom side of the PCB assembly to ensure uniform reflow heat under the IC thermal pad. If insufficient heat is applied, the solder paste under the thermal pad will not reflow. In the case where the LPCC package houses a power amplifier, the thermal pad will not be properly connected to the heat sink and **will likely result in early device failure**. Conversely, if excess heat is applied, the device may be damaged.
4. Manual placement and/or manual repositioning of LPCC packages is not recommended.

3.3 Solder Reflow Profile

1. A solder composition of 63% Sn, 37% Pb for the mounting of surface mount packages is recommended. The PCB assembly should be instrumented and the reflow oven's process parameters established to ensure the solder paste manufacturer's reflow profile specification is met during the assembly process. See Figure 4.
2. The maximum PCB temperature recommended by the supplier must not be exceeded.

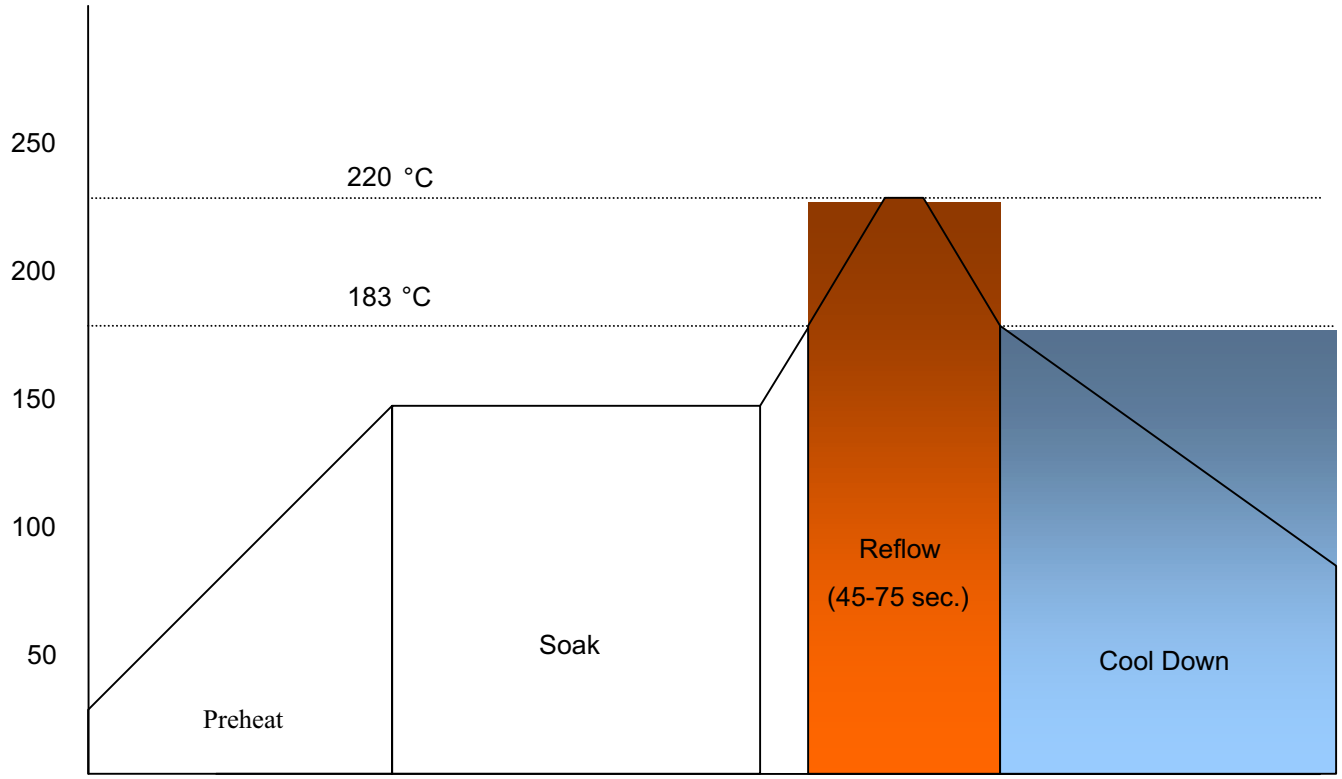


Figure 4. Solder Reflow Profile.

3.4 Rework

1. A package rework tool with vacuum pick-up should be used.
2. A bottom PCB heater should be used to preheat the board within 1" of the rework site.
3. Excess solder must be removed before new part placement.
4. The new package should be placed using pick and place equipment.
5. Reflow conditions should be followed as mentioned before.

3.5 Solder Process Inspection

1. The vias on the back of the PCB should be filled with solder as an indication of good connection of the LPCC thermal pad to the PCB. A thermal pad that is not soldered properly may cause device failure and will accelerate the MTTF (Median Time To Failures).
2. After reflow, verify that there is no bridging of solder to exposed circuitry, vias, or other pins that could cause shorts and affect performance.

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