Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
John Goldie
August 1993

Introduction

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

The Requirements

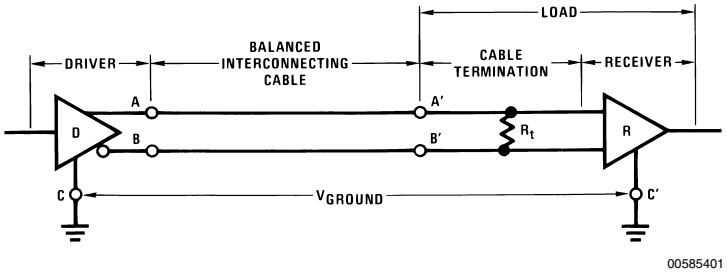
The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and TIA/EIA standards TIA/EIA-422-B (balanced) and TIA/EIA-423-B (unbalanced). In this application note the generic terms of RS-422 and RS-423 will be used to represent the respective TIA/EIA standards. A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1. The cable length
2. The data signaling rate
3. The characteristic of the interconnection cable
4. The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figure 1* and *Figure 2* are the digital interface for balanced *(1)* and unbalanced *(2)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

1. The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2. It is necessary to minimize interference with other signals, such as data versus clock.
3. The interconnecting cable is too long electrically for unbalanced operation (*Figure 3*).



Legend:

R_t = Transmission line termination and/or receiver input impedance

V_{GROUND} = Ground potential difference

A, B = Driver interface

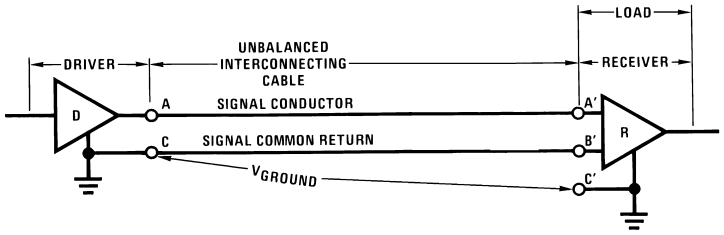
A', B' = Load interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. Balanced Digital Interface Circuit

The Requirements (Continued)



Legend:

R_t = Transmission line termination and/or receiver input impedance

V_{GROUND} = Ground potential difference

A, C = Driver interface

A', B' = Load interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 2. Unbalanced Digital Interface Circuit

Cable Length

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of data signaling rate. *Figure 3* is a composite of the guidelines provided by RS-422 and RS-423 for data signaling rate versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied data rate.

The maximum cable length between driver and load is a function of the data signaling rate. But it is influenced by:

1. A maximum common noise range of ±7 volts
   - A. The amount of common-mode noise

     Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   - B. Ground potential differences between driver and load.
   - C. Cable balance

     Differential noise caused by imbalance between the signal conductor and the common return (ground)
2. Cable termination

   At rates above 200 kbps or where the rise time is 4 times the one way propagation delay time of the cable
3. Tolerable signal distortion

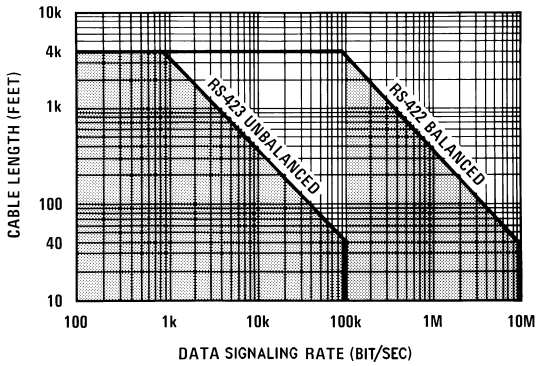


FIGURE 3. Data Signaling Rate vs Cable Length

Data Signaling Rate

The TIA/EIA Standards recommend that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the data signaling rate on these circuits is below 100 kbps, and balanced voltage digital inter-

Data Signaling Rate (Continued)

face on circuits up to 10 Mbps. The voltage digital interface drivers and receivers meeting the electrical characteristics of this standard need not meet the entire data signaling range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower data signaling rates.

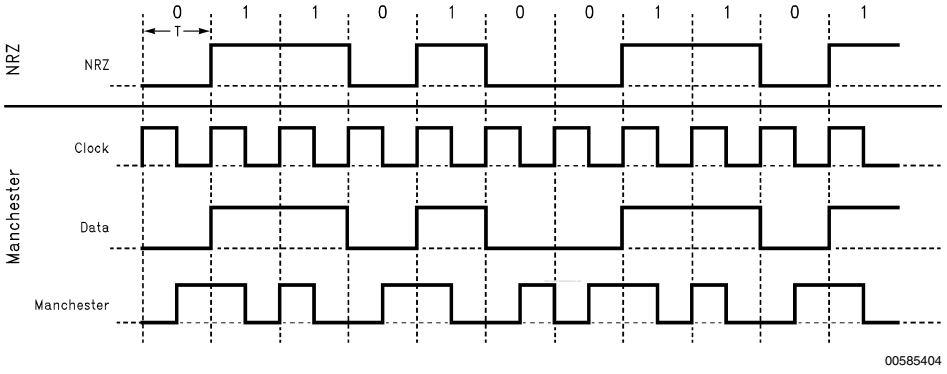
As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

Characteristics

DRIVER UNBALANCED (RS-423)

The unbalanced driver characteristics as specified by RS-423 are as follows:

1. A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.
2. With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the open circuit voltage magnitude (≥ 3.6V) for either binary state.
3. During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed |6V|, nor be less than |3.6V|. V_{SS} is defined as the voltage difference between the two steady state values of the driver output.



	Baud	Bits per Second	Hertz		Baud	Bits per Second	Hertz
CLOCK	—	—	1/T	Manchester	2/T	1/T	—
NRZ	1/T	1/T	—				

Note: bps (bits per second) - Data Information Rate "the number of bits passed along in one second."

baud-Modulation Rate "the reciprocal of the minimum pulse width."

For NRZ bps = bauds

FIGURE 4. Definition of Baud, Bits per Second (bps), Hertz (Hz) for NRZ and Manchester Coding

Characteristics (Continued)

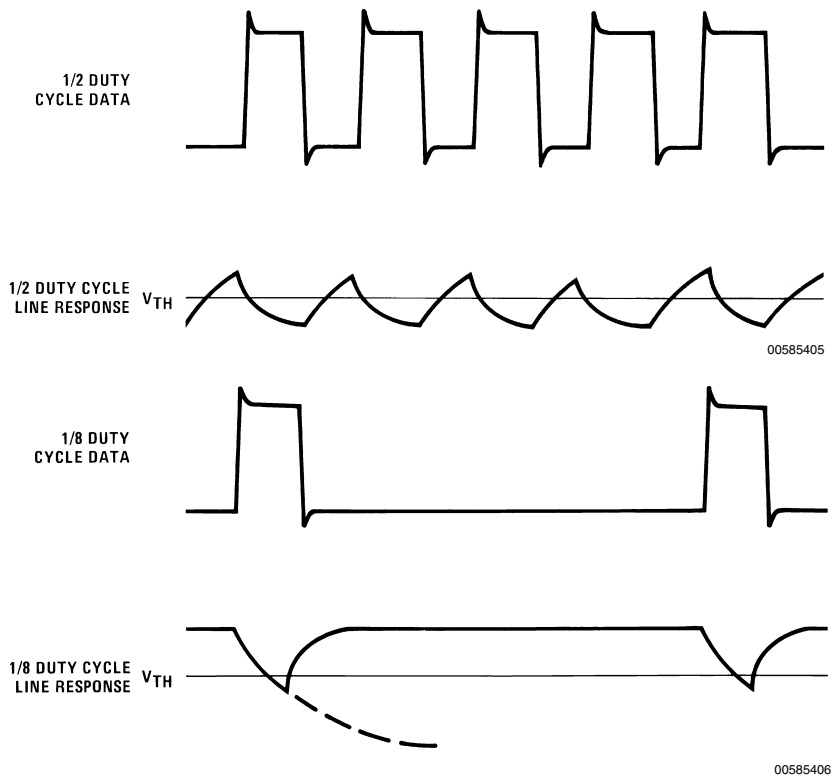
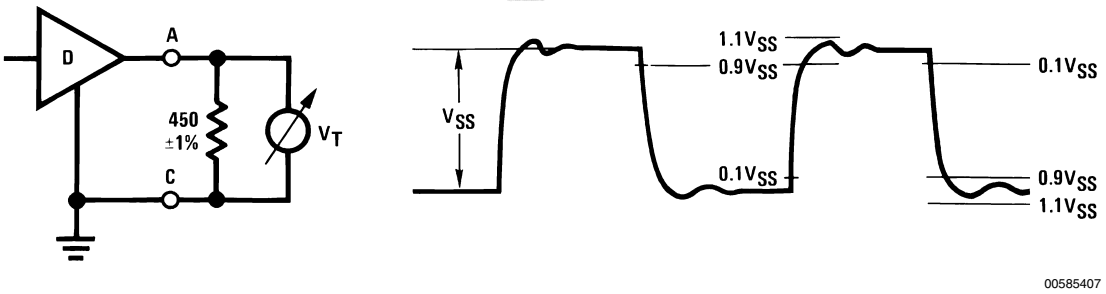


FIGURE 5. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_t|$

V_{SS} = Difference in steady state voltages

FIGURE 6. Unbalanced Driver Output Signal Waveform

Characteristics (Continued)

DRIVER BALANCED (RS-422)

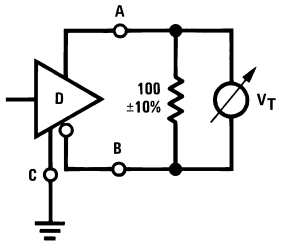
The balanced driver characteristics as specified by RS-422 are as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 10V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.
3. During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 10% of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

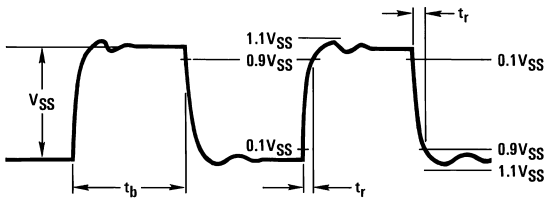
INTERCONNECTING CABLE

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) and is not further specified within the standards.

1. Conductor size of the 2 wires 24 AWG or larger, and wire resistance not to exceed 30Ω per 1000 feet per conductor.
2. Mutual pair capacitance between 1 wire in the pair to the other should be less than 20 pF/ft.



00585408



00585409

t_b = Time duration of the unit interval at the applicable modulation rate.

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - V_t|$

FIGURE 7. Balanced Driver Output Signal Waveform

RECEIVER

The receiver characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. The electrical characteristics of a single receiver without termination or optional fail-safe provisions are specified as follows:

1. Over an entire common-mode voltage range of –7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3. The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load including up to 10 receivers shall not have a resistance less than 90Ω for balanced, and 450Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.

Characteristics (Continued)

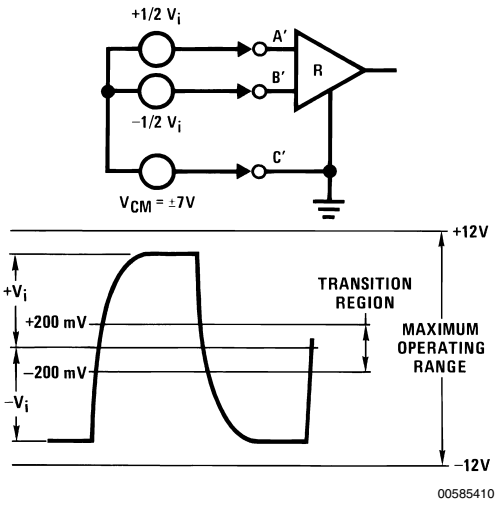


FIGURE 8. Receiver Input Sensitivity Measurement

Signal Rise Time

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum data signaling rate. Below 1 kbps the time to reach 90% V_{SS} shall be between 100 µs and 300 µs. If a driver is to operate over a range of data signaling rates and employ a fixed amount of wave shaping which meets the specification for the maximum data signaling rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 9* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

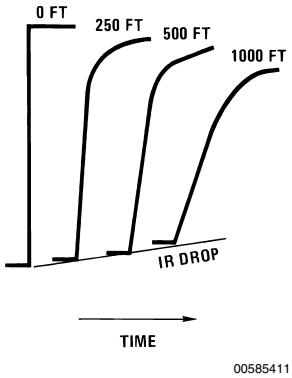


FIGURE 9. Signal Rise Time on Transmission Line vs Line Length

DS1691A/DS78LS120

THE DRIVER

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of both standards. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers (*Figure 10*) or 4 independent unbalanced drivers (*Figure 11*). When configured for unbalanced operation (*Figure 12*) a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable.*Figure 13* is the typical rise time vs external capacitor used for wave shaping. Note that the rise time control capacitors are connected betwen the control pins and the respective outputs.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 is connected V_{CC} = 5V V_{EE} = −5V. For applications with greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

DS1691A/DS78LS120 (Continued)

This mode is also allowed by the “B” revision of RS-422 (TIA/EIA-422-B) which relaxed to open circuit voltage from 6V to 10V in magnitude.

When configured as balanced drivers (*Figure 10*), each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques. If the driver is used in multi-point applications (multiple drivers) the use of the response control capacitors is not allowed.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 14*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1691/DS3691 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 14*, bottom waveform).

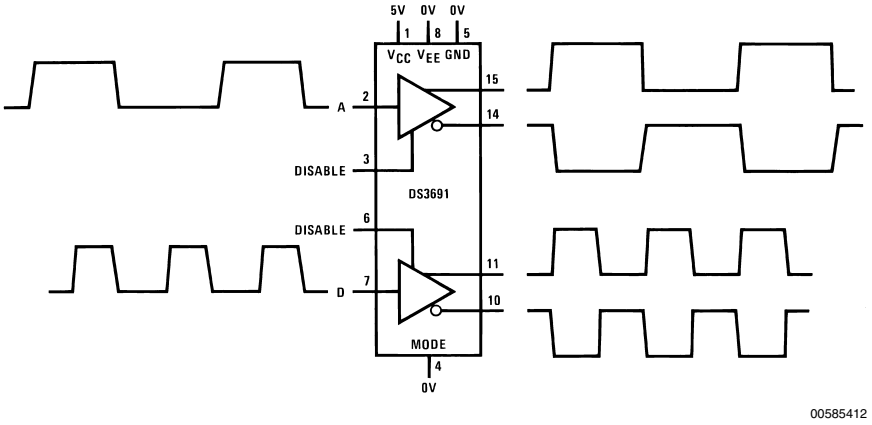


FIGURE 10. DS3691 Connected for Balanced Mode Operation

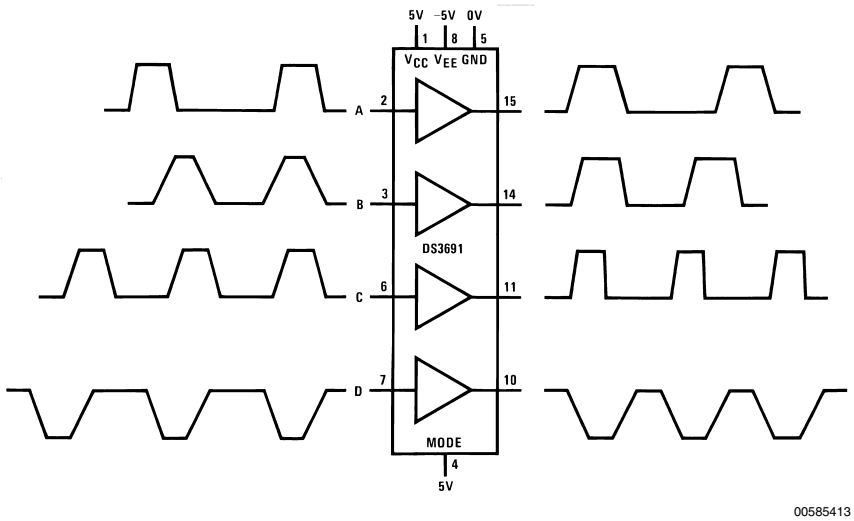


FIGURE 11. DS3691 Connected for Unbalanced Mode Operation (Non-inverting)

DS1691A/DS78LS120 (Continued)

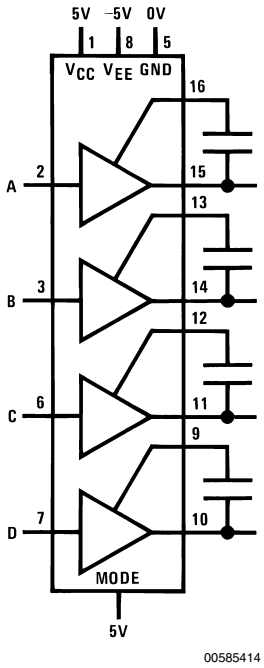


FIGURE 12. Using an External Capacitor to Control Rise Time of DS3691

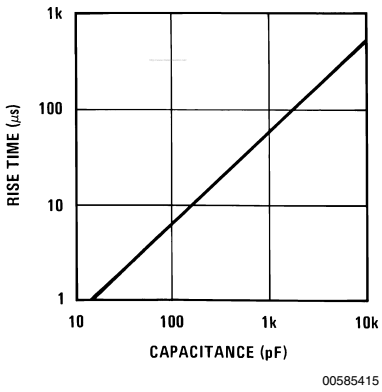


FIGURE 13. DS3691 Rise Time vs External Capacitor

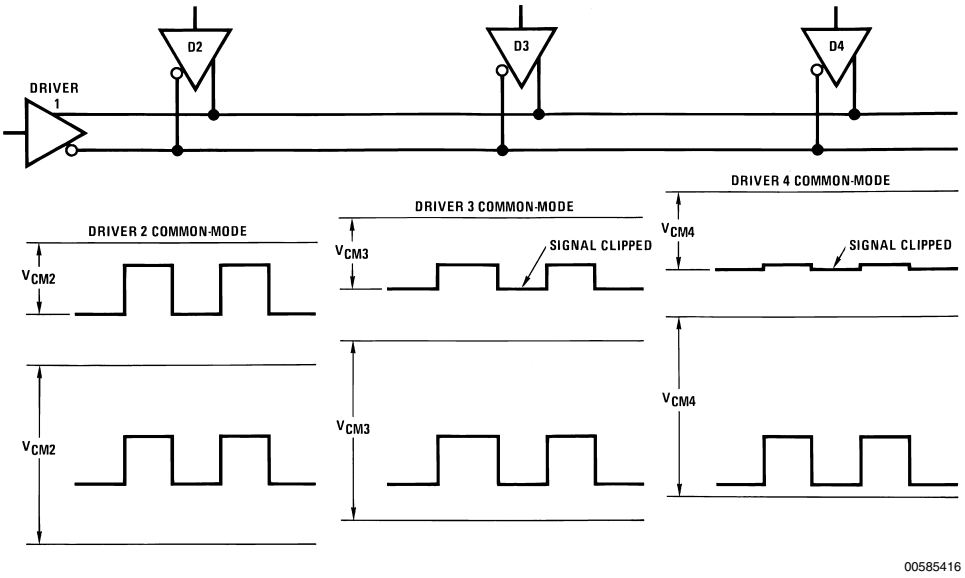
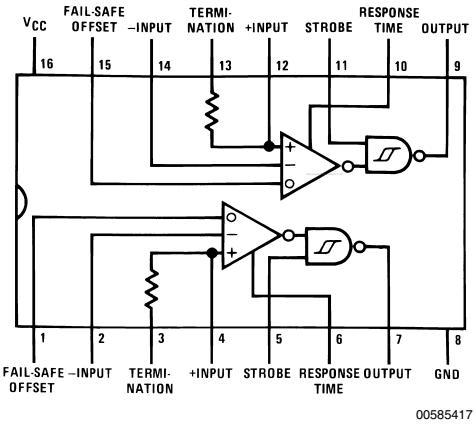


FIGURE 14. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)



Top View

FIGURE 15. DS78LS120/DS88LS120 Dual Differential Line Receiver

DS78LS120/DS88LS120

THE RECEIVER

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate (*Figure 16*). The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 17* . The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.

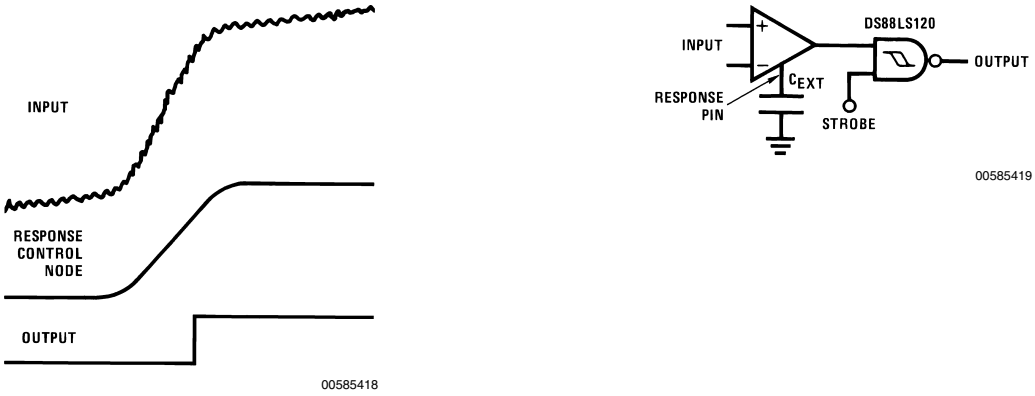


FIGURE 16. Application of DS88LS120 Receiver Response Control and Hysteresis

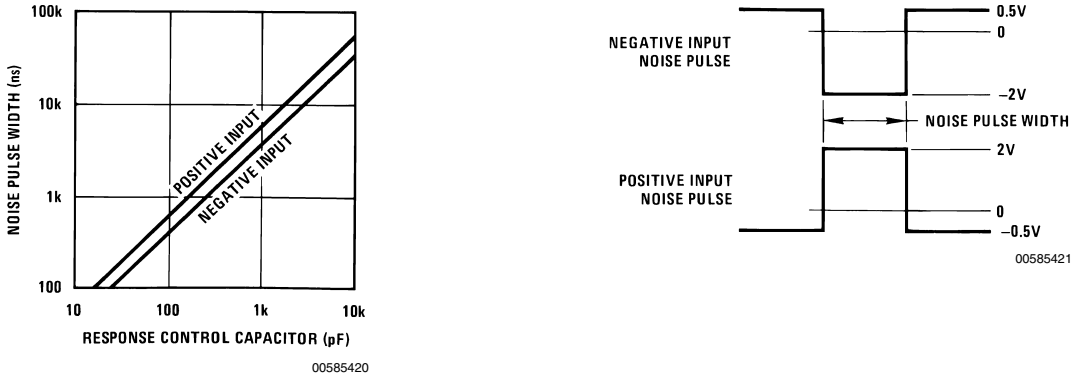


FIGURE 17. Noise Pulse Width vs Response Control Capacitor

Fail-Safe Operation

Some communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/ DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or –200 mV to –700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 18*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The “strobe” input will disable the A and B receivers and therefore may be used to “sample” the fail-safe detector (see *Figure 19*).

Fail-Safe Operation (Continued)

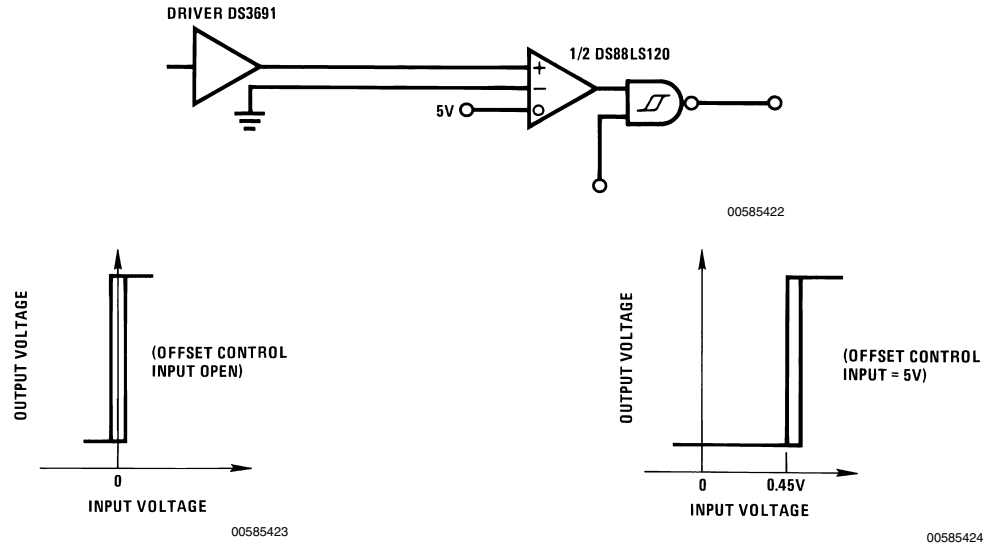


FIGURE 18. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines

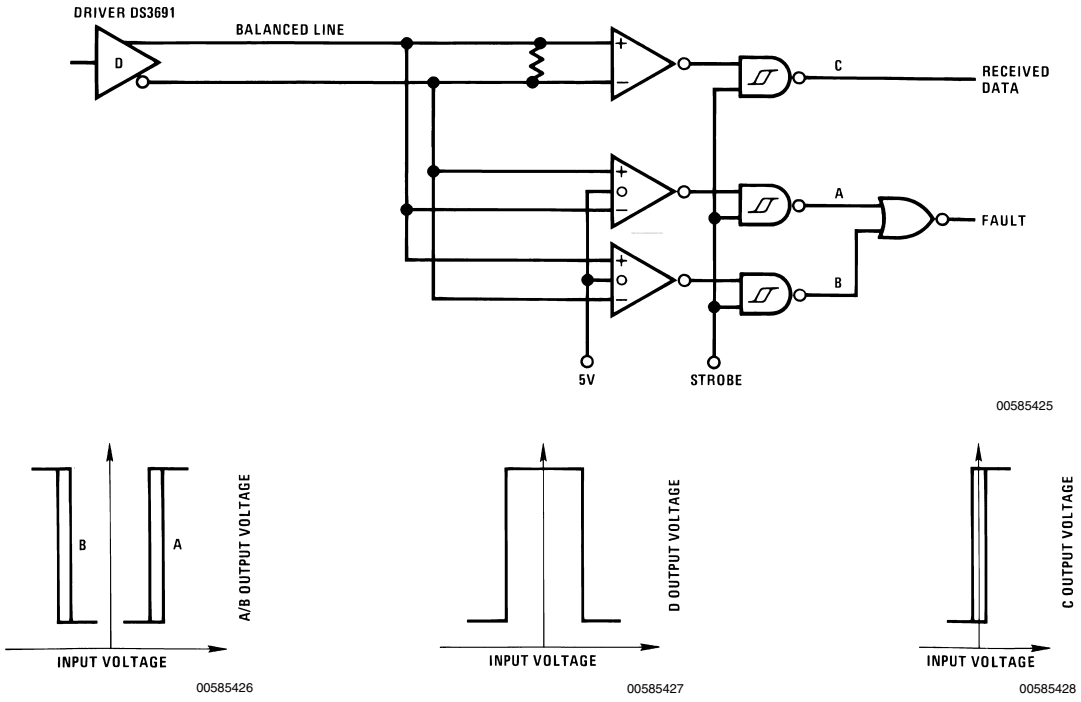


FIGURE 19. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Conclusion

This application note provides a brief overview of TIA/EIA-422-B and TIA/EIA-423-B. At the time of publication of this application note the Rev. B standards were draft standard proposals only. For complete/current information on the respective standards the reader is referenced to the respective standards, as minor differences may exist between this document and the final versions.

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507