AN-6003

"Shoot-through" in Synchronous Buck Converters

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Abstract

The synchronous buck circuit is in widespread use to provide "point of use" high current, low voltage power for CPU's, chipsets, peripherals etc. In the synchronous buck converter, the power stage has a "high-side" (Q1 below) MOSFET to charge the inductor, and a "Low-side" MOSFET which replaces a conventional buck regulator's "catch diode" to provide a low-loss recirculation path for the inductor current.

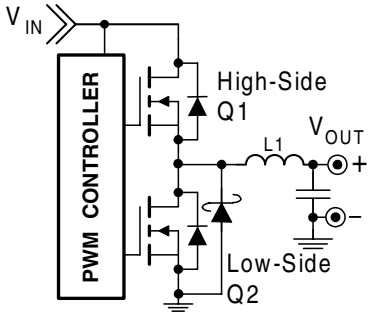

Figure 1. Synchronous Buck output stage

Shoot-through is defined as the condition when both MOSFETs are either fully or partially turned on, providing a path for current to "shoot through" from V_{IN} to GND. To minimize shoot-through, synchronous buck regulator IC's employ one of two techniques to ensure "break before make" operation of Q1 and Q2 to minimize shoot-through:

1. **Fixed "dead-time":** A MOSFET is turned off, then a fixed delay is provided before the low-side is turned on. This circuit is simple and usually effective, but suffers from its lack of flexibility if a wide range of MOSFET gate capacitances are to be used with a given controller. Too long a dead-time means high conduction losses. Too short a dead time can cause shoot-through. A fixed dead-time typically must err on the "too long" side to allow high C_{GS} MOSFETs to fully discharge before turning on the complementary MOSFET.
2. **Adaptive gate drive:** This circuit looks at the V_{GS} of the MOSFET that's being driven off to determine when to turn on the complementary MOSFET. Theoretically, adaptive gate drives produce the shortest possible dead-time for a given MOSFET without producing shoot-through.

In practice, a combination of adaptive and fixed produces the best results, and is typically what is in today's PWM controllers and gate drivers as shown in Figure 2

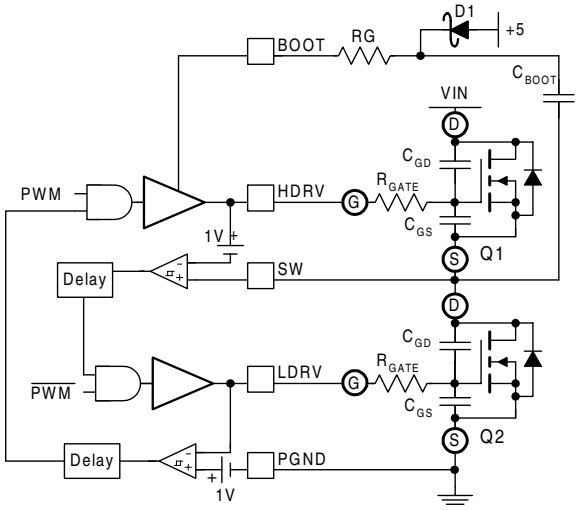

Figure 2. Typical Adaptive Gate drive

Even though there apparently is a "break before make" action by the controller, shoot-through can still occur when the High-side MOSFET turns on, due to Gate Step.

Shoot-through is very difficult to measure directly. Shoot-through currents persist for only a few nS, hence the added inductance in a current probe drastically affects the shoot-through waveform. Shoot-through manifests itself typically as increased ringing, reduced efficiency, higher MOSFET temperatures (especially in Q1) and higher EMI. This paper will provide analytical techniques to predict shoot-through, and methods to reduce it.

"Gate Step" – The shoot-through culprit

If the adaptive circuits are working, then we shouldn't see any shoot-through, right?

Not exactly. Most shoot-through occurs when the high-side MOSFET is turned on. The high dv/dT on the SW node (Drain of the low-side MOSFET) couples charge through C_{GD}. This drives the gate positive at the very moment when the driver is trying to hold the gate low. C_{GD} and C_{GS} form a capacitive voltage divider, which attenuates the gate step such that the worst case peak amplitude of the gate step (V_{STEP}) seen is:

$$V_{STEP(PK)} \approx R_T \bullet C_{GD} \bullet \frac{V_{IN}}{T_R} \bullet \left(1 - e^{\frac{-T_R}{R_T \bullet (C_{GD}+C_{GS})}}\right) \quad (1a)$$

Where $R_T = R_{DRIVER} + R_{GATE} + R_{DAMPING}$ (see Figure 5), and T_R is the rise-time of the SW node.

The limiting case is when $T_R = 0$. Then

$$V_{STEP(MAX)} \approx V_{IN} \bullet \frac{C_{GD}}{C_{GD} + C_{GS}} \quad (1b)$$

This expression only illustrates the AC portion of the gate step. The gate step is injected onto whatever voltage the MOSFET's gate has discharged to. For example, if the switch node rises when VGS = 1V, and the gate step amplitude is 2V, instantaneously there will be 3 V_{GS} which is more than enough to have a high instantaneous current through both MOSFETs. It's important, therefore that adaptive gate drive circuits allow sufficient delay to prevent the high side from turning on before the low-side V_{GS} is discharged down to a few hundred mV.

An illustration of gate step is seen below.

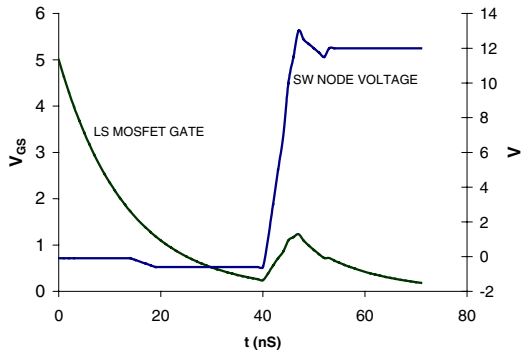

Figure 3. Gate Step for V_{IN} .=12V.

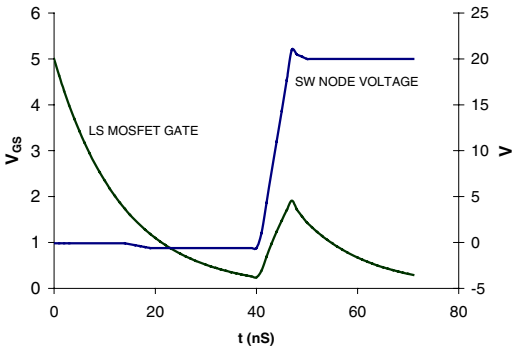

Figure 4. Gate Step for V_{IN} .=20V

Further exacerbating the problem for adaptive circuits is the fact that the adaptive comparator is not actually sensing the voltage at the internal gate junction of the MOSFET. As seen in Figure 5, the internal MOSFET's gate voltage has an unavoidable internal R_{GATE} resistance. In addition, some designers like to have a "damping" resistor in series with the gates of MOSFETs that are located physically far away from their gate drives. This creates a bigger problem for the adaptive gate drive circuit. These series resistances form a voltage divider with the internal pull-down resistance of the low-side gate drive of the IC, causing it to think the gate voltage is lower than it really is when it decides to release the High-side driver.

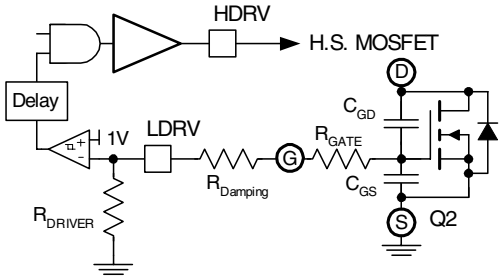

Figure 5. Resistance in the gate drive path attenuates the voltage at the MOSFET gate node.

When there is 1V at the pin of the IC, the internal MOSFET V_{GS} is:

$$V_{GS(I)} = \frac{1V}{R_{DRIVER}} \bullet \left(R_{DRIVER} + R_{GATE} + R_{Damping}\right)$$

Consider an example where:

$R_{DRIVER} = 2\Omega$, $R_{GATE} = 1.2\Omega$

$R_{DAMPING} = 5\Omega$

When the adaptive gate circuit switches, the internal MOSFET gate voltage will be:

$$\frac{1V}{2\Omega} \bullet (2 + 1.2 + 5)\Omega = 4.1V$$

In this example, if there were no delay in the circuit, the HDRV would turn on when the low-side MOSFET has just begun to discharge, causing a very high shoot-through current.

Much of the problem in the above circuit is the damping resistor. If a damping resistance is necessary, place a Schottky diode across the resistor (as shown below) to reduce the effect the damping resistor will have on the adaptive gate drive.

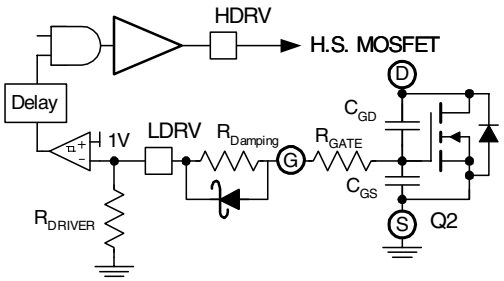

Figure 6. Schottky diode reduces damping resistor error in adaptive gate drive

When using the schottky, the internal gate node will be at:

$$V_{GS(I)} = 0.5 + \frac{1V}{R_{DRIVER}} \bullet (R_{DRIVER} + R_{GATE})$$

or 2.1V for our example. A dramatic improvement. Furthermore, the Schottky reduces the duration of the shoot-through step, since only $R_{GATE} + R_{DRIVER}$ will be discharging C_{GS}, rather than the sum of $R_{GATE} + R_{DAMPING} + R_{DRIVER}$.

Table 1 below illustrates the performance improvement in our example with and without the Schottky diode:

	No Schottky	With Schottky	
Comparator Flips @ $V_{GS(INT)}$ =	4.1	2.1	V
$V_{GS(INT)}$ after 20nS delay	2.23	1.14	V
VSTEP Peak	2.50	1.25	V
Peak current	36	0.29	A
Power Loss @ F_{SW}=300KHz	1100	20	mW

Conditions: Typical low-side MOSFET, 25nS delay from comparator sense to beginning of SW node rise, $19V_{IN}$, 10nS SW node rise time.

Table 1 . Peak Currents with and without Schottky with $R_{DAMPING}$ = 5Ω .

MOSFET Choices

MOSFET characteristics can have a dramatic effect on how much shoot-through current can be induced by the gate step. The worst case for shoot-through is an infinitely fast (0 rise time) on the drain node. The amount of gate step is largely determined by the ration of C_{GS} and C_{GD} . Once the size of the gate step is determined (eq. 1 above), the peak magnitude of the shoot-through current can be calculated as :

$$I_{PEAK(MAX)} \approx K \bullet G_M \bullet (V_{STEP(MAX)} - V_{TH(MIN)}) \quad (2)$$

where G_M is the transconductance (in S, or A/V) given in the datasheet. While only a small percentage of MOSFETs exhibit $V_{TH(MIN)}$ at room temperature, V_{TH} goes down with increasing junction temperature, therefore $V_{TH(MIN)}$ is a good proxy for the V_{TH} at the operating junction temperature of the MOSFET. Subsequent calculations use $V_{TH(MIN)}$ for this reason.

G_M is not really a contstant, however, and its value is greatly reduced low enhancement voltages (V_{GS}-V_{TH}). In these calculations we use a factor "K" from the graph below, which is typical of G_M with low values of enhancement. The X axis of Figure 7 is calculated as $\frac{V_{GS} - V_{TH(MIN)}}{V_{TH(MIN)}}$

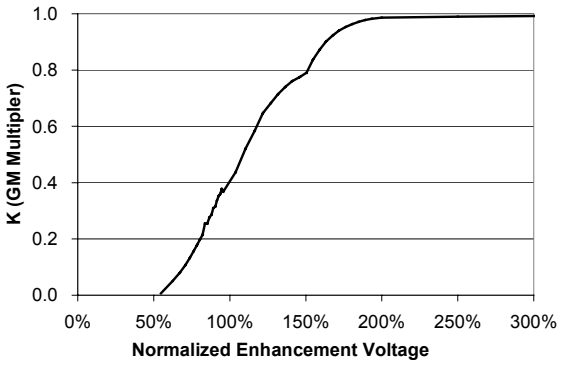

Figure 7 G_M factor (K)

Table 2 shows the relevant MOSFET characteristics which determine the maximum shoot-through current.

MOSFET	C_{GS}	C_{GD}	Typical V_{TH}	Min V_{TH}	G_M
MOSFET1	3,514	307	1.6	1	86
MOSFET2	5,070	230	1.2	0.8	97
MOSFET3	4,942	315	1.6	1	80
MOSFET4	3,888	401	1.6	1	135
MOSFET5	6,324	281	1.15	0.6	90

Table 2 . Low-Side MOSFET Characteristics

Each of the MOSFETs represented is from a different process and has different ratios of internal capacitance.

MOSFET	$V_{STEP(MAX)}$	$V_{TH(MIN)}$	$V_{STEP} - V_{TH(MIN)}$	I_{PEAK} (max)
MOSFET1	1.53	1	0.53	0.31
MOSFET2	0.82	0.8	0.02	0.02
MOSFET3	1.14	1	0.14	0.07
MOSFET4	1.78	1	0.78	16.37
MOSFET5	0.81	0.6	0.21	0.13

Table 3. Maximum V_{STEP} and $I_{SHOOTTHROUGH}$ @ V_{IN} = 19V and $V_{GS(START)}$ = 0V.

Table 3 assumes that the V_{GS} has dropped to 0 before the SW node rises when HDRV turns on. As demonstrated above, the smallest amplitude of V_{STEP} comes from MOSFET2 and MOSFET5, which are low-threshold devices. Low threshold in large part is due to a thin gate oxide, giving the MOSFET a high $\frac{C_{GS}}{C_{GD}}$ ratio, which attenuates V_{STEP}. more than other MOSFETs.

Also, Table 3 only shows the theoretical peak current in Q2 due to the gate step. In a real converter, parasitic inductance limits the rise in current to 4A/nS. Even for the MOSFET4, the gate pulse only stays above threshold for about 5nS, so the shoot-through current would be further limited.

An additional shortcoming of the simplified calculations of Table 3 is the assumption that SW node turn-on begins when V_{GS} of the low-side is at 0. As we saw from the earlier discussion, this may not be the case.

Reducing gate step by slowing down Q1 rise time

Usually, designers attempt to achieve the fastest rise-time possible on the High-Side MOSFET in order to minimize switching losses. A simplified expression for turn-on losses ($P_{(TURN-ON)}$) for the high-side MOSFET is:

$$P_{TURN-ON} \approx F_{SW} \bullet \frac{T_R \bullet V_{IN} \bullet I_{OUT}}{2} \qquad (3)$$

where T_R is the rise-time of the MOSFET. A very fast rise-time (high $\frac{dV}{dt}$ on SW) is desirable to minimize high-side power dissipation, but if it results in a large gate-step, causing shoot-through, the dissipation effect can be greater than the dissipation induced by slowing the rise time. In some situations this is the only practical approach to eliminate shoot-through.

As can be seen in Figure 8, slowing down the rise time has a dramatic effect on the amplitude of V_{STEP} that is coupled into the Low-side MOSFET gate. T_R slowdown has the added benefit of reducing EMI, but comes at a cost of efficiency loss . Figure 8 and subsequent tables were simulated with MOSFETs typical of those used in notebook PC's (2 in parallel) with 15A output current and 19V_{IN}. Figure 8 assumes that the SW node begins to rise when the internal gate node has discharged down to 0.5V.

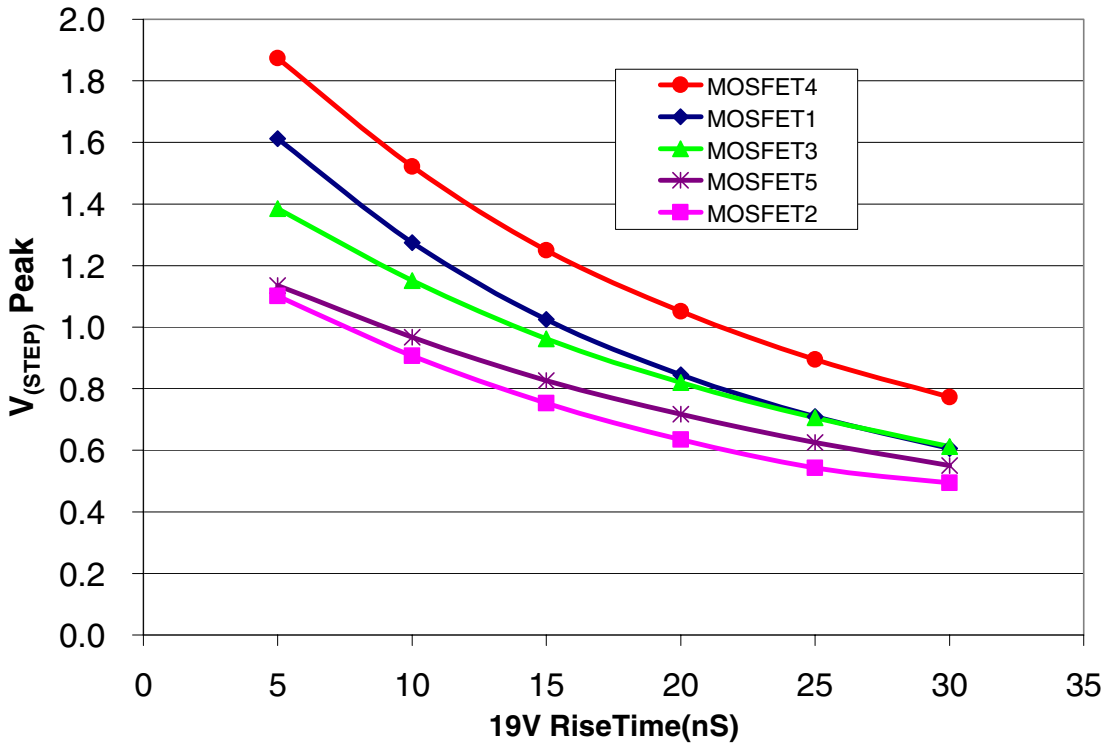

Figure 8 . Effect of SW node rise-time on V_{STEP}
VIN=19V, SW rise starts @ $V_{GS(Q2)}$ = 0.5V

Table 4 shows the power loss due to shoot-through for each MOSFET.

The major component of switching loss during Q1 turn-on is:

$$P_{TURN-ON} \approx t_R \bullet F_{SW} \bullet \frac{V_{IN} \bullet I_{OUT}}{2} \qquad (3)$$

and is computed in the right-most column for each rise-time in Table 4 for I_{OUT} = 15A.

$T_{R(SW)}$	FET1	FET2	FET3	FET4	FET5	Q1 t_R Loss
5	18	10	10	56	27	214
10	12	6	6	39	24	428
15	7	3	3	28	19	641
20	3	0	0	19	16	855
25	0	0	0	11	12	1,069
30	0	0	0	4	8	1,283

Table 4. Worst case (Min V_{TH}) shoot-through power loss (mW)
SW rise starts @ $V_{GS(Q2)}$ = 0.5V

In most cases, the shoot-through is negligble, so slowing down high-side rise-time would not be a prudent choice, since the more power would be lost in slowing down the rise time than power saved by eliminating shoot-through.

If, the controller's gate drive starts to turn Q1 on before allowing the internal node of Q2 to discharge, SW will rise when there is still a substantial V_{GS} on Q2 as shown is Table 5. Slowing down Q1 can then be an effective strategy to reduce shoot-through losses.

$T_{R(SW)}$	FET1	FET2	FET3	FET4	FET5	Q1 t_R Loss
5	90	62	29	380	551	214
10	30	31	24	127	266	428
15	23	26	18	61	58	641
20	16	21	13	50	54	855
25	8	16	7	39	51	1,069
30	0	11	1	25	47	1,283

Table 5. Worst case (Min V_{TH}) shoot-through power loss (mW)
SW rise starts @ $V_{GS(Q2)}$ = 1V

This is typically achieved by adding resistance (RG in Figure 2) in series with C_{BOOT} . An approximation for T_R provides a good starting point for choosing a value of RG:

$$T_R \approx C_{GS} \bullet \left(R_{DRIVE(L-H)} + RG \right) \qquad (4)$$

where $R_{DRIVE(L-H)}$ is the resistance of the IC's high-side MOSFET gate driver when driving from low to high.