AN-6961
Critical Conduction Mode PFC Controller

Description

This application note describes a power factor correction (PFC) circuit using the FAN6961. Both the features of this controller, as well as the operation of the power factor correction circuit, are presented in detail. Based on the proposed design guideline, a design example with detailed parameters demonstrates the performance of the controller.

Introduction

The FAN6961 PFC controller is an 8-pin Boundary Current Mode (BCM) IC intended for controlling PFC pre-regulators. The FAN6961 provides a controlled on-time to regulate the output DC voltage and achieve natural power factor correction. The maximum on-time of the switch is programmable to ensure safe operation during AC brownouts. An innovative multi-vector error amplifier is built in to provide rapid transient response and precise output voltage clamping. Once the output feedback loop is opened, the output driver (GD) is disabled to provide protection of the system. The start-up current is lower than 20μA and the operating current has been reduced to 5mA. The supply voltage can be operated up to 25V, maximizing application flexibility. The FAN6961 also enables cycle-by-cycle current limiting protection for the external power MOSFET.

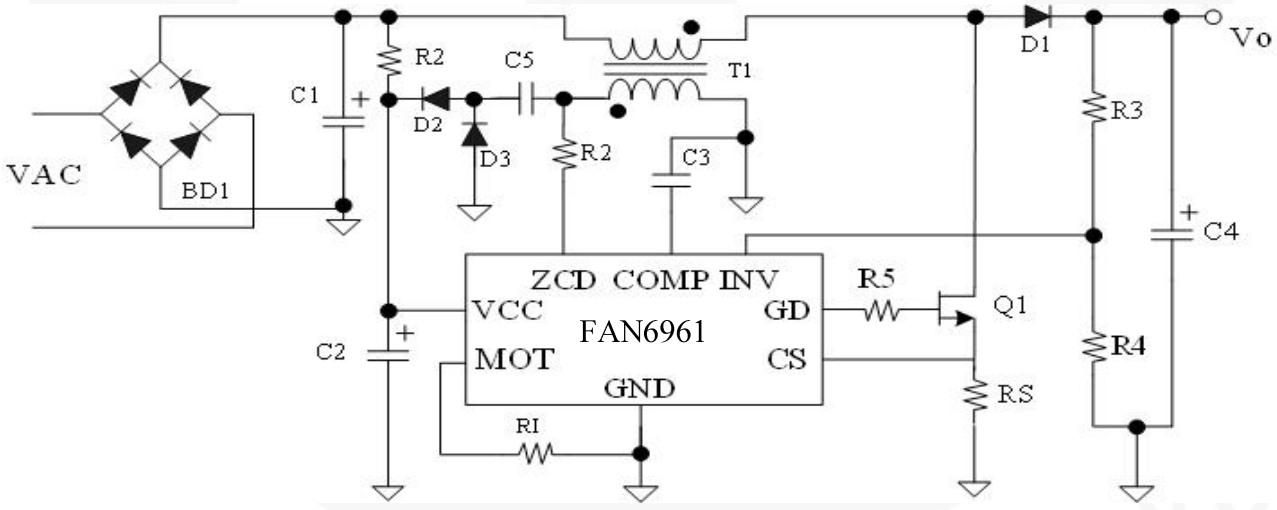


Figure 1. Power Factor Correction Circuit

Basic Operation of the Boost Converter

The typical boost converter and its operational waveforms are shown in Figure 2, 3, and 4, respectively.

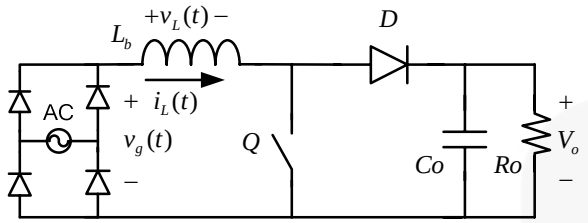


Figure 2. Boost Converter

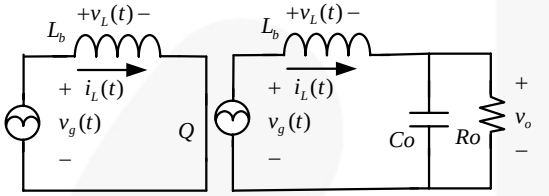


Figure 3. Switching Sequences of the Boost Converter

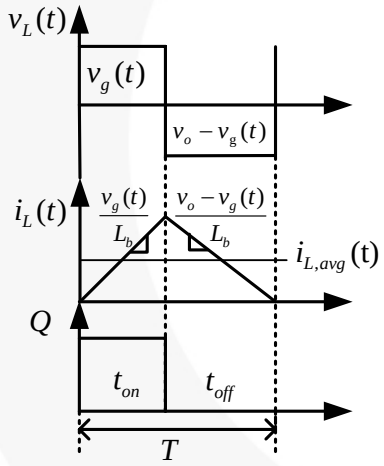


Figure 4. One-cycle Waveform of the Boost Converter

Operation Principle

Switch Q is ON: When Q turns on, the rectifier diode D is reverse-biased and output capacitor C_O supplies load current. The rectified AC line input voltage $V_g(t)$ is applied to the inductor L_b so that inductor current I_L ramps up linearly and can be expressed as:

$$I_L(t_{on}) = \frac{V_g(t)}{L_b} \tag{1}$$

Switch Q is OFF: When Q turns off, the voltage V_O-$V_g(t)$ is applied to inductor L_b and the polarity on the inductor L_b is reversed. The diode D is forward-biased in this stage. The energy stored in the inductor L_b is delivered to supply load current and output capacitor C_O. The inductor current i_L can be expressed as:

$$I_L(t_{off}) = \frac{V_o - V_g(t)}{L_b} \tag{2}$$

Controlled On-Time: The on-time of the power MOSFET Q is determined by the output of the error amplifier that monitors the preregulator output voltage. With a low-bandwidth error amplifier, the feedback signal is almost constant during a half AC cycle, resulting a fixed on-time of the power MOSFET at a specific AC voltage and some certain output power level. Therefore, the peak inductor current I_{Lpk} automatically follows the input voltage $V_g(t)$, achieving a natural power factor correction mechanism. Figure 5 shows the typical inductor current waveform during a half AC cycle.

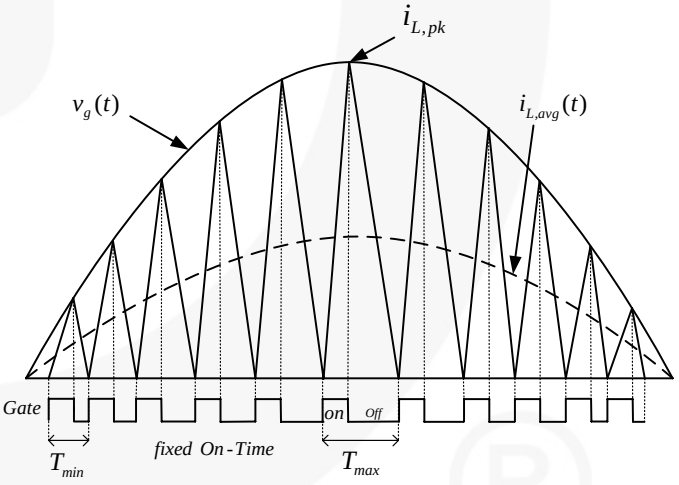


Figure 5. Controlled On-Time Inductor Current Waveform

Referring to Figure 4, considering one switching period the average inductor current $I_{L,ave}(t)$ can be calculated by the average area of triangle waveform of inductor current:

$$I_{L,avg}(t) = \left[V_g(t) + \frac{V_g(t)^2}{V_o - V_g(t)} \right] \bullet \frac{\left[\frac{t_{on}}{T_s} \right]^2}{2 \bullet L_b} \bullet T_s \tag{3}$$

Block Operation Description

Multi-Vector Error Amplifier

The FAN6961 has a trans-conductance type amplifier that provides better dynamic performance. Referring to Figure 6, the error amplifier output V_{EA} is compared with a sawtooth waveform to generate a fixed on-time. To achieve a low input current THD, the variation of the on-time within one input AC cycle should be very small. Therefore, the bandwidth of the feedback loop should be set below 20Hz to maintain a constant on-time for a line half-cycle. Connecting a capacitance C_{EA}, such as 1μF, between COMP and GND is suggested.

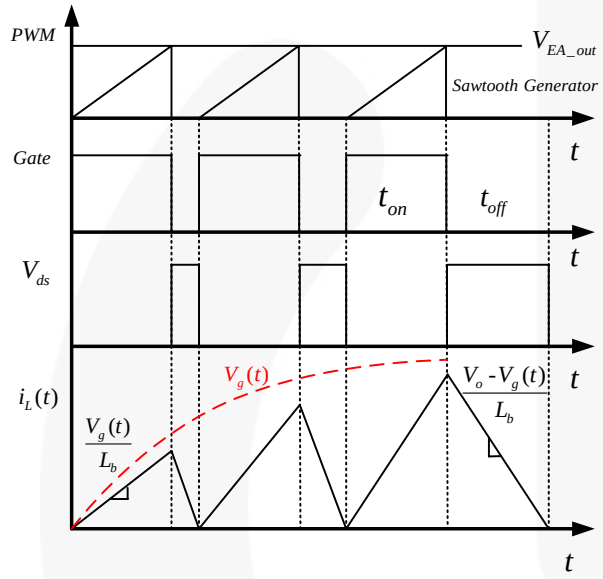


Figure 6. Operation Waveforms of Fixed On Time Technique

For fast transient response and precise clamping of the output voltage overshoot and undershoot, the FAN6961 has a built-in multi-vector error amplifier. Figure 7 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds +6% and -8% of the reference voltage, the multi-vector error amplifier adjusts its output impedance to increase the loop response.

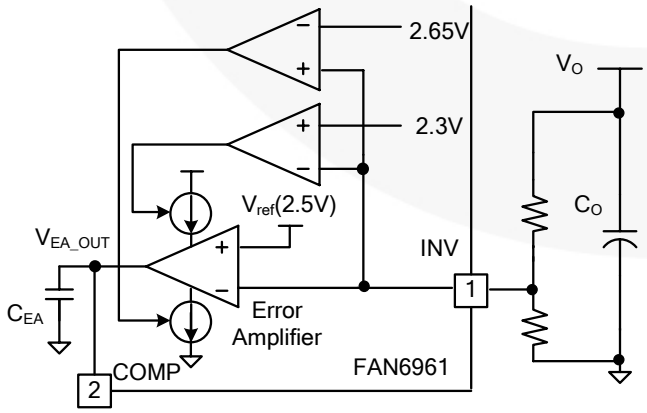


Figure 7. Block Diagram of the Multi-Vector Error Amplifier

Total Harmonic Distortion (THD) Optimization

As discusses previously, the FAN6961 uses the controlled on-time technique to achieve power factor correction mechanism. However, to get better THD at light load condition, especially at high input voltage, a THD optimization circuit is inserted into the FAN6961. With this internal THD optimization circuit, the on-time of the power MOSFET is modulated to further improve the THD performance. The calculated on-time variation within one line voltage period with the fixed on-time technique, and after the THD optimization is added, are shown in Figure 8. The calculated input current waveform is shown in Figure 9.

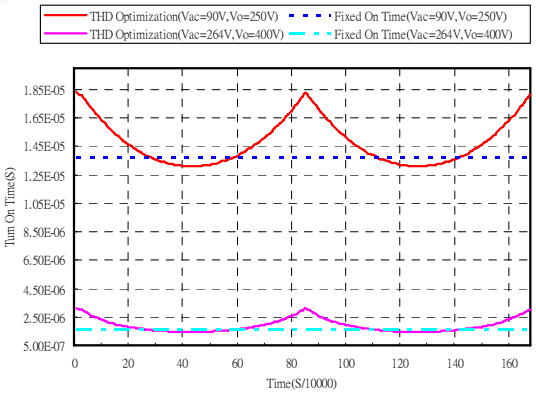


Figure 8. MOS Turn-on Time Calculational Curve (Before and After THD Optimization Circuit Added)

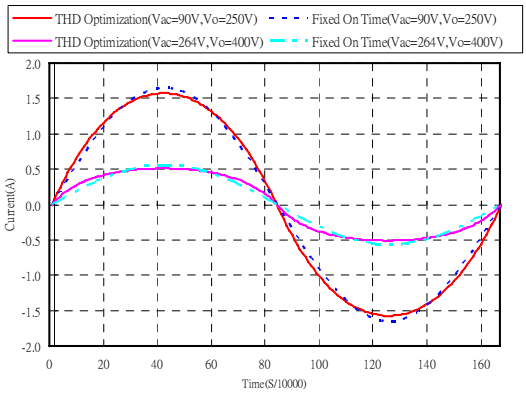
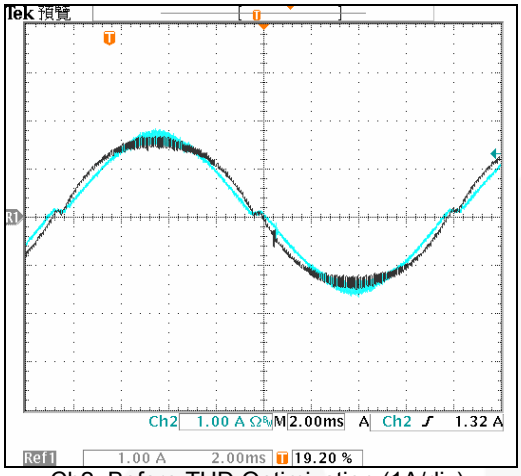


Figure 9. Calculated Waveforms of the Input Current (Before and After THD Optimization Circuit Added)

Figure 10 shows the measured input current on the example circuit board.



Ch2: Before THD Optimization (1A/div);
Ref1: After THD Optimization (1A/div)

Figure 10. Calculated Waveforms of the Input Current (Before and After THD Optimization Circuit is Added)

Figure 11 shows the measured THD performance on the example circuit board.

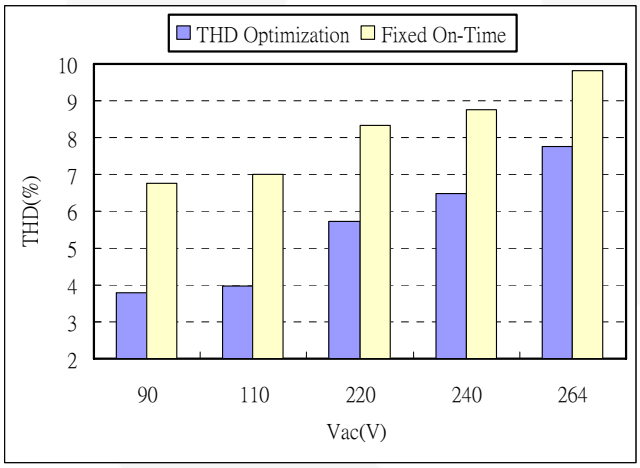


Figure 11. Measured THD Result at Full Load Condition (Fixed On-time Technique vs. THD Optimization)

Over- / Under-Voltage Protection (OVP/UVP)

Over / under-voltage protection is built-in to provide protection by detecting and examining the voltage on INV pin. When the voltage V_{INV} exceeds 2.75V due to abnormal conditions, the internal OVP protection circuit is triggered to disable the PWM output. Over-voltage conditions are usually caused by an open-loop feedback. A debounce time around 35μs is added to prevent false triggering. If the voltage V_{INV} is below 0.45V due to short-circuit conditions, PWM output is turned off.

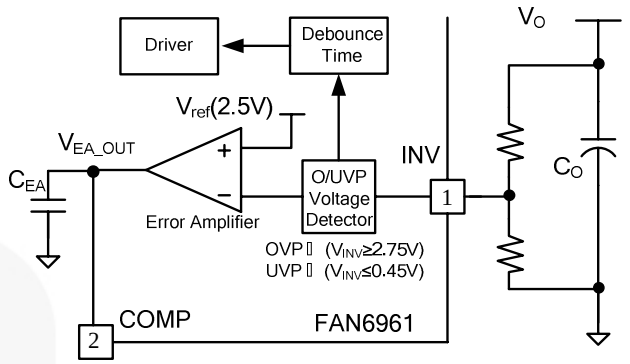


Figure 12. Block Diagram of the Over / Under- Voltage Protection

Zero-Current Detection

Figure 13 shows the block diagram of the zero-current detection. The zero inductor current detection is performed by sensing the information on an auxiliary winding of the PFC inductor. As shown in Figure 14, when Q turns off, the stored energy of the inductor starts to release to the output. The voltage on the ZCD starts to decrease when the energy in the inductor dries out. Once the ZCD voltage is lower than the threshold voltage (1.75V typical), the PWM output is high again and initiates a new switching cycle. The output rectifier is always turned off with zero current, so the converter works in boundary mode conditions and the power MOSFET is switched on with low voltage to minimize the switching losses.

Once the ZCD voltage is lower than the disable threshold voltage (around 0.25V) for a duration of about 800μs, the PWM output is disabled.

To prevent high switching frequency during light load conditions, an inhibit timer function is built in to limit the maximum switching frequency.

An RC filter (C_{ZCD} is around 0~22pF, R_{ZCD} is around 33K~68KΩ) connected from auxiliary winding to the ZCD pin is recommended to improve noise immunity on the ZCD pin.

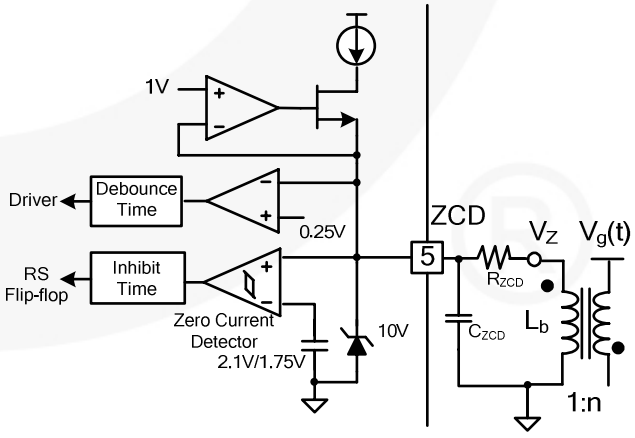


Figure 13. Block Diagram of the Zero-Current Detection

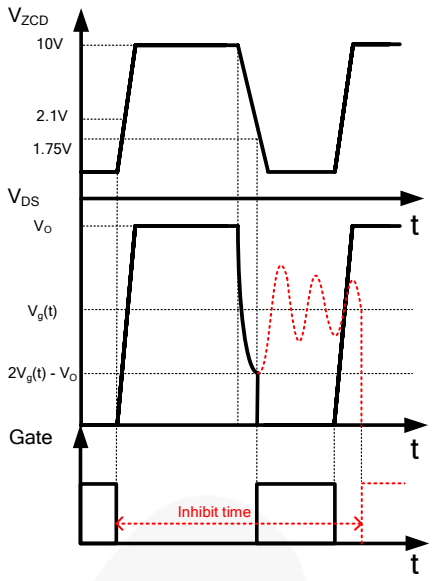


Figure 14. V_{DS} & V_{ZCD} & Gate Waveform

Maximum On-Time Operation

The on-time of the power MOSFET is varied with the output power and the AC input voltage. While the AC input voltage decreases, the on-time increases accordingly. The maximum on-time limit $t_{on,max}$ can be programmed by the resistor connected between MOT and GND pin.

$$t_{on,max} = R_{mot}(k\Omega) \bullet \frac{25}{24}(\mu s) \quad (4)$$

The range of the maximum on-time is designed to be within 10~50μs; 25μs is recommended.

V_{CC} Over-Voltage Protection

A V_{CC} over-voltage protection avoids damage when the voltage V_{DD} exceeds the internal threshold due to an open-loop failure. Once the protection is triggered, the PWM output is turned off.

Peak Current Limiting

The switch current is sensed across a resistor and supplied to an input terminal of a comparator. A voltage higher than the 0.82V threshold voltage on the CS pin immediately terminates the current switching cycle, activating cycle-by-cycle current limiting.

Leading-Edge Blanking (LEB)

A turn-on spike inevitably occurs at the CS pin when the power MOSFET is switched on. At the beginning of each switching pulse, the current-limit comparator is disabled for around 350ns to avoid premature termination. The gate drive output cannot be switched off during the blanking period.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off threshold voltages are fixed internally at 12V and 9.5V, respectively. This hysteresis behavior guarantees a one-shot start-up, as long as a proper start-up resistor and hold-up capacitor are used.

Output Driver

With a low on resistance and a high current driving capability, the output driver can drive an external capacitive load larger than 3000pF. Cross conduction currents are avoided to minimize heat dissipation, improving efficiency and reliability. This output driver is internally clamped by a 17V Zener diode.

Lab Note

Before rework or solder/desolder on the power supply, **discharge the primary capacitors by external bleeding resistor**. Otherwise, the PWM IC may be destroyed by external high voltage during solder/desolder.

Design Guideline

PFC Inductor Design

As shown in Figure 15, considering one AC line voltage cycle, the minimum switching frequency $f_{s,min}$ occurs at the peak of the AC line voltage. To avoid audible noise, the minimum switching frequency $f_{s,min}$ must be above audible frequency. The appropriate inductance can be calculated by Equation 5. The minimum switching frequency $f_{s,min}$ may happen in AC maximum or minimum input voltage, depending on the output voltage. Therefore, calculate both the maximum and the minimum input voltages, then choose the lower inductance value.

$$L_b = \frac{\eta \bullet V_{pk}^2 \bullet (V_o - V_{pk})}{4 \bullet P_o \bullet V_o \bullet f_{s.min}} \quad (5)$$

where:
L_b is the PFC inductor,
η is conversion efficiency,
V_{pk} is the peak of the AC line voltage,
P_O is rated output power,
V_O is PFC output voltage,
f_s,min is the minimum switching frequency.

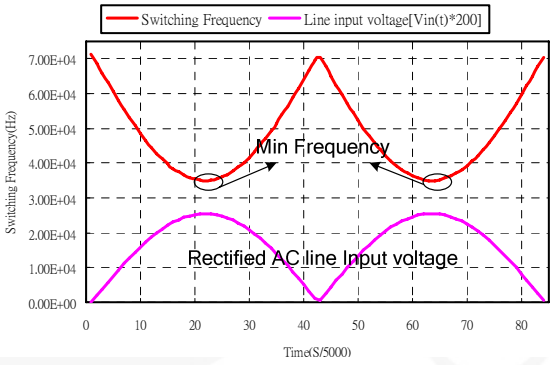


Figure 15. Frequency vs. Input Voltage

The peak inductor current i_{Lpk} can be expressed as:

$$i_{L,pk} = \frac{4 \bullet P_o}{\sqrt{2} \bullet V_{rms.min} \bullet \eta} \quad (6)$$

where $V_{rms.min}$ is the minimum input line rms voltage.

With the internal THD optimization circuit, the real peak inductor current is smaller than calculated. Usually, the real peak current is around 95% of calculated value.

Determine Current-Sense Resistor

The MOSFET on-time and the input current increase with the decreasing AC input voltage or increasing load. The FAN6961 can establish the maximum on-time limit (25μs is recommended) of power MOSFET. Once the voltage on current-sense pin reaches the internal limit V_{CS}, 0.82V typically, the FAN6961 stops the PWM output immediately. Thus, the maximum output power can be designed by the current-sense resistor and maximum on-time limit. In general operation, the maximum on-time occurs at minimum AC input voltage and maximum loading conditions.

When the output power increases from full load to maximum load, the on-time is restricted to the maximum on-time limit first, then the current limit. In the design example, the voltage on the current-sense pin is set to 0.57V at full load and minimum input voltage conditions. At this condition, the maximum power is about 156% of full load at minimum input voltage condition. The current-sense resistor can be calculated from Equation 7. The calculated curve of the MOSFET turn-on time at different loading conditions are shown in Figure 16. The calculated waveforms of the PFC inductor current at two kinds of current limit are shown in Figure 17.

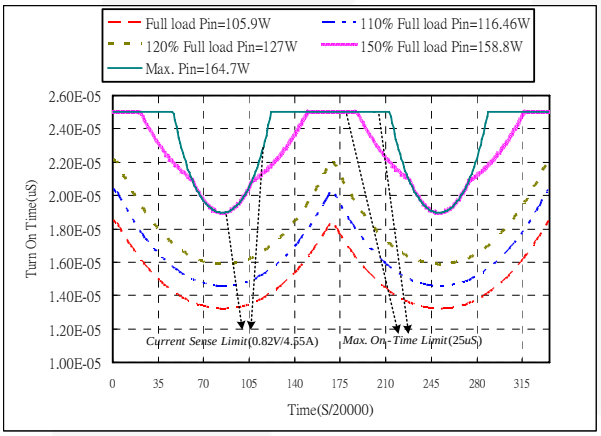


Figure 16. Calculated Curve of the MOSFET Turn-on Time at Different Loading Conditions

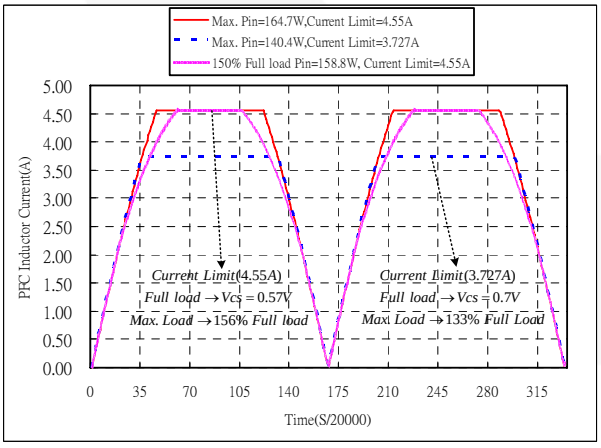


Figure 17. Calculated Waveforms of the PFC Inductor Current at Two Current Limits

$$R_S = \frac{0.57}{I_{L,PK} \bullet 95\%} \quad (7)$$

The FAN6961 current-sense limit, V_{CS}, is 0.82V typically.

From Faraday's law, the number of turns for PFC inductor can be obtained by:

$$N_b = \frac{L_b \bullet I_{L,pk}}{B_{max} \bullet A_e} \bullet 10^6 \quad (8)$$

where:
A_e is the effective area of the core-section,
B_{max} is saturation magnetic flux density.

Determine the Auxiliary Winding

The FAN6961 can perform zero-current detection by sensing the information on an auxiliary winding of the PFC inductor. As discussed previously, when the ZCD voltage is lower than the threshold voltage (1.75V typical), the PWM output is high again and initiates a new switching cycle. However, there is a prerequisite: the zero-current detector voltage must exceed the rising-edge threshold voltage (2.1V typical) before it falls below 1.75V. The minimum rising-edge voltage of zero-current detector input occurs at the peak of the highest AC line voltage, which is equal to $V_O - \sqrt{2} \bullet V_{rms,max} / n$ and must be larger than the ZCD input rising-edge threshold voltage (2.1V typical). The ZCD voltage V_{ZCD} should be established as high as 120% of 2.3V to have a safe margin; therefore, the number of turns for auxiliary winding is obtained as:

$$N_{aux} = \frac{V_{zcd} \bullet 1.2}{V_o - \sqrt{2} \bullet V_{rms.max}} \bullet N_b \quad (9)$$

where $V_{rms,max}$ is the maximum input line rms voltage.

V_{ZCD} is the rising-edge voltage of zero-current detector input.

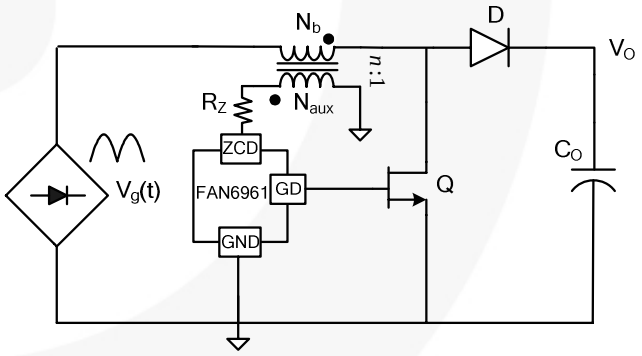


Figure 18. Simplified Power Stage

Calculate On-Time $t_{on.fix}$

The fixed on-time for the specific output power, inductor, and input voltage can be calculated by:

$$t_{on.fix} = \frac{2 \bullet P_o \bullet L_b}{V_{rms}^2 \bullet \eta} \quad (10)$$

where:

L_b is the PFC inductor,
η is conversion efficiency,
P_O is the maximum rated output power,
V_{rms} is the input line rms voltage.

Determine the Output Capacitor C_o

The output capacitor is determined by the requirement of sufficient hold-up time t_{Hold}:

$$C_O = \frac{2 \bullet P_O \bullet t_{hold}}{\left(V_o^2 - V_{O.min}^2\right) \bullet \eta} \quad (11)$$

where t_{Hold} is the output capacitor hold-up time, which is measured from the time the AC input turns off to before the output voltage falls below the minimum operating voltage of the following DC/DC stage.

The output ripple voltage ΔV_O is expressed as:

$$\Delta V_O = \frac{P_O}{\omega \bullet C_O \bullet V_O} \quad (12)$$

where:
ω= 2 π f,
f is AC line frequency,
I_O is the output current.

Determine the Compensation Capacitor C_{EA}

As discussed previously, to achieve a low input current THD, the variation of the on-time within one input AC cycle should be very small. To achieve this, the bandwidth should be lower than 20Hz. The capacitance C_{EA} connected between COMP and GND can be obtained as:

$$C_{EA} = \frac{g_m}{2 \bullet \pi \bullet BW} \quad (13)$$

where BW is PFC control loop bandwidth and establishes it as 20Hz. The error amplifier is a trans-conductance amplifier that converts voltage to current with a 125μmho output conductance.

Design Example

This section shows a design example of a 90W (19V/4.74A) adaptor. From the specification, all critical components are treated and final measurement results are given.

The basic design specification are shown as following:

- AC Input Voltage Range V_{rms}: 90 ~ 264 V_{AC}
- Rated Output Power P_O: 90 W
- Minimum Switching Frequency $f_{s,min}$: 35KHz
- High Regulated Output Voltage: 400V (at 180 ~ 264V_{AC})
- Low Regulated Output Voltage: 250V (at 90 ~ 132V_{AC})

Based on the given design guideline, the critical parameters are calculated and summarized in Table 1:

Table 1. Critical System Parameters

L_b	530μH	$t_{on,fix}$(90V_{rms})	13.86μs
i_{pk}	3.327A	$t_{on,fix}$(132V_{rms})	6.44μs
N_b	65T	$t_{on,fix}$(180V_{rms})	3.46μs
N_{aux}	7T	$t_{on,fix}$(264V_{rms})	1.61μs
C_O	68μF/450V	ΔV_O(V_O = 250V)	14.043V
C_{EA}	1μF	ΔV_O(V_O = 400V)	8.77V

Reference Circuit

The complete circuit diagram is shown in Figure 19 and the Bill of Materials for the PFC stage is shown in Table 2.

Table 2. BOM List of PFC Stage

Reference	Components	Reference	Components
F1	4A/250V	C2	0.33μ/275V
R1	510K	C3	Open
R2	510K	C4	Open
R3	10K	C5	Open
R4	1M	C7	0.47μF/400V
R5	18.7K	C8	0.47μF/400V
R6	1M	C11	2.2μF/50V
R7	430K	C12	68μF/450V
R8	1M	C24	104pF
R13	Open	C25	Open
R14	24K	C27	Open
R15	68K(47K)	C28	Open(22p)
R16	10Ω	C29	221pF
R17	0Ω	Q1	2N-7002
R18	0.18Ω/2W	Q2	2SK-2482/ TO-220
R55	Open	BD1	KBP205G
R56	Open	ZD1	ZD24V
R57	Open	D2	R860/TO-220
R58	Open	D3	1N4148
R59	0Ω	L1	1mH
MOV1	470V/7D	L2	13mH
TR1	055	L4	RM-10/ 530μH
U1	FAN6961	L5	400μH
C1	224pF		

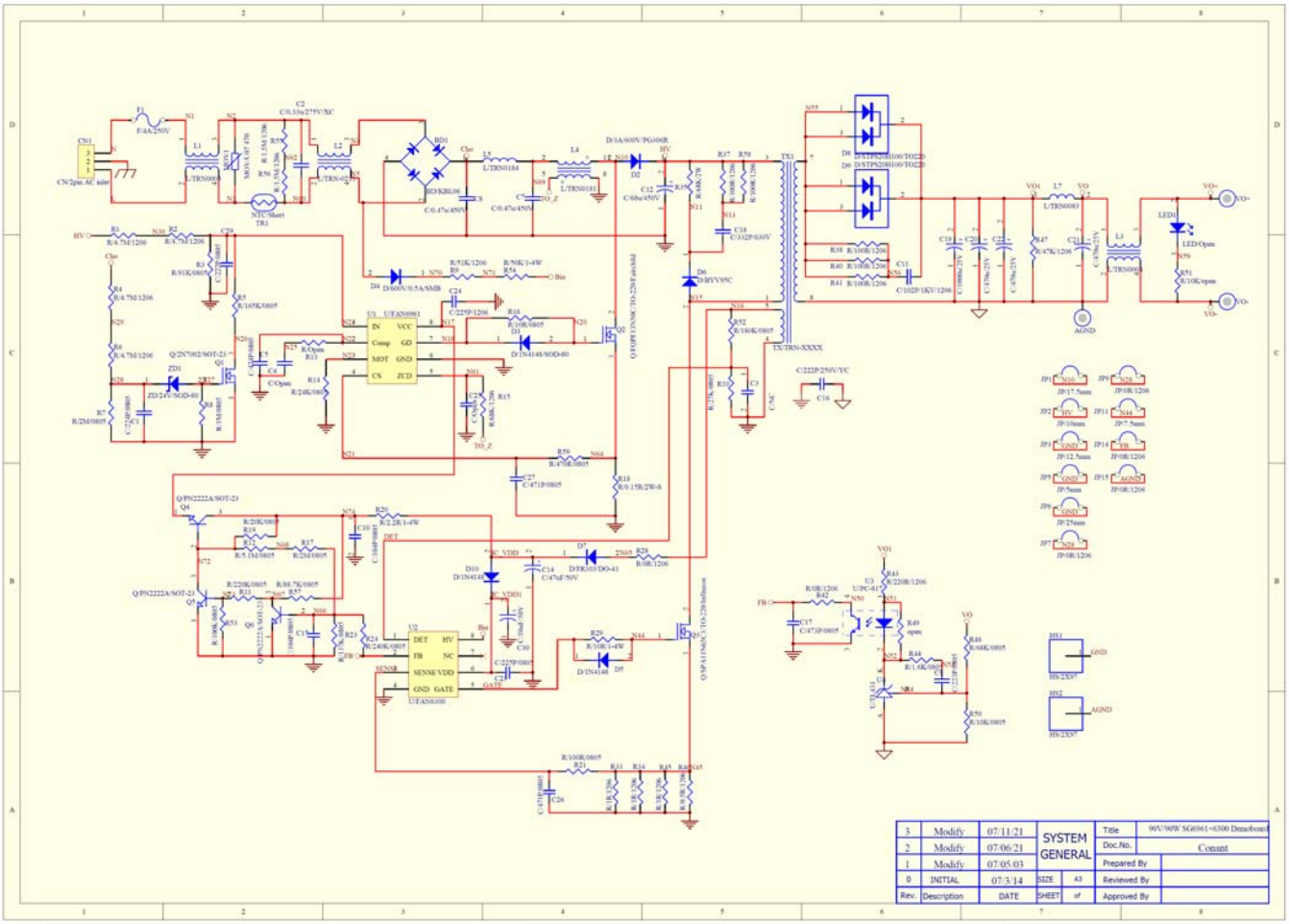


Figure 19. Application Circuit Diagram (90W/19V)