# AN1042/D

# High Fidelity Switching Audio Amplifiers Using TMOS Power MOSFETs

Prepared by: Donald E. Pauly ON Semiconductor Special Consultant

Almost all switching amplifiers operate by generating a high frequency square wave of variable duty cycle. This square wave can be generated much more efficiently than an analog waveform. By varying the duty cycle from 0 to 100%, a net dc component is created that ranges between the negative and positive supply voltages. A low pass filter delivers this dc component to the speaker. The square wave must be generated at a frequency well above the range of hearing in order to be able to cover the full audio spectrum from dc to 20 kHz. Figure 1 shows a square wave generating a sine wave of one–ninth its frequency as its duty cycle is varied.



Figure 1. Switching Amplifier Basic Waveforms

The concept of switching amplifiers has been around for about 50 years but they were impractical before the advent of complementary TMOS power MOSFETs. Vacuum tubes were fast enough but they were rather poor switches. A totem pole circuit with supply voltages of  $\pm 250$  volts would drop about 50 volts when switching a current of 200 milliamps. The efficiency of a tube switching amp could therefore not exceed 80%. The transformer needed to match the high plate impedance to the low impedance speaker filter was impractical as well.



http://onsemi.com

# **APPLICATION NOTE**

With the introduction of complementary bipolar power transistors in the late 1960s, switching amplifiers became theoretically practical. At low frequencies, bipolar transistors have switching efficiencies of 99% and will directly drive a low impedance speaker filter. The requirement for switching frequencies above 100 kHz resulted in excessive losses however. Bipolar drive circuitry was also complex because of its large base current requirement.

With the advent of complementary (voltage/current ratings) TMOS power MOSFETs, gate drive circuitry has been simplified. These MOS devices are very efficient as switches and they can operate at higher frequencies.

A block diagram of the amplifier is shown in Figure 2. An output switch connects either +44 or -44 volts to the input of the low pass filter. This switch operates at a carrier frequency of 120 kHz. Its duty cycle can vary from 5% to 95% which allows the speaker voltage to reach 90% of either the positive or negative supplies. The filter has a response in the audio frequency range that is as flat as possible, with high attenuation of the carrier frequency and its harmonics. A 0.05 ohm current sense resistor (R27) is used in the ground return of the filter and speaker to provide short circuit protection.

The negative feedback loop is closed before the filter to prevent instabilities. Feedback cannot be taken from the speaker because of the phase shift of the output filter, which varies from 0° at dc to nearly 360° at 120 kHz. Since the filter is linear, feedback may be taken from the filter input, which has no phase shift. Unfortunately, this point is a high frequency square wave which must be integrated to determine its average voltage. The input is mixed with the square wave output by resistors R4 and R5 shown in Figure 2. The resultant signal is integrated, which accurately simulates the effect of the output filter. The output of the integrator will be zero only if the filter input is an accurate inverted reproduction of the amplifier input. If the output is higher or lower than desired, the integrator will generate a negative or positive error voltage. This error voltage is applied to the input of the switch controller, which makes the required correction. The integrator introduces a 90° phase shift at high frequencies which leaves a phase margin of nearly 90°.

This document may contain references to devices which are no longer offered. Please contact your ON Semiconductor representative for information on possible replacement devices.

Semiconductor Components Industries, LLC, 2002
August, 2002 – Rev. 3

## AN1042/D



Figure 2. Block Diagram of Class D Amplifier

The switch controller has three main functions. First, it insures that the output duty cycle is never less than 5% or greater than 95%. This is made necessary by the use of ac coupling for the drive. Second, it controls the output duty cycle in response to the error voltage input. This duty cycle is a linear function of the error voltage input. Third, it provides short circuit protection to the amplifier in response to the current sense input. If overcurrent is detected, the error voltage reduced as necessary to bring the current back within limits.

A class B analog amplifier has a theoretical efficiency of 78.5% when producing a sine wave at the point of clipping. A switching amplifier, or so called class D amplifier, must do much better to justify its extra complexity. The switching amplifier described in this paper achieves an efficiency of 92% at its rated power of 72 watts. Its efficiency peaks at 95% for 30 watts output and falls to 50% for 1.5 watts output. These efficiencies result from the good performance of TMOS power MOSFETs at high switching frequencies and the simplicity of complementary drive circuitry. Above the 100 watt level, a switching amplifier costs less than a conventional amplifier although it is slightly more complex. The heatsink size is about one–tenth and the weight is about one–fourth that of a class B amplifier.



A switching amplifier must switch at a frequency well above the highest frequency to be reproduced. A low pass filter must follow the switching stage to eliminate the high frequency square waves and pass the audio to the speaker. High switching frequencies can simplify filter design, but cause excessive losses in the switching devices. Low switching frequencies limit the upper frequency response of the amplifier and complicate filter design. The amplifier described in this paper operates at a switching frequency of 120 kHz. Its response extends down to dc, with an upper -3 dB point of 20 kHz.

The filter chosen here is a 4 pole Butterworth Low Pass which is maximally flat in the passband. It is designed to be driven by a voltage source and loaded into 8 ohms. This type of filter has a transfer function of

$$\mathsf{E} = \frac{1}{\sqrt{1 + \left(\frac{\mathsf{f}}{\mathsf{f}_{\mathsf{C}}}\right)^8}}$$

where f is the frequency of interest and  $f_c$  is the cutoff frequency. At the 120 kHz switching frequency, this filter has a voltage attenuation of 62 dB. With a ±44 volt square wave into the filter at 120 kHz, the maximum residue is a sine wave of about 30 millivolts rms. The filter is only 0.1 dB down at 12.5 kHz and 1 dB down at 17 kHz as shown in Figure 3. The -3 dB point is 20 kHz.

The frequency response of the filter will be flat only if it is properly loaded into 8 ohms. A 16 ohm speaker load will cause high frequency peaking and a 4 ohm speaker will cause high frequency loss. The output impedance of the filter changes across the band as shown in Figure 4. It exhibits a parallel resonance at 11.4 kHz and 35.2 kHz, and a series resonance at 20 kHz. In practice, these resonances cause no difficulty with typical speakers and crossover networks.

This amplifier and a high quality conventional amplifier were both fed pink noise while driving full range speakers. A broad band audio spectrum analyzer with a calibrated microphone was used to measure sound pressure level. The difference in sound pressure level between the two, if any, was well under 1 dB from 60 Hz to 16 kHz.



Output Impedance

The amplifier output impedance at dc is about 4 milliohms and gradually becomes inductive. At 100 Hz, its output impedance is 0.1 ohm giving a damping factor of 80. Damping factor is the ratio of load impedance to amplifier output impedance.

The complementary power MOSFET output stage of the amplifier is shown in Figure 5. It generates a  $\pm 44$  volt square wave whose duty cycle can vary from 5% to 95%. This variable duty cycle square wave is fed to the output filter where the low frequency component is passed on to the 8 ohm speaker. This filter allows frequencies under 20 kHz to pass with negligible loss, but greatly attenuates the switching frequency. Since both sources are connected to a supply rail, a drive of 10 volts peak to peak on each gate insures full turn on. A buffer amp using  $\pm 5$  volts supplies provides this drive.

The 4.7 ohm resistors, R17 and R18, in each gate lead prevents high frequency oscillation during switching. The 12 volt Zeners, CR3 and CR4, serve both as conventional diode clamps and provide static discharge protection. They act as dc restorers, and are made necessary by the ac coupling. The 10 k resistors, R15 and R16, provide a slight discharge path to keep conduction pulses in the clamp

diodes. They also discharge the gates in about 1 millisecond if the drive signal is lost. About 9 volts of turn–on bias is applied to each gate. Tight coupling between the gates prevents simultaneous turn–on of both devices.

The output stage inverts the drive signal and generates rise and fall times of about 30 nanoseconds. It is designed to put out a maximum current of  $\pm 5$  amps down to a frequency of 0.1 Hertz. Below that frequency, maximum current may need to be derated to prevent alternate overheating of each output device. Excessive heatsink temperature increases the ON resistance and the storage time of the source drain diode. The resultant increase in losses can lead to thermal runaway.

The drive waveform duty cycle must be a linear function of the control voltage. The Duty Cycle Controller is shown in Figure 6. A square wave of  $\pm 5$  volts at 120 kHz is coupled through C1 and R1 to integrator U1B. C1 blocks dc and R1 is the integrator resistor. C2 is the integrator capacitor which generates a  $\pm 2$  volt triangle on the output of U1B. R2 provides a small amount of dc leakage to insure that the output has no significant dc component. R3 couples the triangle to the noninverting input of comparator U1D. It improves the waveform by isolating the input capacitance of the comparator from the integrator. The dc offset on the triangle is equal to the offset of U1B and its linearity is better than 1%.

Input audio is applied to the inverting input of U2C through R4. The output square wave of the power amp is applied through R5 to the same summing point. U2C functions as an integrator with C3 as the integrator capacitor. Since R5 is 20 times R4, an inverting voltage gain of 20 must result if the input of U2C is to be at ground. The output of U2C serves as the error voltage and is fed to the inverting input of U1D through R6 and R7. C4 eliminates short spikes on the error buss. Current limiting circuitry is connected to the junction of R6 and R7. When current drawn from the amplifier tries to exceed safe limits, the error voltage is overridden and overcurrent is prevented.



Figure 5. Output Circuit of a Class D Amplifier



Figure 6. Duty Cycle Controller

The  $\pm 2$  volt triangle is applied to the non-inverting input of U1D. The error voltage normally varies over this same range. As it does so, the output of U1D is a square wave at 120 kHz whose duty cycle varies from 0% to 100%. The error voltage will exceed normal limits if the amplifier should clip. In that case, the output drive waveform will lock up at either +5 or -5 volts. If not corrected, the ac coupling of the drive signal would cause a loss of drive to the final amplifiers and associated severe distortion.

To prevent loss of drive, the drive waveform duty cycle must be restricted to the range of 5% to 95%. This is accomplished by the circuit of Figure 7. The 120 kHz square



Figure 7. Schematic of Duty Cycle Limiter and Output Driver

wave clock is fed to a pair of CMOS monostables each of which produces a 250 nanosecond pulse. Only timing resistors are used and internal parasitics serve as the timing capacitance. One monostable produces a pulse on the positive transition of the square wave, and the other produces a pulse on the negative transition. These short pulses are connected to the control inputs of two CMOS analog switches. When the 120 kHz square wave goes positive, the upper CMOS switch turns on and the common terminal is switches to + 5 volts. When the 120 kHz square wave goes negative, the bottom CMOS switch turns on and the common terminal is switched to -5 volts.

Since the drive signal from U1D is fed through R9, it will be overridden if either of the CMOS switches is on. If the error voltage to U1D is out of limits, its output will be locked up at either +5 or -5 volts. The CMOS switches will then act to insure either short negative or positive pulses to the input of U1C. U1C is a comparator used as an inverting buffer between the CMOS switches and the small signal TMOS drivers. These devices have low input capacitance and low output impedance.

The drive signal is fed through R12 to the gates of Q1 and Q2. They function as a low impedance inverting buffer to drive the output stage. Decoupling networks isolate the sources of Q1 and Q2 from the  $\pm 5$  volt supplies. This prevents the disruption of other circuitry by the large current spikes needed to drive the output stages. Note that the feedback path from R5 to the output experiences 5 polarity inversions. They are U2C, U1D, U1C, Q1–Q2 and Q3–Q4. An odd number of inversions is required to make the overall feedback negative.

The current limiting circuitry is shown in Figure 8. R27, a 0.05 ohm noninductive resistor, senses the ground current in the output filter and speaker. The voltage across this resistor is amplifier by op amp U2D. R28 and R29 set the gain of U2D at 10. C11 rolls off the response above 300 kHz. The level at the output of U2D is -0.5 volt per amp of output current. The output of U2D is applied through R8 to the error amp for filter resistance compensation as shown in Figure 6. For every amp drawn by the speaker, the output voltage is increased by about 0.1 volt. This compensates for the loss in the filter and current sensing resistor. The lowered output impedance at low frequencies improves speaker damping.

The amplified current signal at the output of U2D is also routed to the noninverting inputs of U2A and U2B. These op amps are the current limiters. U2A limits negative current and U2B limits positive current. Only U2A will be described since U2B operates in an identical manner. R19 and R21 form a voltage divider with an output of 2.5 volts. This voltage is applied to the inverting input of U2A. When the non–inverting input of U2A is more positive than 2.5 volts, the speaker current is greater than –5 amps. In that case, the output of U2A will rise towards +5 volts. This output coupled through CR1 takes over control of the error voltage buss. A voltage between  $\pm 2$  volts is rapidly reached



Figure 8. Schematic of Current Limiting and Current Sense Amplifier

at the output of CR1 to limit the current at -5 amps. Note that U2B has +5 volts for its output at this time and CR2 is reverse biased. R23 limits the low frequency gain of U2A to 45. R25 in conjunction with C12 limits the high frequency gain. If the output current exceeds -5 amps by as little as 0.1 amp, the output voltage can be reduced to zero from full voltage.

The resistor–capacitor combination of R25 and C12 form a lag compensation filter. They are necessary because the output inductors introduce a  $90^{\circ}$  lag in output current near 1 kHz when the output is shorted. The values chosen for the lag filter are a compromise between speed of response and stability under short circuit conditions. An overcurrent of 0.1 amp requires about 50 microseconds to

reduce the output to zero. At frequencies above 8 kHz, filter phase shift makes the current limiting ineffective. This will not be a problem unless the output is short circuited during high frequency sine wave testing. R30 through R33 set the bias currents for the operational amplifiers and comparators.

The efficiency of a class B amplifier at the point of clipping is  $\frac{\pi}{4}$  or 78.5%. As the output is reduced the efficiency linearly drops to 0% with no voltage out. The average power of music integrated over one second has been measured by the author at one tenth of peak power. This does not seem to vary appreciably with different music or speech as long as they are continuous. Under these conditions, a class B amplifier will have an effective efficiency of 25%. Figure 9 shows a plot of heatsink power loss for a class B amplifier and a switching amplifier as a function of output power. Note that a class B amplifier actually runs hottest at slightly less than half power. Maximum heating occurs at 40% of maximum power. The heat rise varies only 25% as the power changes from 10% to 90% of maximum.

As a result, a switching amplifier has one-tenth of the heatsink requirements of a class B amplifier. Its greater efficiency allows it to use a power supply of one-fourth the size of a class B amplifier power supply. The author used a switching power supply operated off 120 vac line at 20 kHz. If a switching power supply is used, proper shielding must be provided to prevent pickup of power supply spikes by sensitive portions of the amplifier. A discussion of power supplies is beyond the scope of this paper.

Switching amplifiers have a little known property of power supply buss runaway when producing dc or low frequency ac. The origin of this problem can be understood by referring to Figure 10. It shows the current in the positive switch when a sine wave just short of clipping is produced by the amp. During the first half cycle, the switch is on most of the time and power is delivered to the load, with some energy being stored in the output inductor. During the second half cycle, the switch is off most of the time and current flow is reversed through the switch. This reverse current comes from the output inductor, which is returning energy to the positive supply through the source drain diode of Q3. The forward current of the first half cycle tends to drop the positive supply voltage, and the reverse current of the second half cycle will raise it.

It can be shown that the current averaged during the switching cycle in the positive switch is  $\frac{\sin x + \sin^2 x}{2}$ . This function is shown by the dashed curve in Figure 10. The current averaged during the first half cycle of the output sine wave is  $\frac{\pi + 4}{4\pi}$ , which is 0.5683 times peak current. The average current during the second half output of the cycle is  $\frac{\pi - 4}{4\pi}$ , which is 0.0683 times peak.



The average current during the complete cycle is 0.250, being half the average power of a sine wave referenced to peak power. Average reverse current through the switch peaks at 0.125 of average peak forward current. This will cause the voltages in a conventional supply to build to destructive levels in short order, unless the power source is a battery.

Figure 10 only applies to a switching amp that is operated just short of clipping with a normal load. If the amp is operated into a short, conditions worsen. The average forward and reverse currents will both be 0.500. This means that no net power will be taken from the supply when averaged over the whole cycle. This reflects the fact that no power can be delivered into a short circuit.

To accommodate shorts on the output of the amplifier without generating dangerous voltages, special power supply circuitry must be used. These circuits must be able to handle reverse currents on each buss equal to one–half of the peak short circuit output current. Conventional rectifier based supplies will not tolerate reverse current for sustained periods. Large filter capacitors help but they merely postpone the inevitable reckoning. A better solution is coupling between the positive and negative power supply busses.





Figure 11. Voltage Balance Circuit

One means of coupling the positive and negative supplies that has been used successfully by the author is shown in Figure 11. A complementary pair of TMOS power MOSFETs is driven by a square wave at 20 kHz. This drive signal was obtained from the switching power supply used with the amplifier. If lower efficiency is acceptable, the 120 kHz switching amplifier frequency may be used instead. The Ferroxcube E core is gapped to allow a large current without saturation. its primary inductance is 100 microhenries and the primary current is a triangle of  $\pm 5.5$  amps. Any mismatch in the two supply voltages will result in a net average dc component on the square wave going to the primary. A direct current of 3.5 amps can be added to the 11 amp peak to peak triangle before reaching the 9 amp saturation level.

If the +44 volt supply is high, extra energy will be stored in the primary of T1 during the on time of Q5. When Q5 is turned off and Q6 is turned on, the energy is transferred from the primary of T1 through Q6 to the -44 volt supply. The net effect is that the +44 volt buss is reduced in voltage and the -44 volt buss is increased. This restores the balance between the two supplies. If the -44 volt supply is too high, the operation is similar with the roles of Q5 and Q6 reversed. It is important to use Litz wire for the primary of T1 because of the large high frequency component of primary current. An 8 turn secondary winding can be used to generate  $\pm 11$  volts for powering  $\pm 5$  volt regulators for the switching amp. If that is done, the amp will not operate unless the voltage balance circuit is working properly. This is a very important safety feature, since the amplifier can be destroyed if the supply voltages run away.

The losses in the switching amplifier are attributable to on resistance, switching times, diode recovery spikes and the output filter. Diode recovery losses dominate all these losses. The new improved E series devices will greatly reduce these losses because their recovery times are about one fourth as long.

At low frequencies, the principal loss in the output filter is the winding resistance. See Figure 5. The winding resistance is on the order of 40 milliohms which causes a loss of about 0.5%. At 20 kHz, this rises to about 2% due to skin effect. If Litz wire is not used, losses can easily reach 5%. Capacitor losses in the output filter are negligible if multilayer film capacitors are used. The inductors used in the filter must tolerate well over 5 amps of dc without saturation and have very low hysteresis loss. Molypermalloy cores were used first for output filter inductors but their losses were too high. They exhibited third harmonic distortion of 5% in the 5 kHz region as well as severe heating when passing high frequencies. These problems were caused by their excessive hysteresis.

Gapped ferrites wound with #14 solid magnet wire were next used. They cured the high frequency heating and distortion problems. However, the high frequency -3 dB point was 17 kHz instead of the theoretical 20 kHz. This was found to be due to skin effect losses in the windings. Use of #16 Litz wire raised the high frequency cutoff point to 19.5 kHz.

The input inductor must handle 120 kHz triangle current of  $\pm 0.8$  amp during no signal conditions. The loss is about 0.1 watt due to this triangle. The input inductor has 31 turns and saturates at about 10 amps. The output inductor has only 26 turns and saturates at about 12 amps. These currents are well above the 5 amp current limit of the amplifier and insure that the inductors will remain linear. Inductors for higher power filters must use larger cores with appropriate gaps to avoid saturation. Higher voltage capacitors must also be used.

Capacitors used in the filter must have a Q in excess of 100 at 20 kHz and must be nonpolarized. Multilayer film capacitors with a rating of 63 volts dc have been used successfully. If the filter is unloaded and the amplifier is operated in the vicinity of one of its parallel resonance points, excessive voltages will be generated. This problem is most severe at 11.4 kHz. Only 1 volt out of the amplifier under normal conditions will generate 60 volts at the junction of the filter inductors when the output is unterminated. Several amps of current will be generated in the inductors as well, possibly resulting in their saturation. Such high frequency operation can lead to failure of capacitors in the filter and destruction of output switching transistors. The filter may be open circuited with music or speech without damage, since little continuous power exists at the 11.4 kHz resonance point.

Good RF layout practices must be used in construction of the filter. The winding end closest to the core should be used as the input on both inductors. This will provide a measure of shielding against capacitively coupled RFI. The cores and the current sense resistor R27 should be grounded to the same point as the power supply grounds of the output switching transistors. The lead for the input inductor that connects to the switching transistors must be as short as possible to minimize RFI.

The on-resistance of the MTP12N210/12P10 is rated at 0.18 and 0.3 ohms maximum respectively. We will assume that 5 amps is being switched by the two devices. In that case the N channel will dissipate 4.5 watts and the P channel will dissipate 7.5 watts.

At forward currents of 5 amps, the source drain voltage of the N channel will be 0.9 volts and the P channel will be 1.5 volts. If this current is reversed, the drop will be high enough to activate the source drain diode. This will occur for reverse currents of about 3 and 2 amps for the N and P channel devices respectively. Charge stored in the source drain diode causes recovery current spikes when the opposite device turns on. These spikes are the main cause of heating in the switching devices. On resistance losses are somewhat less than expected on the basis of drain resistance calculations because of the voltage clamping effect of the source drain diode during reverse current.

The approximate combined output capacitance of the N and P channel is about 700 pF. Charging and discharging this capacitance takes energy. At  $\pm$ 44 volt supply voltages and 120 kHz, this amounts to about 0.3 watts in each device. This loss is the least significant of the various losses.

When reverse current flows through the source–drain diode, a charge is stored in the form of minority carriers in the junction. When the opposite switch turns on, this diode acts as a momentary short until these carriers are recombined. This short exists for about 0.1 microsecond for the N channel and slightly less for the P channel. During this time, the opposite switch will be conducting a current of about 12 amps in an attempt to clear out the carriers stored by the previous 5 amp current. The 88 volts across the switch during this time causes a peak dissipation of 1056 watts. The average power during the 120 kHz switching cycle will be 10 watts for the N channel and 12 watts for the P channel.

Diode recovery losses dwarf all other losses. When the switching devices get hot, their diode storage time increases This aggravates the problem and can lead to thermal runaway. The increase in loss with temperature can be mistaken for on resistance increase. Remember that a slow diode heats the opposite switch. The P channel therefore takes the blame for the slower N channel diode. The short high current pulses cause troublesome spikes on power supply busses and generate RFI. The author has found dramatic differences in the recovery times of power MOSFETs from various manufacturers. In several cases, devices of lower on resistance caused much higher losses in the opposite switch due to their slower diodes.

When we add all losses, we get a total of 14.8 watts for the N channel and 19.8 watts for the P channel. The normal conditions of 50% duty cycle for each device gives losses of 7.5 and 10 watts respectively. To avoid overheating, short circuits must be limited to 5 minutes. With normal sine wave output of 72 watts, the N channel dissipates 2 watts and the P channel dissipated 3 watts. Heatsinks used must limit the temperature of the switching devices at 80°C to prevent thermal runaway caused by increased diode recovery losses.

The three components of switching loss are drain resistance, drain capacitance and diode recovery. Drain resistance loss varies only as the square of the current. Drain capacitance loss varies as the product of the drain capacitance, the square of the supply voltages, and the switching frequency. Diode recovery loss varies as the product of the supply voltage, switching frequency, and diode recovery time. Rise time has little effect on diode recovery loss. The best way to reduce losses is with the new E series TMOS with improved source drain diodes. The only other way to reduce loss is to lower the switching frequency. Lower on resistance will have only a small effect on overall loss.

It is desirable to switch at the lowest possible frequency in order to reduce losses in the output devices. On the other hand, low frequencies can introduce 2nd harmonic distortion in the the signal and complicate the output filter design. Tables 1 and 2 show the spectrum of the output of a switching amplifier before the filter as derived by Fourier analysis. The spectrum shown is for a sine wave of various levels of 20 kHz output for carriers of 80 and 100 kHz. Note that the 100 kHz carrier generates no even harmonics. The 80 kHz carrier generates a substantial amount of even harmonics.

Table 1. Frequency Spectrum of Switching Amplifier
Carrier Frequency = 80 kHz with 20 kHz Sine Wave Modulation

Harmonic	Percent of Rated Power		
Number	100%	50%	25%
Fundamental	0.981	0.498	0.250
2	0.186	0.048	0.012
3	0.052	0.007	0.001
4	0.600	1.084	1.224
5	0.118	0.018	0.002
6	0.362	0.130	0.035
7	0.309	0.390	0.235
8	0.192	0.017	0
9	0.065	0.328	0.226
10	0.217	0.176	0.056

Harmonic	Percent of Rated Power		
Number	100%	50%	25%
Fundamental	0.988	0.498	0.25
2	0	0	0
3	0.183	0.053	0.014
4	0	0	0
5	0.600	1.084	1.224
6	0	0	0
7	0.506	0.147	0.036
8	0	0	0
9	0.366	0.391	0.235
10	0	0	0

Table 2.	Frequency	Spectrum	of Switching	Amplifier
Carrier F	requency – 10	0 kHz with 2	0 kHz Sine Wav	Modulation

With both the 80 and 100 kHz carriers, a 6 pole Butterworth filter will be necessary in order to reduce the residual carrier to acceptable levels. It has a much sharper cutoff than a 4 pole filter and a transfer function of

$$E_{out} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^{12}}}$$

A cutoff frequency of 20 kHz will be assumed.

Note that the carrier increases as output level is reduced. The carrier for 100%, 50% and 25% output is 0.600, 1.084, and 1.224 respectively. The 80 kHz and 100 kHz carriers will be attenuated by 72 and 84 dB respectively. The filter in the amplifier described here attenuates its 120 kHz carrier by 62 dB.

With an 80 kHz carrier a lower sideband will occur at 40 kHz and will have an amplitude of 18.6% of the fundamental at full output. At half output, this sideband will be reduced to 9.6% and further reduced to 4.8% at one–fourth output. This sideband will appear as second harmonic distortion of the fundamental. After the filter, second harmonic levels will be 0.3%, 0.15%, and 0.075% for full, half, and quarter output levels. At full output the fundamental is only 98% of normal. Second harmonic distortion does not occur with a 100 kHz carrier and 20 kHz modulation.

The practical lower limit for the switching frequency appears to be 4 times the maximum signal frequency. Even if the difficulties associated with modulation are overcome, operation at 3 times signal frequency will require an 8 pole Butterworth filter. This will negate any advantage in lower switching losses. At this low carrier frequency, the first lower side band appears on top of the output frequency. An undesirable beat between that sideband and the output frequency results.

As the switching frequency is lowered, the error voltage integrator in Figure 6 must be made more sluggish to keep the ac component of the error voltage within common mode range of the duty cycle comparator. This effectively reduces the high frequency feedback and increases the distortion in the vicinity of 5 kHz. It also slows the transient response of the amplifier. More exotic means may be used for filtering the error voltage, but many of these introduce phase shift that makes the feedback loop unstable.

One of the more outstanding features of a switching amplifier is that it has absolutely no crossover distortion. This is true only so long as there are no operational amplifiers or analog transistors in the signal path that have such distortion. In the amplifier described here, the MC14573/575 series of operational amplifiers have class A output stages that meet this criterion. Digital circuitry passing the variable duty cycle waveform cannot introduce crossover distortion.

Conventional amplifiers overheat readily when operated into highly reactive loads. The power wasted in a class B amplifier with a reactive load is  $\frac{4}{4-\pi} = 4.66$  times the power wasted with a resistive load. A 600 Hz test was done using a 2 millihenry choke for a load. A 1000 Hz test was also done using a 20 microfarad polypropylene capacitor as a load. Both have a reactance of 8 ohms at the test frequency. The only results of note were slight heating of the choke and lack of any appreciable power taken from the line. Heatsink temperatures were the same as when a resistive load was used. A conventional amplifier with normal sized heatsinks would have burned up under those conditions. If reactive loads are driven, resonances must be avoided in the output filter.

During the later stages of development, the author received a complaint about an audible high frequency whine coming from the amplifier. A few tenths of a volt of 10 kHz sinewave were found on the outputs of both channels. This 10 kHz signal was locked to the power supply 20 kHz. No flip flops existed that were capable of dividing the power supply frequency by two. Shorting the input of the amplifier did not help. An audio spectrum analyzer finally found a few millivolts of 10 kHz signal riding on the 120 kHz triangle.

An MC14046 Phase Locked Loop had been used to lock the switching frequency to the power supply frequency. Hunting in the loop was producing the 10 kHz. This caused a small amount of am and fm on the 120 kHz triangle. This PLL has about 0.1 microsecond of time crossover distortion in the vicinity of phase lock. The distortion comes from internal lead lag flip flop switching near lock. Introducing a few tenths of a microsecond dc offset with a bias resistor cured the problem. Great care must be taken to achieve a stable loop. If a PLL is not used, the power supply should be driven at a frequency synchronous with the switching frequency to avoid troublesome beats and distortion products.

A complete discussion of RFI elimination is also beyond the scope of this paper. The author operated the left and right channels of the amplifier out of phase at their switching frequency to minimize RFI. Proper shielding and layout techniques must be followed and a line filter will be necessary.

With paralleled devices, larger heatsinks, and redesigned output filters it is feasible to drive loads of less than 8 ohms. The new E series devices can be operated much closer to their maximum ratings in switching service. The availability of E series devices in 250 volt ratings will make 70.7 volt line amps feasible without transformers. When the E series become available at 500 volt ratings, they will make it practical to generate 120 vac from switching amplifiers. Computer back up power supply and 50 Hz power generation are two promising applications for such devices.

## AMPLIFIER PERFORMANCE

#### **Table 3. Harmonic Distortion**

Frequency	% Distortion
10 Hz	0.08
100 Hz	0.08
1.0 kHz	0.19
10 kHz	0.31

- Intermodulation Distortion: 0.24% (60 Hz and 6 kHz mixed at 4:1)
- Signal to noise ratio: 100 dB below full rated power
- Power bandwidth: dc to 20 kHz
- Damping factor: 80
- Efficiency: 92% at 72 Watts of output power
- NOTE: Distortion measurements taken with Tektronix SG505 oscillator and AA501 analyzer. Output set to  $\pm$ 30 Volts into 8 Ohms.



Horizontal: 100 µs/Division



### **CLASS D AMPLIFIER PARTS LIST**

#### Capacitors

C1, C7, C8: 0.1, 63 Volts C2, C3, C12, C13: 470 pF C4, C11: 47 pF C5, C6, C9B: 0.47, 63 Volts C9A: 1, 63 Volts C10A: 0.22, 63 Volts C10B: 0.15, 63 Volts

#### Diodes

CR1, CR2: 1N4148 CR3, CR4: 1N5242B

### Inductors

L1: 98 µH (31 Turns) L2: 68 µH (26 Turns)

## Resistors

R1, R15, R16, R25, R26, R30, R31, R32, R33: 10 k R2: 1 m R3: 470 R4: 4.99 k, 1% R5: 100 k, 1% R6, R7, R10, R11: 4.7 k R8: 470 k R9: 2.2 k R12, R13, R14: 22 R28: 1 k, 1% R17, R18: 4.7 R19, R20, R21, R22, R29: 10 k, 1% R23, R24: 220 k R34: 100 R27: 0.05, 1%, 2 Watts, non-inductive All resistors 1/4 W unless otherwise noted. All resistors 5% unless otherwise noted. All resistor values are Ohms unless otherwise noted. All capacitors 1000 V ceramic unless otherwise noted. All capacitor values are µFd unless otherwise noted.

# Integrated Circuits

U1: MC14575 U2: MC14573 U3: MC14528 U4: 14066

## Transistors

Q1: VP0300L Q2: VN0300L Q3, Q6: MTP12P10 Q4, Q5: NTP12N10

NOTES: T1, L1 and L2 use Ferroxcube EC35/35G gapped ferrites with #16 Litz wire. U4C, U4D and U1A are not used.



Figure 13. Schematic for Class D Amplifier

## AN1042/D

**ON Semiconductor** and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

#### PUBLICATION ORDERING INFORMATION

#### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA **Phone:** 303–675–2175 or 800–344–3860 Toll Free USA/Canada **Fax:** 303–675–2176 or 800–344–3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850 Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.

AN1042/D