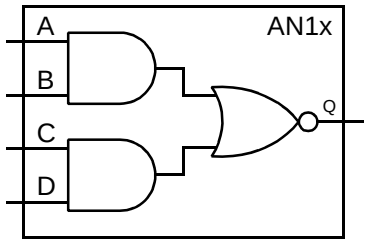
Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.0	1.0	1.0	2.1
D	1.0	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	2.0	TBD	2.3
AN12	4.0	TBD	6.3
AN14	4.0	TBD	7.9
AN16	8.0	TBD	14.7

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN11	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.19 0.20	0.24 0.25	0.40 0.40	0.55 0.55	0.65 0.65
AN12	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.38	0.43 0.48	0.56 0.61	0.70 0.77	0.81 0.89
AN14	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.40	0.50 0.53	0.60 0.64	0.70 0.74	0.81 0.85
AN16	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.35	0.46 0.49	0.55 0.58	0.64 0.68	0.75 0.78

Delay will vary with input conditions. See page 2-17 for interconnect estimates.