DATA SHEET

Part No.	AN12975A
Package Code No.	ULGA020-L-0404

Contents

AN12975A

Stereo BTL amplifier IC with built-in AGC (I^2C bus-control correspondence)

■ Overview

AN12975A is the stereo BTL amplifier which contained the AGC circuit for clip prevention of a speaker output. This IC performs a mode change by the I^2C bus control system.(Standby function ON/OFF change etc.)

■ Features

- Selection by I^2C bus control is possible in the on-level of AGC. (3-bit, 8-step)
- Selection by I^2C bus control is possible in an attack/recovery time of AGC. (attack: 2-bit , recovery: 3-bit)
- The resistance and the capacitor of a detector circuit which were being used for the conventional AGC are unnecessary.
- In order to realize high efficiency of output power, it adopts CMOS power amplifier circuit .

■ Applications

- Audio amplifier for mobile, such as a cellular phone

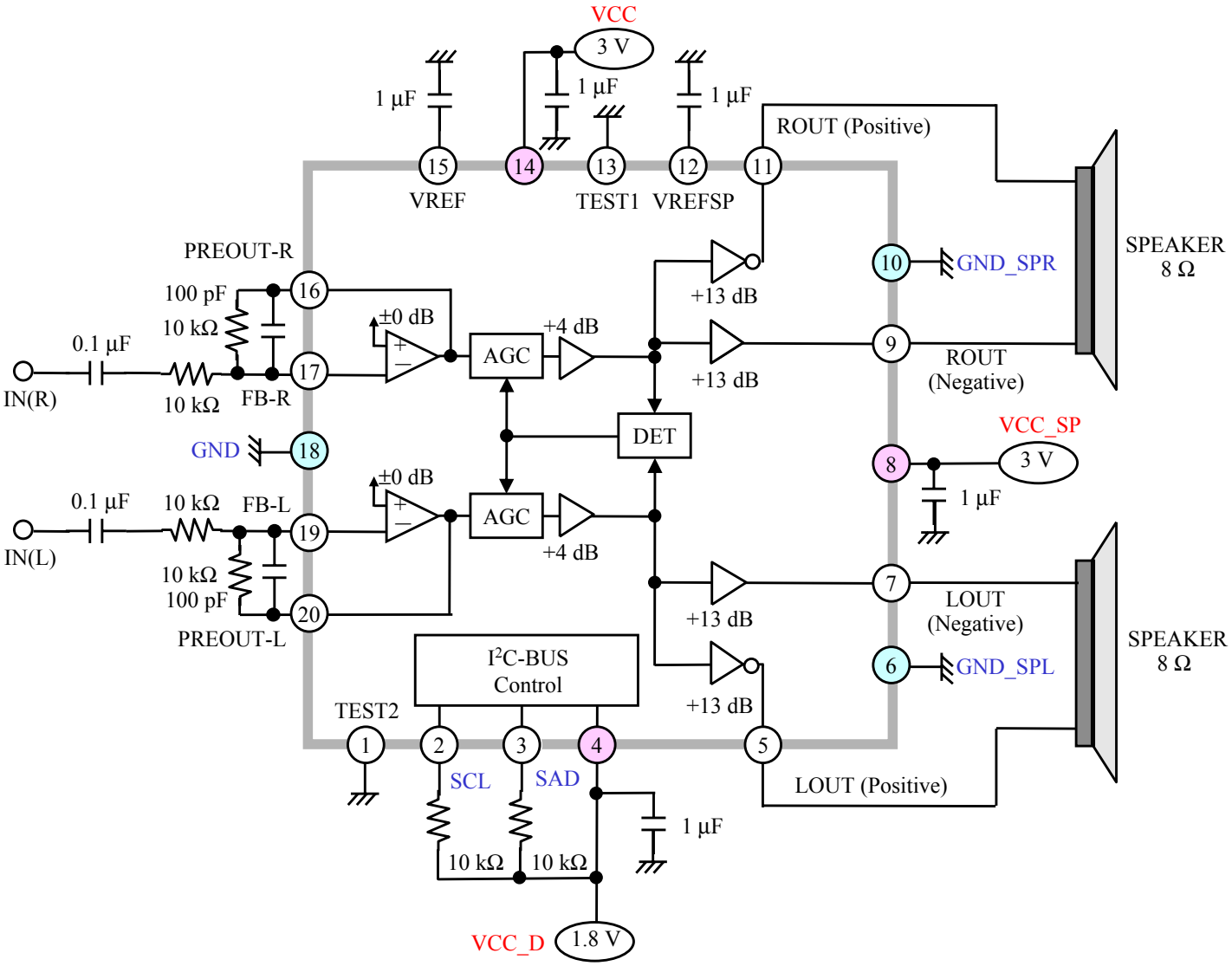
■ Package

- 20 pin plastic non lead package of four directions (LGA Type)

■ Type

- Silicon Monolithic Bi-CMOS IC

■ Application Circuit Example (Block Diagram)



Note) This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	TEST2	—	Terminal for testing (please connect to Ground)
2	SCL	Input	SCL
3	SAD	Input / Output	SDA
4	VCC_D	Power Supply	Power supply VCC_D for logic circuit
5	LOUT_POS	Output	SP amplifier L-ch. output (+)
6	GND_SPL	Ground	Ground for SP L-ch. amplifier system
7	LOUT_NEG	Output	SP amplifier L-ch. output (–)
8	VCC_SP	Power Supply	Power supply VCC_SP for SP output
9	ROUT_NEG	Output	SP amplifier R-ch. output (–)
10	GND_SPR	Ground	Ground for SP R-ch. amplifier system
11	ROUT_POS	Output	SP amplifier R-ch. output (+)
12	VREF_SP	Input	Terminal of reference voltage for SP output circuit
13	TEST1	—	Terminal for testing (please connect to Ground)
14	VCC	Power Supply	Power supply VCC
15	VREF	Input	Terminal of reference voltage
16	PREOUT_R	Output	First stage amplifier output R-ch.
17	FB_R	Input	Negative feedback input stage amplifier R-ch.
18	GND	Ground	Ground
19	FB_L	Input	Negative feedback input stage amplifier L-ch.
20	PREOUT_L	Output	First stage amplifier output L-ch.

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	VCC	3.6	V	*1
		VCC_D	3.6		
		VCC_SP	5.0		
2	Supply current	I_{CC}	—	A	—
3	Power dissipation	P_D	222	mW	*2
4	Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
5	Storage temperature	T_{stg}	–55 to +150	°C	*3

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the • P_D – T_a diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	VCC	2.7 to 3.3	V	
	VCC_D	1.7 to 2.6		
	VCC_SP	2.7 to 4.5		

Note) The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Electrical Characteristics at VCC = 3.0 V , VCC_D = 1.8 V , VCC_SP = 3.0 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Circuit Current								
1	Circuit current 1A at non-signal (VCC)	IVCC1A	VCC = 3.0 V, Non-signal STB = OFF, SP = ON, AGC = ON	1.5	3.9	6.0	mA	
2	Circuit current 2A at non-signal (VCC_SP)	IVCC2A	VCC_SP = 3.0 V, Non-signal STB = OFF, SP = ON, AGC = ON	1.0	13	24	mA	
3	Circuit current 3A at non-signal (VCC_D)	IVCC3A	VCC_D = 1.8 V, Non-signal STB = OFF, SP = ON, AGC = ON	—	0.1	10	µA	
4	Circuit current 1B at non-signal (VCC)	IVCC1B	VCC = 3.0 V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
5	Circuit current 2B at non-signal (VCC_SP)	IVCC2B	VCC_SP = 3.0V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
6	Circuit current 3A at non-signal (VCC_D)	IVCC3B	VCC_D = 1.8 V, Non-signal STB = ON, SP = OFF, AGC = ON	—	0.1	1.0	µA	
7	Circuit current 1C at non-signal (VCC)	IVCC1C	VCC = 3.0 V, Non-signal STB = OFF, SP = OFF, AGC = ON	1.5	3.7	6.0	mA	
8	Circuit current 1C at non-signal (VCC_SP)	IVCC2C	VCC_SP = 3.0 V, Non-signal, STB = OFF, SP = OFF, AGC = ON	—	0.3	1.0	mA	
9	Circuit current 1C at non-signal (VCC_D)	IVCC3C	VCC_D = 1.8 V, Non-signal STB = OFF, SP = OFF, AGC = ON	—	0.1	10	µA	
Input/output characteristics								
11	SP reference output level	VSPOL VSPOR	Vin = –31.0 dBV , f = 1 kHz RL = 8 Ω	–9.5	–8.0	–6.5	dBV	
12	SP reference output distortion	THSPOL THSPOR	Vin = –31.0 dBV , f = 1 kHz RL = 8 Ω , to THD 5th	—	0.07	0.5	%	
13	SP reference output noise voltage	VNSPOL VNSPOR	Non-Signal using A curve filter	—	–78	–71	dBV	
14	SP maximum rating output	VMSPOL VMSPOR	THD = 10% , f = 1 kHz RL = 8 Ω , AGC = OFF	300	500	—	mW	
15	output level at power save	VSSPOL VSSPOR	Vin = –31.0 dBV , f = 1 kHz RL = 8 Ω , using A curve filter	—	–114	–90	dBV	
16	SP AGC output level 1	VSPOA1L VSPOA1R	Vin = –17.0 dBV , f = 1 kHz RL = 8 Ω AGC－SELECT = [100]	3.0	4.0	5.0	dBV	
17	SP AGC output level 2	VSPOA2L VSPOA2R	Vin = –12.0 dBV , f = 1 kHz RL = 8 Ω AGC – SELECT = [100]	3.0	4.0	5.0	dBV	

■ Electrical Characteristics at VCC = 3.0 V , VCC_D = 1.8 V , VCC_SP = 3.0 V (continued)

Note) T_a = 25°C±2°C unless otherwise specified.

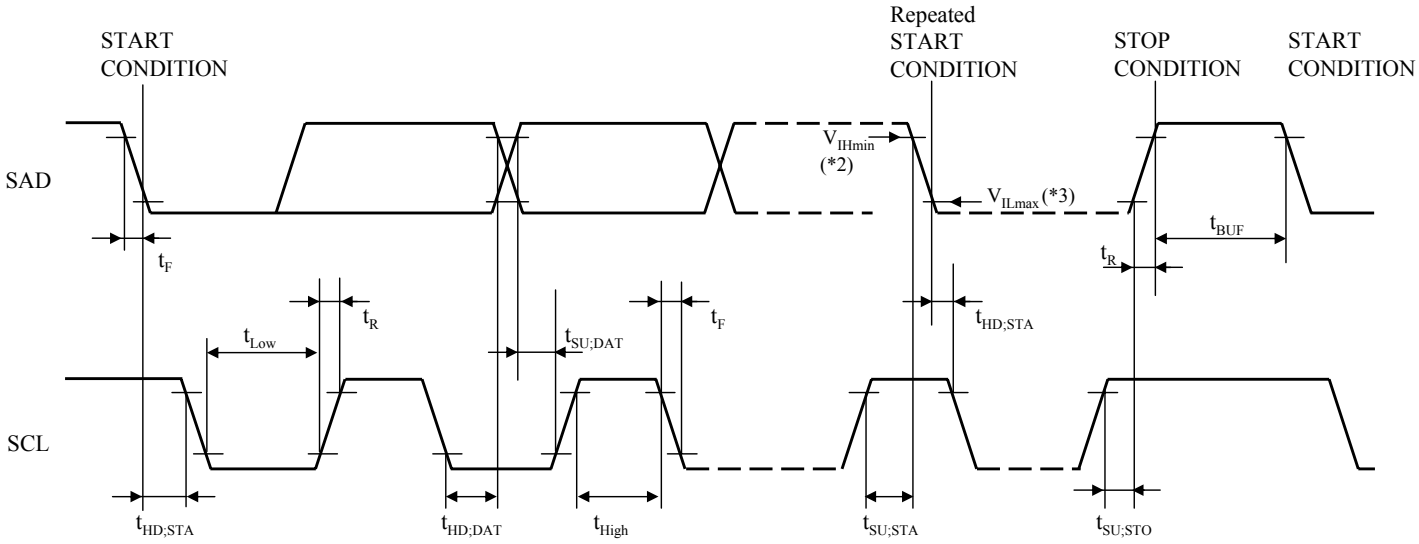
B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
43	SCL, SDA signal input low level	V_{IL}		– 0.5	—	0.3 × VCC_D	V	
44	SCL, SDA signal input low level	V_{IH}		0.7 × VCC_D	—	VCC_D + 0.5	V	
45	SDA output signal low level	V_{OL}	Open corrector, Sync current: 3 mA	0	—	0.2 × VCC_D	V	
46	SCL, SDA signal input current	I_i	Input voltage: 0.1 V to 1.7 V	–10	—	10	µA	
47	SCL maximum frequency of signal input	f_{SCL}		0	—	400	kHz	

■ Electrical Characteristics (Reference values for design) at VCC = 3.0 V , VCC_D = 1.8 V, VCC_SP = 3.0 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
66	Bass free time between a condition of stop and a condition of start	t_{BUF}		1.3	—	—	µs	*1
67	Setup time of a condition of start	$t_{SU;STA}$		0.6	—	—	µs	*1
68	Hold time of a condition for satart	$t_{HD;STA}$		0.6	—	—	µs	*1
69	"L" time of SCL clock	t_{Low}		1.3	—	—	µs	*1
70	"H" time of SCL clock	t_{High}		0.6	—	—	µs	*1
71	rising time of SDA , SCL signal	t_R		—	—	0.3	µs	*1
72	fall time of SDA,SCL signal	t_F		—	—	0.3	µs	*1
73	Data setup time	$t_{SU;DAT}$		0.1	—	—	µs	*1
74	Data hold time	$t_{HD;DAT}$		0	—	0.9	µs	*1
75	Rising up time of a condition of stop	$t_{SU;STO}$		0.6	—	—	µs	*1

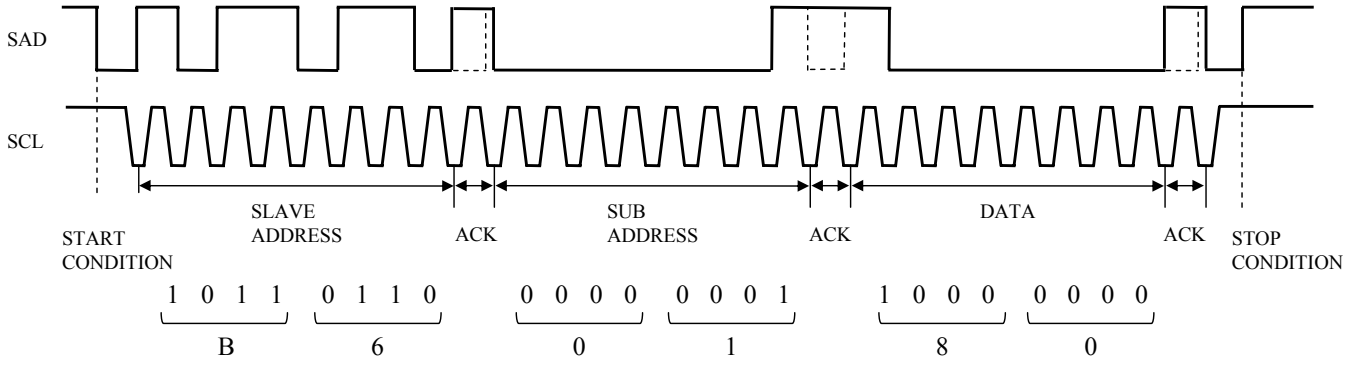
Note) *1: All values are V_{IHmin} (*2) and V_{ILmax} (*3) level standard.
*2: V_{IHmin} is the minimum limit of the signal input high level.
*3: V_{ILmax} is the maximum limit of the signal input low level.



■ Technical Data

- I^2C-bus Mode

1. Write Mode



Example of transmission messages

Two transmission messages (i.e., the SCL and SDA) are sent in synchronous serial transmission. The SCL is a clock with fixed frequency. The SDA indicates address data for the control of the reception side, and is sent in parallel in synchronization with the SCL. The data is transmitted in 8-bit, 3 octets (bytes) in principle, where every octet has an acknowledge bit. The following description provides information on the structure of the frame.

<Start Conditions>

When the level of the SDA changes to low from high while the level of the SCL is high, the data reception of the receiver will be enabled.

<Stop Conditions>

When the level of the SDA changes to high from low while the level of the SCL is high, the data reception of the receiver will be aborted.

<Slave Address>

The slave address is a specified one unique to each device. When the address of another device is sent, the reception will be aborted.

<Sub Address>

The sub address is a specified one unique to each function.

<Data>

Data is information under control.

<Acknowledge Bit>

The acknowledge bit is used to enable the master to acknowledge the reception of data for each octet. The master acknowledges the data reception of the receiver by transmitting a high-level signal to the receiver and receiving a low-level signal returned from the receiver as shown by the dotted lines in Fig.
The communication will be aborted if the low signal is not returned.

The SDA will not change when the level of the SCL is high except start or stop conditions are enabled.

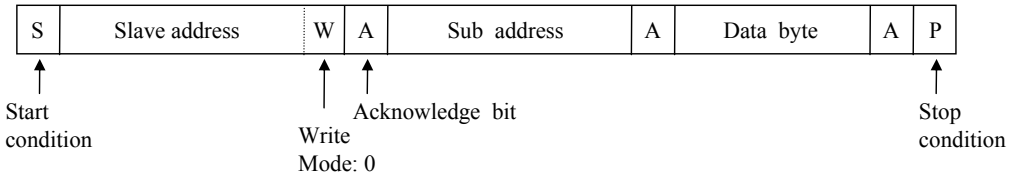
■ Technical Data (continued)

- I²C-bus Mode (continued)

1. Write Mode (continued)

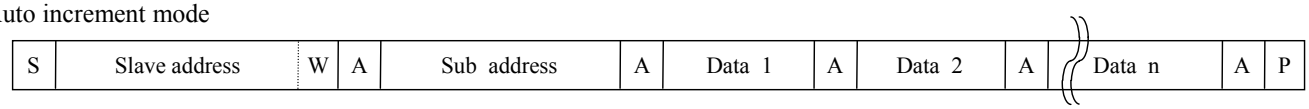
(a) I²C-bus PROTOCOL

- Slave address: 10110110 (B6Hex)
- Format (normal)



(b) Auto increment

- Sub-address 0*Hex: Auto increment mode
  (When the data is sent in sequence, the sub address will change one by one and the data will be input.)
- Auto increment mode



(c) Initial condition

The initial state of the device is not guaranteed. Therefore, the input of 00Hex resister-D0 (Note.1) will be absolutely 0, when the power is turned ON.

(d) Sub-address Byte and Data Byte Format

Sub-address	Data byte MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
*0Hex	*	*	0 (Note.2)	0 (Note.2)	AGC 0 → OFF 1 → ON	SP Save 0 → ON 1 → OFF	Standby 0 → ON 1 → OFF	0 (Note.1)
*1Hex	AGC-ON data bit3	AGC-ON data bit2	AGC-ON data bit1	AGC-REC data bit3	AGC-REC data bit2	AGC-REC data bit1	AGC-ATT data bit2	AGC-ATT data bit1
*2Hex	0 (Note.2)	0 (Note.2)	0 (Note.2)	*	*	0 (Note.2)	0 (Note.2)	0 (Note.2)

0 (Note.2) ← Please use these bit only Data = "0", because they are used by our company's final test and fine-tuning AGC-on level.

<00Hex Register>
D0, D4, D5, D6, D7: Always set to 0
D1: Standby ON/OFF switch
D2: SP Save ON/OFF switch
D3: AGC ON/OFF switch
<01Hex Register>
D0, D1 : AGC-attack-time selection
D2, D3, D4: AGC-recovery-time selection
D5, D6, D7: AGC-on-level selection
<02Hex Register>
D0 to D7: Always set to 0 (test&adjust mode)

■ Technical Data (continued)

- I²C-bus Mode (continued)

1. Write Mode (continued)

(e) AGC-attack-time selection

Write 01Hex Register		Attack time
D1	D0	
0	0	0.5 ms
0	1	1 ms
1	0	2 ms
1	1	4 ms

(f) AGC-recovery-time selection

Write 01Hex Register			Recovery time
D4	D3	D2	
0	0	0	1.0 s
0	0	1	1.5 s
0	1	0	2.0 s
0	1	1	3.0 s
1	0	0	4.0 s
1	0	1	6.0 s
1	1	0	8.0 s
1	1	1	12.0 s

(g) AGC-on-level selection (at VCC = 3.0 V, VCC_SP = 3.0V)

Write 01Hex Register			AGC On Level	Output Po (Ω)	VCC_SP (Recommend)
D7	D6	D5			
0	0	0	0 dBv	125 mΩ	-
0	0	1	1 dBv	157 mΩ	-
0	1	0	2 dBv	198 mΩ	-
0	1	1	3 dBv	249 mΩ	-
1	0	0	4 dBv	314 mΩ	3.0 V ≤
1	0	1	5 dBv	395 mΩ	3.3 V ≤
1	1	0	6 dBv	498 mΩ	3.7 V ≤
1	1	1	7 dBv	626 mΩ	4.1 V ≤ *

Note) *: We recommend more than VCC = 2.9 V for 7 dBV output level.

■ Technical Data (continued)

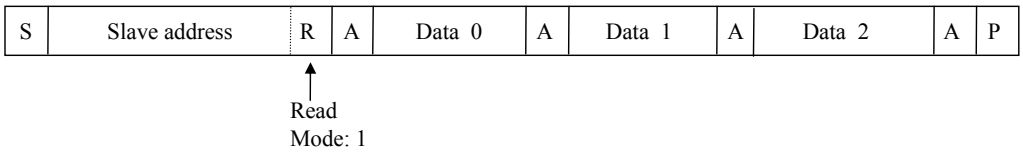
- I²C-bus Mode (continued)

2. Read Mode

(a) I²C-bus PROTOCOL

・Slave address 10110111(B7Hex)

・Format



Note) At the slave address input, it is sequentially output from data 0.
There is no necessity for inputting the sub-address.

(b) Sub-address Byte and Data Byte Format

	MSB			Data byte				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Data 0	Sub address *0Hex Latch data [D7]	Sub address *0Hex Latch data [D6]	Sub address *0Hex Latch data [D5]	Sub address *0Hex Latch data [D4]	Sub address *0Hex Latch data [D3]	Sub address *0Hex Latch data [D2]	Sub address *0Hex Latch data [D1]	Sub address *0Hex Latch data [D0]
Data 1	Sub address *1Hex Latch data [D7]	Sub address *1Hex Latch data [D6]	Sub address *1Hex Latch data [D5]	Sub address *1Hex Latch data [D4]	Sub address *1Hex Latch data [D3]	Sub address *1Hex Latch data [D2]	Sub address *1Hex Latch data [D1]	Sub address *1Hex Latch data [D0]
Data 2	Sub address *2Hex Latch data [D7]	Sub address *2Hex Latch data [D6]	Sub address *2Hex Latch data [D5]	Sub address *2Hex Latch data [D4]	Sub address *2Hex Latch data [D3]	Sub address *2Hex Latch data [D2]	Sub address *2Hex Latch data [D1]	Sub address *2Hex Latch data [D0]

Purchase of Panasonic I²C components conveys a license under the Philips I²C patent right to use these components in an I²C systems, provided that the system conforms to the I²C standard specification as defined by Philips.

- Operating temperature guarantee of I²C-bus Control

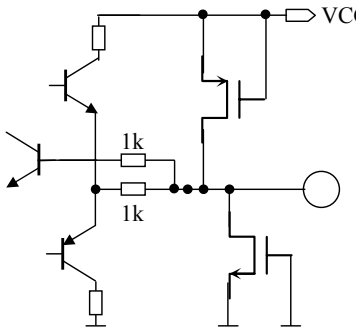
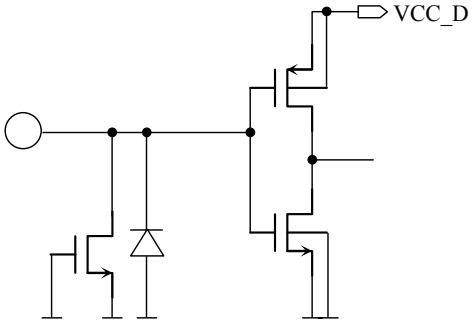
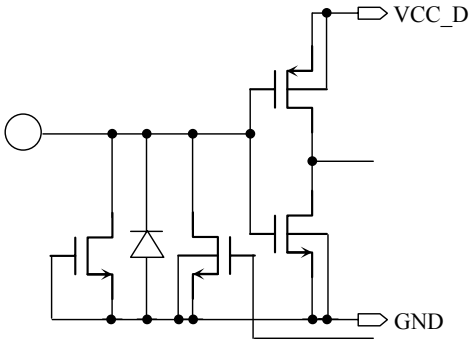
The performance in the ambient temperature of operation is guaranteed theoretically in the design at normal temperature (25°C) by inspecting it at a speed of the clock that is about 50% earlier regarding the operating temperature guarantee of I²C-bus Control.

But the following characteristics are logical values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics ,Panasonic will respond in good faith to customer concerns.

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions

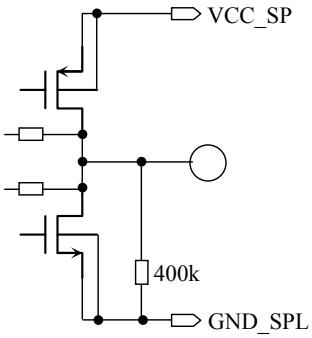
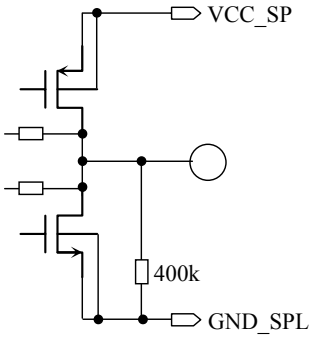
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
1	Test2 Hi-Z		TEST mode output pin It is Hi-Z at normal operation. Please connect to GND.
2	SCL Hi-Z		I^2C-bus SCL pin
3	SAD Hi-Z		I^2C-bus SDA pin
4	VCC_D 1.8 V(typ.)	—	Power supply pin for I^2C-bus

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

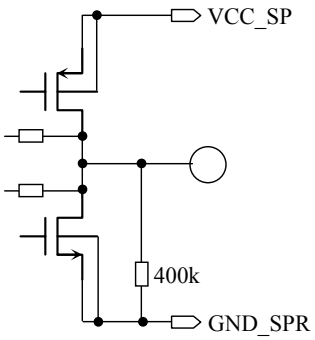
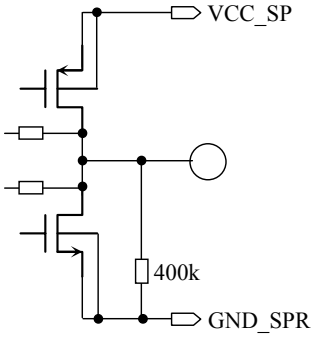
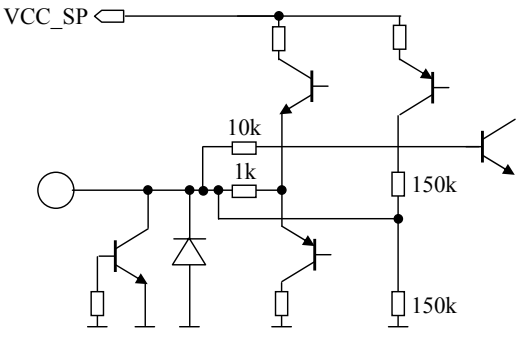
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
5	LOUT_POS DC 1.45 V		L-ch. positive speaker output pin
6	GND_SPL	—	Ground pin for L-ch. speaker output
7	LOUT_NEG DC 1.45 V		L-ch. negative speaker output pin
8	VCC_SP 3.0 V(typ.)	—	Power supply pin for speaker output

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

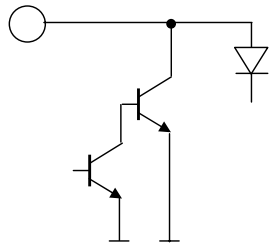
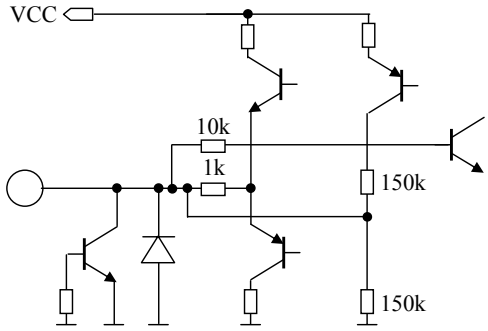
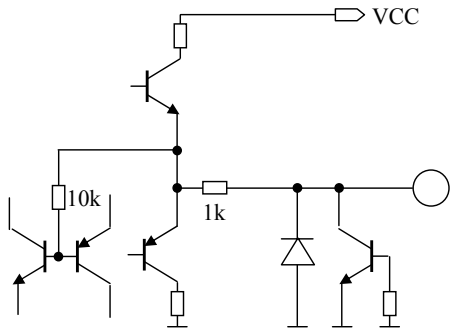
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
9	ROUT_NEG DC 1.45 V		R-ch. positive speaker output pin
10	GND_SPR	—	GND pin for R-ch. speaker output
11	ROUT_POS DC 1.45 V		R-ch. negative speaker output pin
12	VREF_SP DC 1.45 V		Reference voltage pin for output stage

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

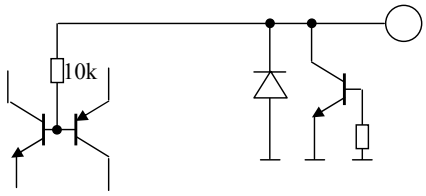
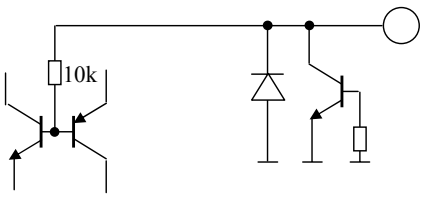
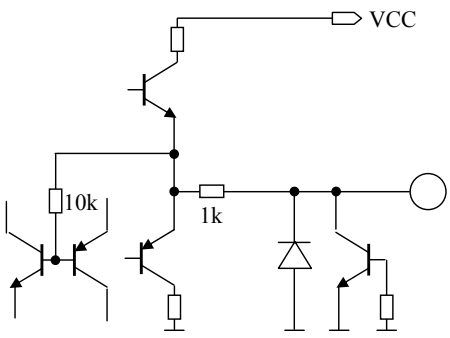
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
13	Test1 Hi-Z		Test mode pin Please connect to GND.
14	VCC 3.0 V(typ.)	—	Power supply pin
15	VREF DC 1.45 V		Reference voltage pin
16	PREOUT_R DC 1.45 V		First stage amplifier L-ch. output pin

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Description
17	FB_R DC 1.45 V		Negative feedback pin for input stage amplifier L-ch.
18	GND	—	Ground pin
19	FB_L DC 1.45 V		Negative feedback pin for input stage amplifier L-ch.
20	PREOUT_L DC 1.45 V		First stage amplifier L-ch. output pin

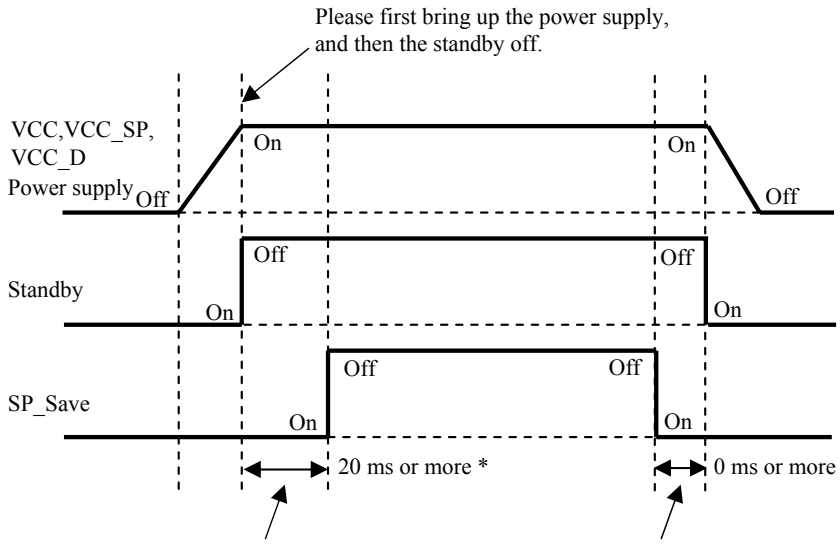
■ Technical Data (continued)

- Power supply and logic sequence

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1. The sequence of the power supply and each logic



The basic procedure at the power-on

1. The power OFF condition
   Both the standby and the SP_Save are in the ON condition.
2. Power ON
3. Standby Off
4. SP_Save Off

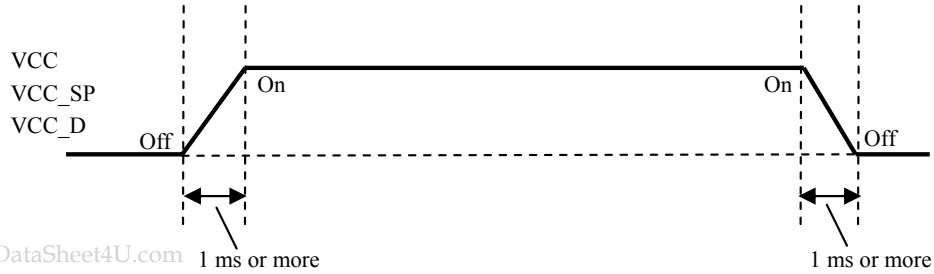
The basic procedure at the power-off

1. The power ON condition
   Both the standby and the SP_Save are in the OFF condition.
2. SP_Save On (= Standby On)
3. Standby On
4. Power Off

Note) *: This IC contains the pre-charge circuit. It is time until each bias is stabilized from Standby Off.
It depends for this time on the capacity value linked to a reference voltage terminal (VREF and VREFSP), and the capacity value and resistance linked to an input terminal (IN_R and IN_L).
It is a recommendation value in a constant given in the example of ■ Application Circuit Example (Block Diagram).

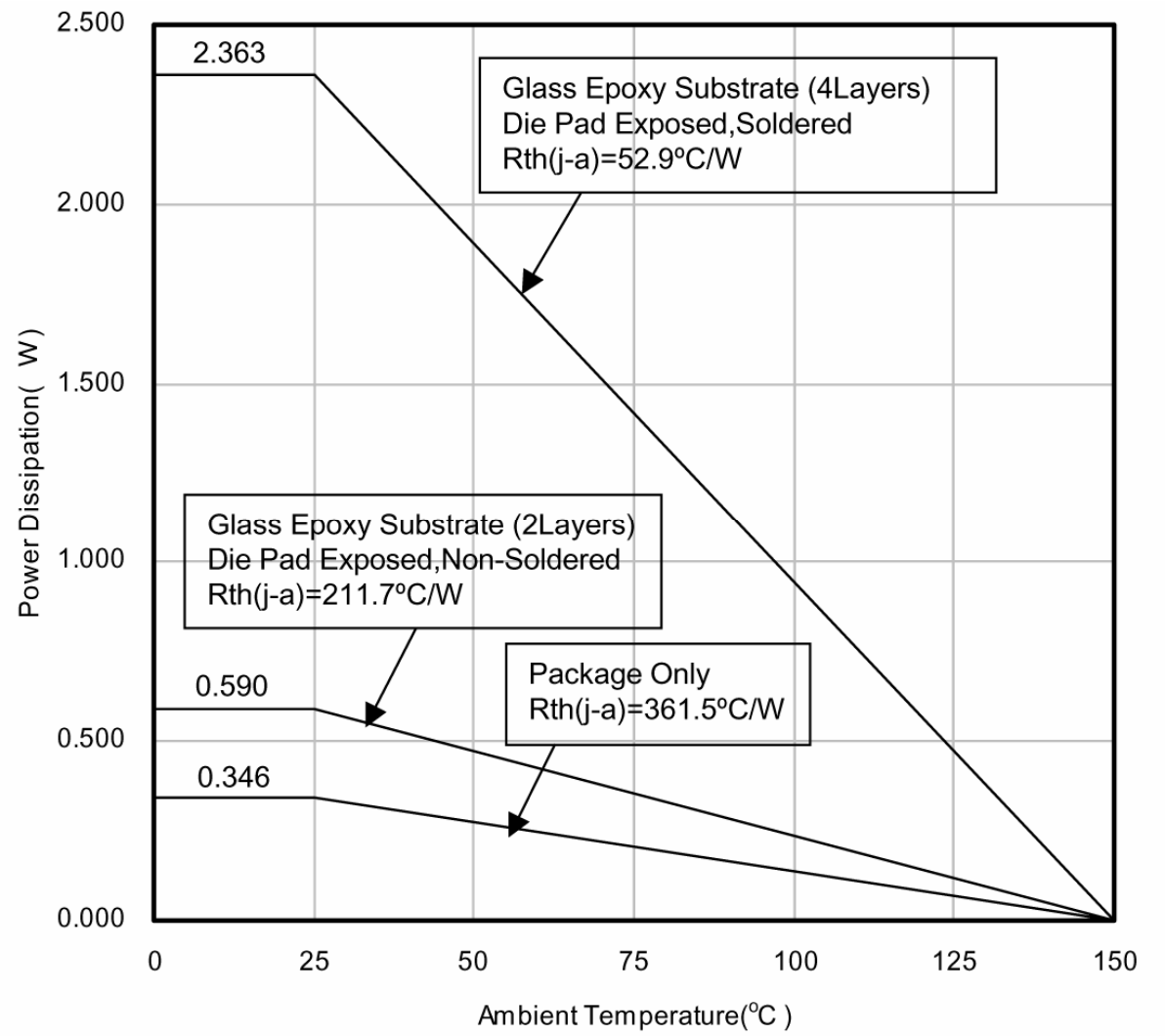
2. The sequence of VCC and VCC_SP and VCC_D

This IC have not a standup and falling order in VCC and VCC_SP.
A standup and falling time of VCC and VCC_SP recommend 1 or more ms.



■ Technical Data (continued)

• P_D — T_a diagram



■ Usage Notes

1. Please take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as SP output pin (Pin5, Pin7, Pin9, Pin11) – power supply pin short, SP output pin (Pin5, Pin7, Pin9, Pin11) – GND short, or SP output (Pin5, Pin7, Pin9, Pin11)-to-SP output-pin short (load short).

2. Please absolutely do not mount the IC in the reverse direction on to the printed-circuit-board.
   It damaged when the electricity is turned on.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

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