MOTOROLA
SEMICONDUCTOR APPLICATION NOTE

Order this document
by AN1577/D

AN1577

Motorola's D2 Series Transistors for Fluorescent Converters

Prepared by: Pascal M. OTERO
Application Engineer – MOTOROLA – Toulouse

INTRODUCTION

Switching bipolar transistors are very popular in the fluorescent ballast field where they provide cheap designs. Nevertheless the use of bipolar transistors is not straightforward: they are based on minority carrier operation making switching simulation difficult and inaccurate. Designing fluorescent converters with standard bipolar transistors requires a certain amount of skill.

The inductive storage time (tsi) variations and the optimization of fall time, so the switching losses and the case temperature are probably the most critical issues the designer has to deal with.

The aim of the D2 series is to drastically simplify the design of electronic ballasts for fluorescent tubes. This is possible due to the integration of two extra devices (D2): a freewheeling diode and an anti–saturation network.

This application note presents the interest of the D2 structure and how to utilize this new series to solve the critical issues that the designer must deal with.

Standard Bipolar Transistors Structure:

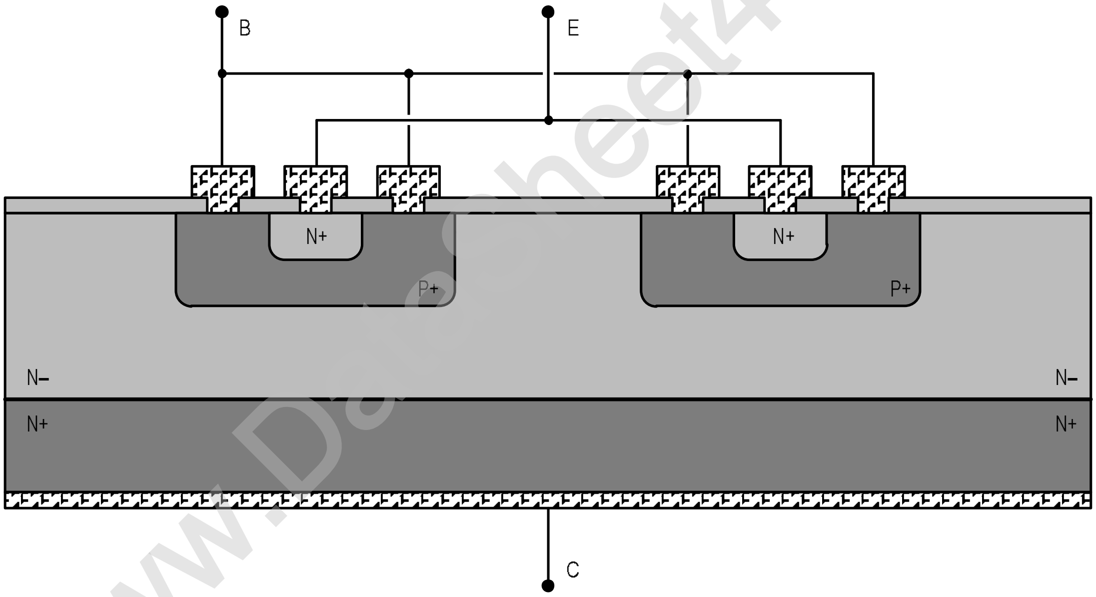


Figure 1. Standard Bipolar Transistor, Two Emitter Fingers Cross Section

During the saturation phase, the base and collector regions are filled with carriers that reduce significantly the resistivity of these areas.

This phenomenon has two consequences:

1. During turn off, the base resistance is either shorted to the emitter or connected to a negative voltage, so as the internal base voltage is still positive, the minority carriers are extracted from the base area (see Figures 18 and 19).

This phase takes time because the base resistivity depends on the carrier density of each part of the base area. The faster the carriers located near the base contact are extracted, the faster the resistivity increases near the base contact and the slower the carriers located under the emitter fingers will be extracted (Figure 2).

During this phase, the base current (named I_{B2}) is negative but V_{CE} is still V_{CEsat} and I_C is still flowing. This phase corresponds to the storage time (tsi).

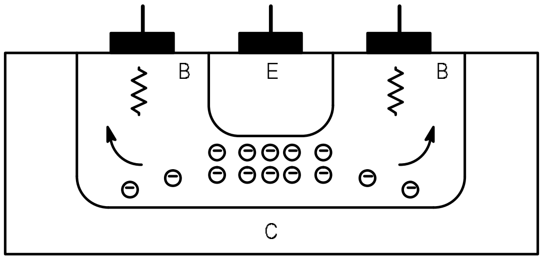


Figure 2. Poor Minority Carriers Extraction

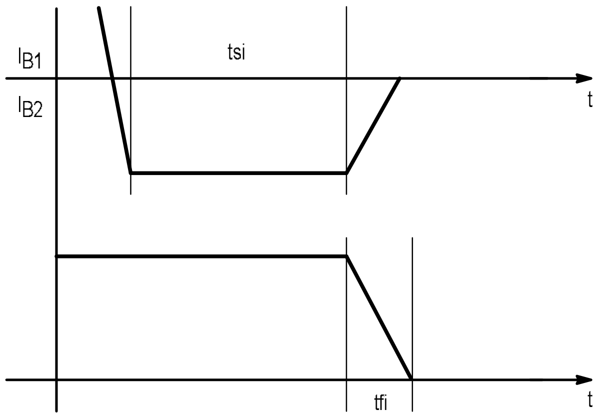


Figure 3. tsi and tfi Definition

When no charge remains trapped within the base, I_{B2} decreases to zero and I_C goes to zero as well: this is the fall time phase (See Figure 3 and Reference 3).

2. The drop of resistivity of the base and collector areas allows very low collector to emitter voltage, even if the current density is high (V_{CEsat}). See Figure 4.

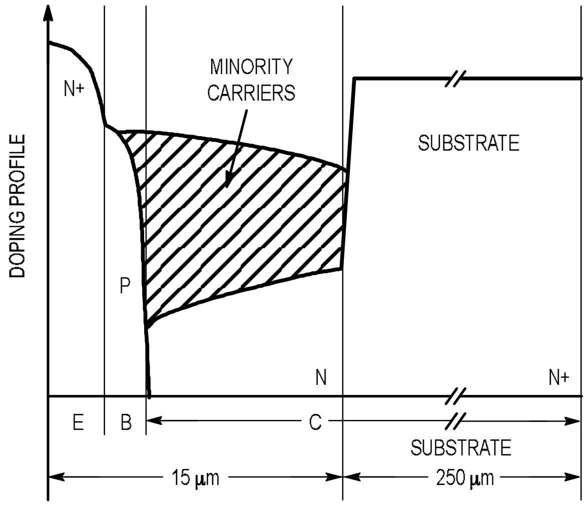


Figure 4. Minority Carriers Distribution During Saturation Condition

The low resistivity of the emitter, base and active collector areas, combined with their small depth, make the resistance of these areas very low compared to the substrate.

This modulation mechanism of the resistivity explains why bipolar on losses are smaller than those of MOSFET for a given die size.

D2 Series Structure:

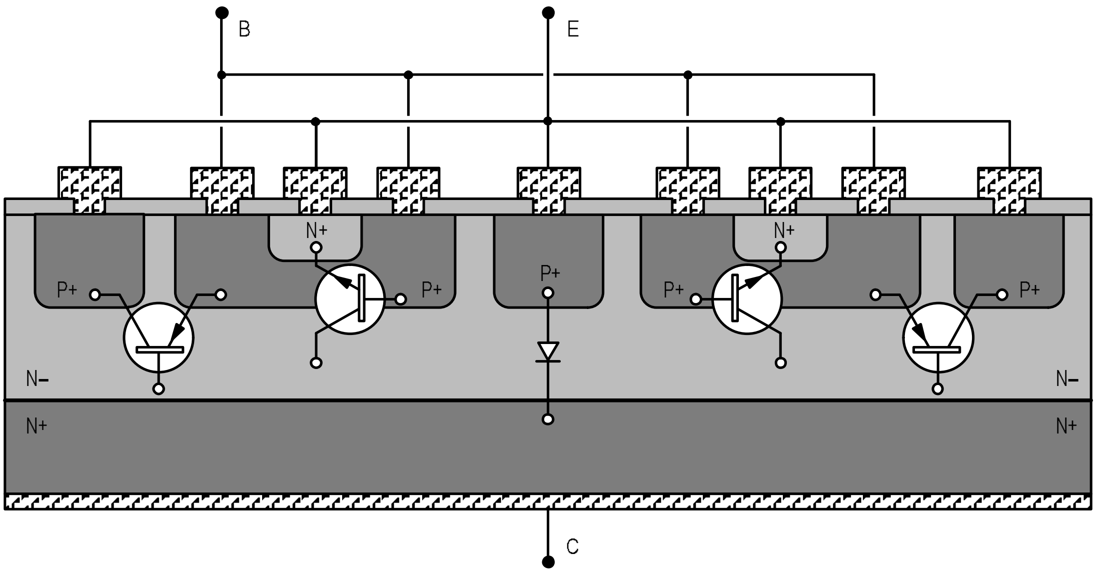


Figure 5. D2 Transistor Simplified Cross Section

Figure 5 shows the cross section of a D2 device. The main difference between D2 series and other transistors having built in freewheeling diode consists in the way the freewheeling diode is designed.

Instead of adding the diode in a corner of the die, the D2 devices have the diode, distributed across the active area of the transistor. This protected geometry gives an extra lateral PNP and unique advantages.

Freewheeling Diode:

An important point would be to measure the dynamic parameters of this diode. Unfortunately the measurement of the t_{rr} and Q_{rr} is impossible because it is not possible to isolate the distributed diode from the transistor structure.

However, we can compare I_C waveforms, coming from the application between BUL44 (standard switching transistor using external freewheeling diode), against BUL44D2.

Figure 6a shows the typical waveform of BUL44 collector current associated with 1N4937 and Figure 6b with MUR160, Figure 6c depicts BUL44D2 I_C curves. As we can see the distributed diode behavior is close by the MUR160 one from a t_{rr} point of view.

One must point out there is no advantage to connect an extra freewheeling diode across a D2 device. This external diode sets a different Q_{rr} than that of the internal one, and the PNP behavior is highly modified, implying an increase of power losses and heat dissipation within the switch.

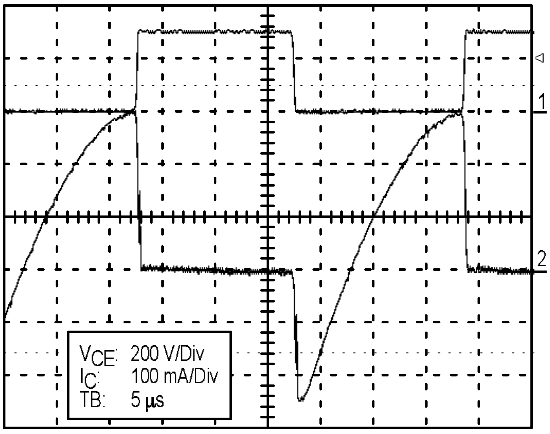


Figure 6a: BUL44 and 1N4937

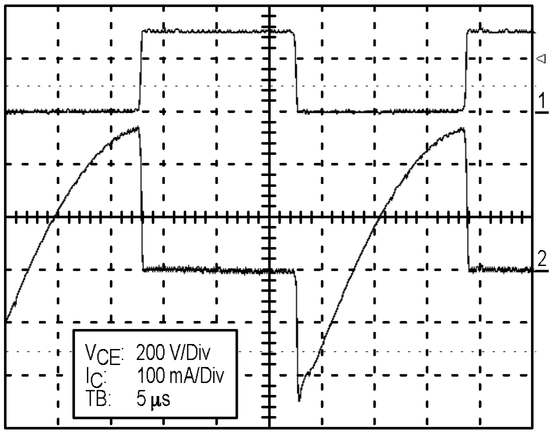


Figure 6b: BUL44 and MUR160

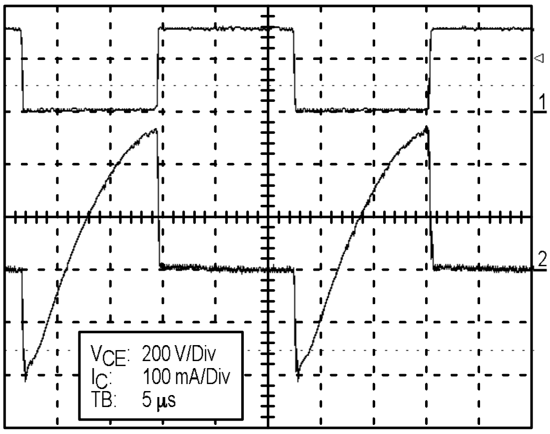


Figure 6c: BUL44D2

Anti–Saturation Network:

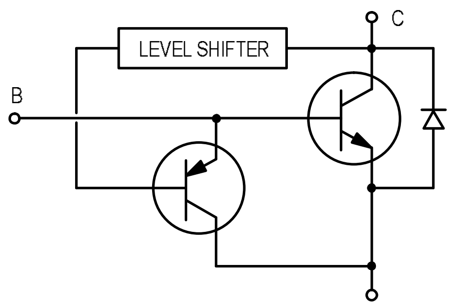


Figure 7. D2 Equivalent Schematic

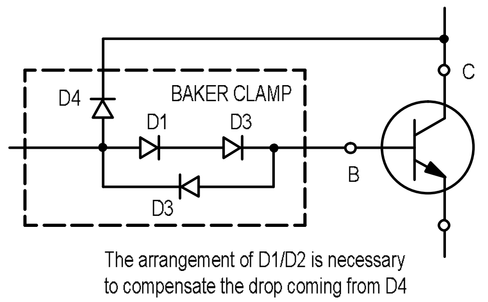


Figure 8. Baker Clamp Schematic

The anti–saturation network is built around the extra PNP connected as shown Figure 7. The effective I_B current of the main transistor is controlled by the feedback provided through the PNP and the V_{CEsat} sense of the NPN structure.

Like Baker clamp (Figure 8) this network allows either proportional drive or avoids hard saturation. The base current of the power transistor is limited when its V_{CE} voltage becomes too low. In case of a Baker clamp, the minimum V_{CE} is about two diode drops, as given by equation [1].

$$V_{CEsat} = V_{BE} + V_{D1} + V_{D2} - V_{D4} \quad [1]$$

The anti–saturation network built in of the D2 devices gives the same advantages as the Baker clamp, but without the drawback of a high V_{CEsat}. Figures 9a and 9b show two curves comparing dynamic V_{CEsat} observed in case of a BUL44D2 and the Baker clamp topology built around a BUL44 and 1N4937.

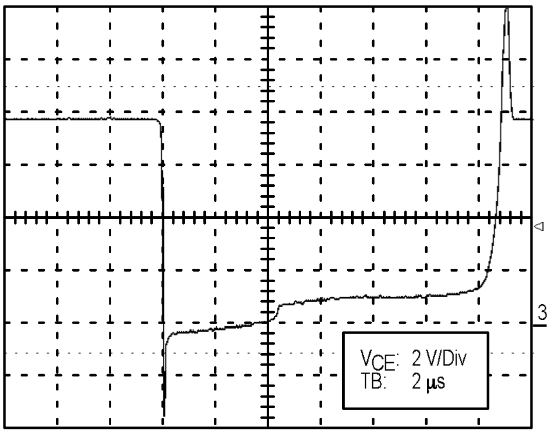


Figure 9a: BUL44D2 Dynamic V_{CEdyn}

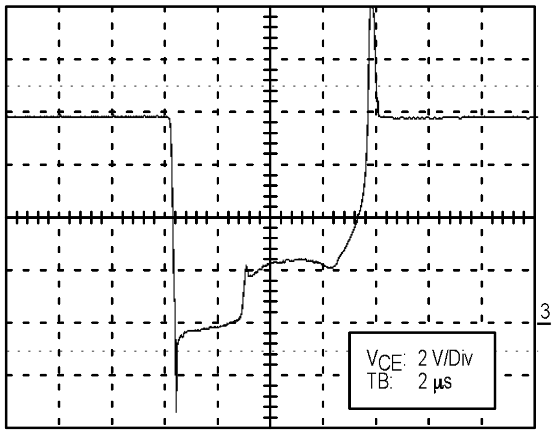


Figure 9b: BUL44/Baker Clamp V_{CEdyn}

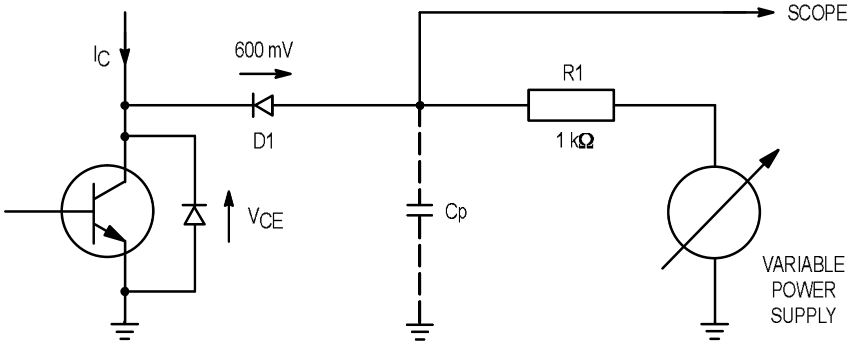
Note: Due to the test jig depicted in Figure 10, we must subtract from the observed values 600 mV (calibrated), coming from the diode drop.

This gives a net V_{CEsat} of 507 mV for BUL44D2, compared to 1.92 V for the Baker clamp topology.

Since R1 is small, this circuit has a small parasitic time constant R1Cp.

Critical Application Requirements:

The purpose of this paragraph is not to establish an exhaustive list of the switches technical requirements, but to point out the most critical ones (Refer to AN1543/D “Electronic Lamp Ballast”, where switches selection is described).



Since R1 is Small, this Schematic Allows a Small Parasitic Time Constant R1Cp.

Figure 10. Dynamic V_{CEsat} Test Jig

Inductive Storage Time (tsi) Dispersion:

The inductive storage time corresponds to the time required to extract the charges stored within the base, the collector load being inductive.

Since the tsi is a part of the converter half period, tsi variations can be pernicious to the life time of the tube. Due to the inductive load, frequency variations means power dissipation variations within the tube. Figure 11 shows the consequences of tsi variations on the power dissipated.

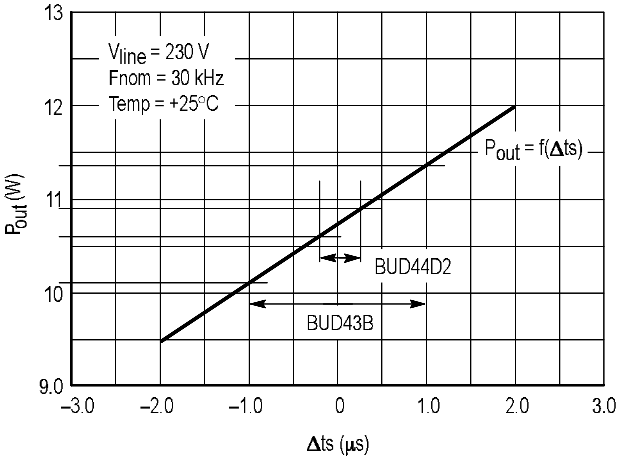


Figure 11. Ptube versus Δ (tsi)

We can observe the extremely tight tsi dispersion of D2 devices compared to standard ones. The specification guaranties the tsi dispersion at ±150 ns (whatever be the temperature within the specified range), and the output power follows the same dispersion.

Figure 12 shows the t_{off} variation of the BUL45D2 versus the temperature between –40°C and +125°C. Leaving aside the tolerances coming from the measurements, the t_{off} variation follows a straight line and, due to the tight dispersion of this parameter, is absolutely predictable.

Manufacturing standard fluorescent converters using bipolar transistors requires to guaranty an h_{FE} window to correlate a tsi window.

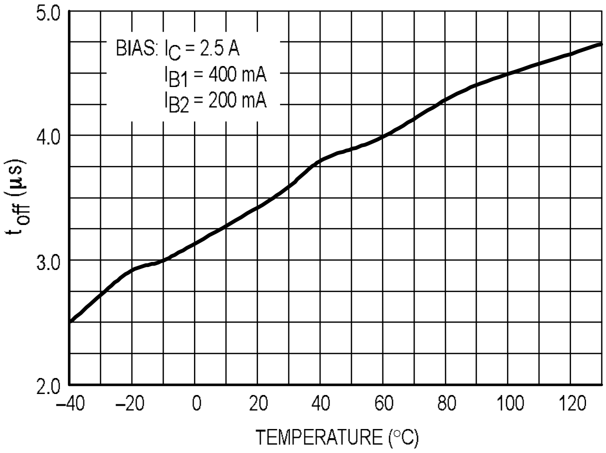


Figure 12. BUL45D2 t_{off} Variation versus Temperature

In case of D2 devices h_{FE} windows does not make sense anymore. Since the power transistor and the PNP one are diffused on the same die, h_{FE} variations are equivalent for both transistors. So PNP h_{FE} variation tends to compensate the NPN one, making tsi nearly constant when h_{FE} varies.

Fall Time and Power Losses:

Power losses are an important criterium since they are responsible of the operating case temperature which can be approximated using equation [2]:

$$T_C - T_a = P_1 \times Rth_{JA}. \qquad [2]$$

Where T_C: Case temperature

T_a: Ambient temperature

P_1: Power losses within the switch

Rth_{JA}: Thermal resistance between Junction to Ambient.

(Assuming $Rth_{JA} >> Rth_{JC}$).

Since the junction temperature is limited for reliability reasons at 150°C max, the lower the losses, the higher can be the ambient temperature.

Following the usual analysis, power losses can be split in four different parts corresponding to the four phases of a switching sequence (Figure 13).

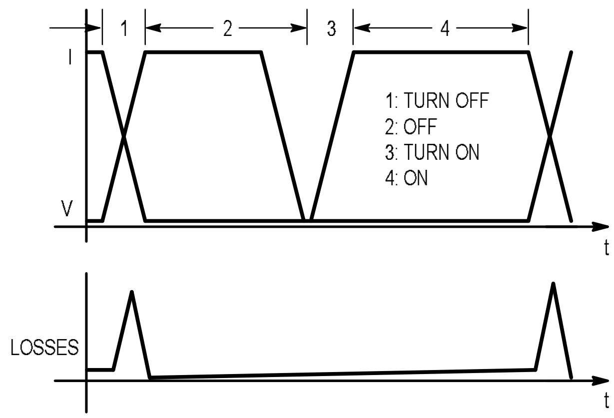


Figure 13. Switching Sequence

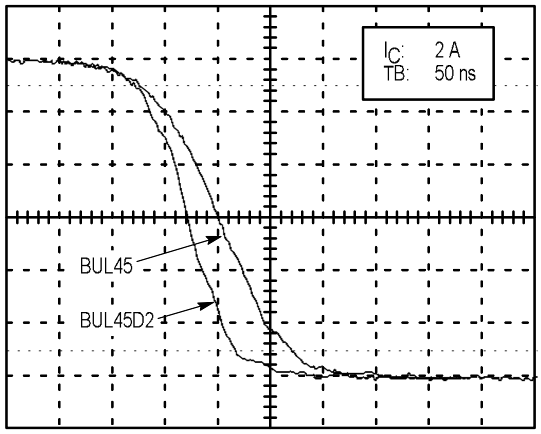


Figure 14. BUL45D2 tfi: 95 ns, BUL45 tfi: 150 ns

1– Turn off losses:
The minority carriers trapped into the base and the collector areas, during the on phase are responsible of fall time. This produces losses only during switch off as the dV_{CE}/dt is high due to inductive switching. Figure 14 shows BUL45D2 and BUL45 tfi under the same bias condition.
2– Off losses are negligible due to the low value of the leakage current.
3– Turn on losses are negligible as well because V_{CE} drops to V_{CEsat} before I_C increases.
4– On losses:
They are characterized by the product: $V_{CEsat} \times I_C$.

During the saturation phase, the base and the collector areas are filled with minority carriers. This reduces the resistivity of the silicon and provide low losses (Figure 4).

Due to the D2 design, the power dissipated within the switch is no longer related to the switching phase, but comes from the on phase (1).

This is extremely important from a design safety point of view:

During turn off phase, the transistor is reverse biased (I_B is negative, V_{CE} and I_C positive) and has to sustain a moving I_C/V_{CE} operating point. The switch can be destroyed in few micro seconds if this point goes out of the Reverse Bias Safe Operating Area as shown Figure 15. (See AN873/D and AN875/D).

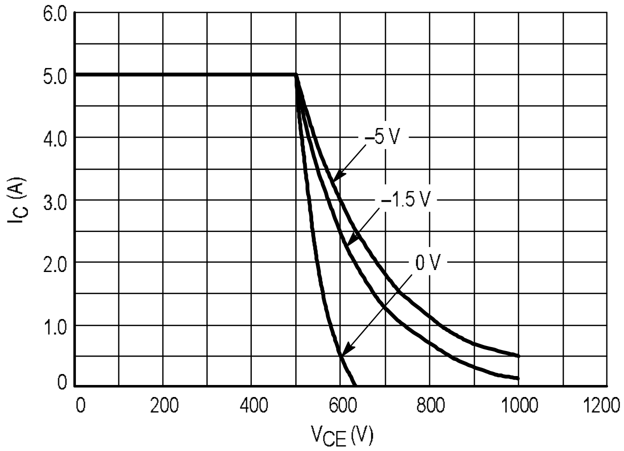


Figure 15. Typical RBSOA Curve versus Different Reverse Bias Voltages Applied on the Base

Power losses produced during the on phase are much more safer because they follow thermal laws.

D2 in Fluorescent Application:

Another important advantage of this network consists in the drastic simplification of the calculation of the drive and so the development time of the designer.

Usually designers have to adapt the oscillation transformer output to the transistor.

The base drive conditions set up the behavior of the transistor as follows:

I_{B1} peak must be high enough to guaranty low V_{CEsat}
I_{B1} negative going slope must be optimized to adjust the tsi and the frequency
I_{B2} shall be adjusted to minimize turn off losses

We must point out it is difficult to achieve the accurate control of the negative going slope of the base current in a cheap way.

The use of D2 device is much more simpler as it is less sensible to the I_{B1} to I_{B2} transition, accommodates sharp edges and high I_{B2} level.

The same principle allows proportional drive:

One of the interest of the Baker clamp is the proportional drive that consists in the possibility to drive either one or two tubes or more, keeping the bias network of the transistor constant.

By connecting several tubes to a single converter, the I_C current varies proportionally to the number of tubes. This means I_B current must be able to follow this variation according to the transistor transfer curve.

This is not possible due to the non linear response of the saturable core of the oscillation transformer.

The use of D2 devices is a way to overcome this non linearity.

(1) It is important to notice this new way to manage the power dissipated within the bipolar transistor allows operating frequencies up to 100 kHz.

How to Get Best Benefits Out of the D2 Series:

We demonstrated the D2 series works fine within a wide range of biases. Most of the time designers need transistors operating at high ambient temperature. (i.e. due to the housing, compact fluorescent ambient temperature can reach 125°C, the transistors must operate safely. The thermal constraint is more sensitive for DPAK packaged devices).

Generally speaking the problem consists in pushing further the thermal runaway occurrence.

A possible cause of a thermal runaway is a pre–switching off desaturation (V_{CE} begins to increase at the end of the tsi phase, as I_C is maximum, before switch off). This phenomenon can occur, mainly with the D2 series because of its specific structure. The operating principle of these devices is to never run in hard saturation (Figure 7), this means the among of charges trapped within the base is small.

So, as soon as I_{B2} extracts a certain amount of charge, V_{CE} tends to increase: the device is desaturated.

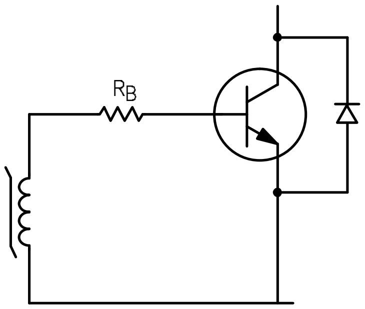


Figure 16.

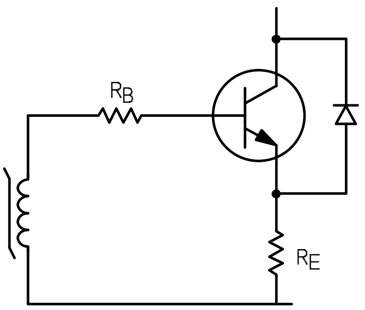


Figure 17.

Based on the cheapest and the most common drive circuits shown Figures 16 and 17, the analysis of this specific bipolar transistor operation gives two ways to stabilize the device at high operating temperature, when the I_C current tends to runaway:

– Increase the emitter resistance value (Re).

As the collector current is high, the drop voltage across the emitter resistance provides a negative feed–back to the base of the D2 device.

So, during I_{B1} phases, the net voltage available across the base circuit (out of the secondary of the toroid) is reduced by the feedback voltage.

During I_{B2} phases, the oscillator transformer does not provide any driving voltage anymore and the secondary winding shorts the base resistance to the ground. As I_C value is still high, the emitter voltage is positive (Figure 19).

This increases I_{B2} (as if a negative voltage were applied across the base), limits any pre–switching off desaturation and improve significantly the thermal behavior of the device.

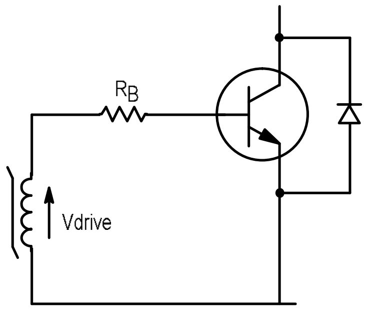


Figure 18.

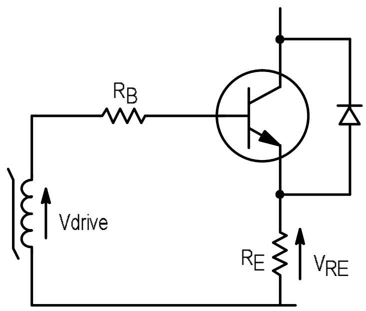


Figure 19.

– Increase IB1 value.

The value of I_{B1} current can be very different without having significant impact on switching parameters, due to the anti–saturation network.

The h_{FE} of the built in PNP, like other bipolar transistors, is limited by the level of I_C current (see typical h_{FE} versus I_C curves). So the extra base current derived via the PNP is limited as well. When I_{B1} is higher than that the PNP can handle, its h_{FE} drops and the anti–saturation network does not work anymore. So the amount of charges trapped within the power NPN transistor base can be larger and the pre–switching desaturation phenomenon disappears.

Both solutions generally imply an adjustment of the toroid turns ratio to adjust the operating frequency.

Designers that are used to driving standard bipolar transistors know that the negative slope of I_{B1} and the value of I_{B2} are critical to optimize ts, tf and hence the switching losses.

Using a D2 device is simple: ts, tf and switching losses will be optimized as soon as I_{B2} value is high (this value can be higher than that of I_{B1}) and I_{B2} waveform is as square as possible (fast falling edge).

CONCLUSION

Standard bipolar transistors are attractive in the lamp ballast field because of their price and performances, nevertheless designing bipolar transistors requires a certain skill, mainly due to tsi variation from lot to lot.

The new D2 family combines cost advantage and simplifies the design.

The coming of the D2 series allows the saving of PCB space because the freewheeling diode is built in and some drive components can be removed. Due to the specific way the diode is laid out, an anti–saturation network is integrated, providing significant advantages such as extremely tight tsi distribution (typically: ±80 ns), inexpensive designs, high operating speed (up to 100 kHz, under accurate biases conditions), lower power dissipation and proportional drive enabling variable load.

The D2 family of application specific transistors enables the design of bipolar based fluorescent converters. They are not only cost effective but simple and straightforward as well.

SELECTOR GUIDE

DEVICE TYPE	V_{CEO}	V_{CES}	I_{Cmax}	PACKAGE
BUD44D2	400 V	700 V	2 A	DPAK
MJD18002D2	450 V	1000 V	2 A	DPAK
BUL44D2	400 V	700 V	2 A	TO220
BUL45D2	400 V	700 V	5 A	TO220
MJE18002D2	450 V	1000 V	2 A	TO220
MJE18004D2	450 V	1000 V	5 A	TO220
MJE18604D2	800 V	1600 V	2 A	TO220

References:

1. MOTOROLA, AN873: Understanding Power Transistor Dynamic Behavior.
2. MOTOROLA, AN875: Power Transistor Safe Operating Area.
3. MOTOROLA, AN1543: Electronic Lamp Ballast Design.

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848
INTERNET: http://www.mot.com/SPS/

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298