DATA SHEET

Part No.	AN15887A
Package Code No.	QFP048-P-1212C

Contents

AN15887A

Audio video SW for TV with multi-signal input output

■ Overview

AN15887A has video switch portion which consists of :

- 6 inputs for composite video
- 2 Video output driver with sag compensation

AN15887A has audio switch portion which consists of :

- 5 inputs for left and right channels
- 2 outputs for left and right channels

It contributes to the rationalization design of a TV system.

■ Features

- Output frequency can be switched between LPF (6.75 MHz) and through
- Wide bandwidth video frequency −3 dB at 25 MHz in through mode
- 6.0 dB gain for video signal
- Selectable output driver for 75 Ω/10 kΩ load
- Selectable isolator function for different audio/Video input channels
- 0 dB/−6 dB audio gain switch for audio OUT
- Various input mode (audio and video) can be selected by using flexible internal switch
- Supports I^2C bus

■ Applications

- TV, car navigation

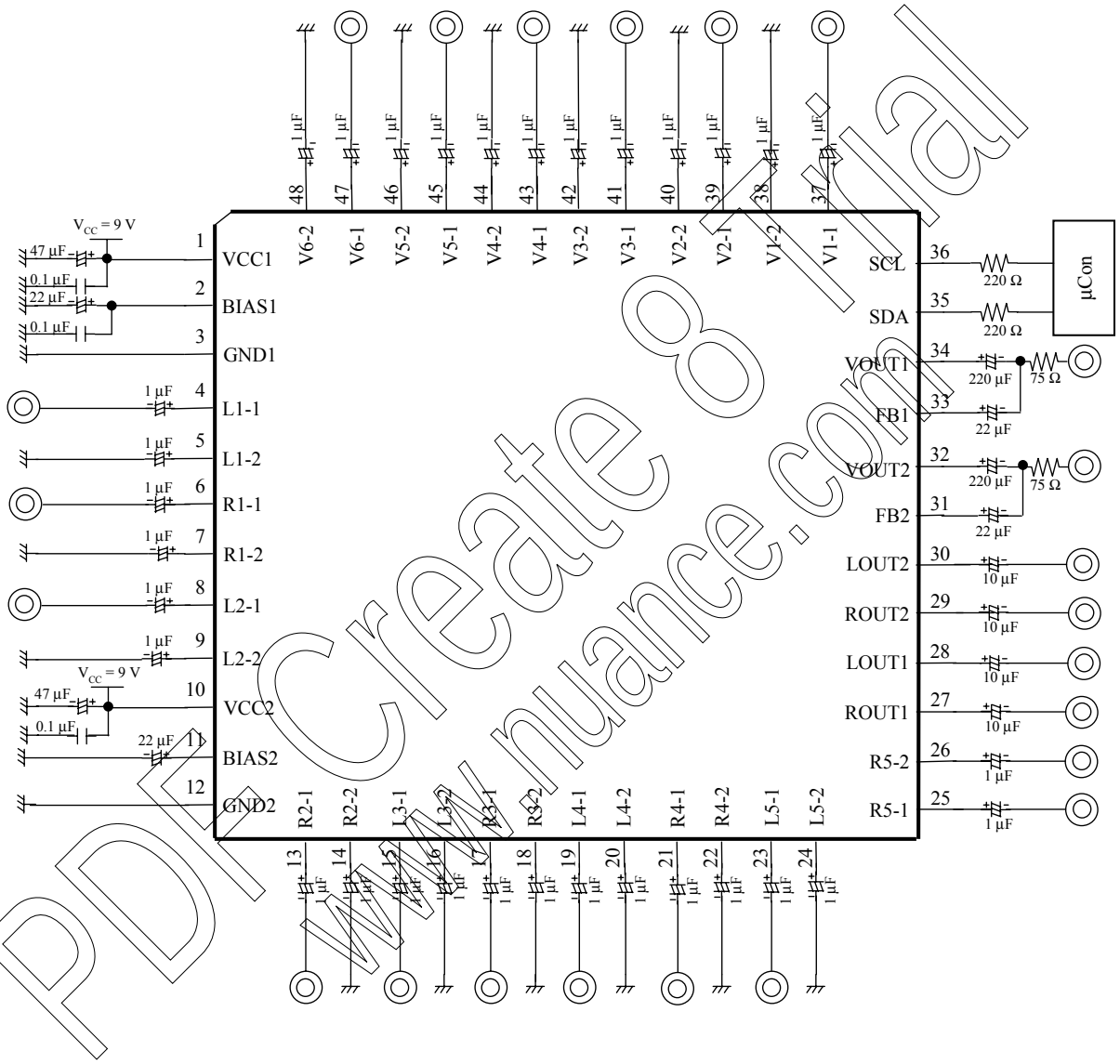
■ Package

- 48 pin plastic quad flat package (QFP type)

■ Type

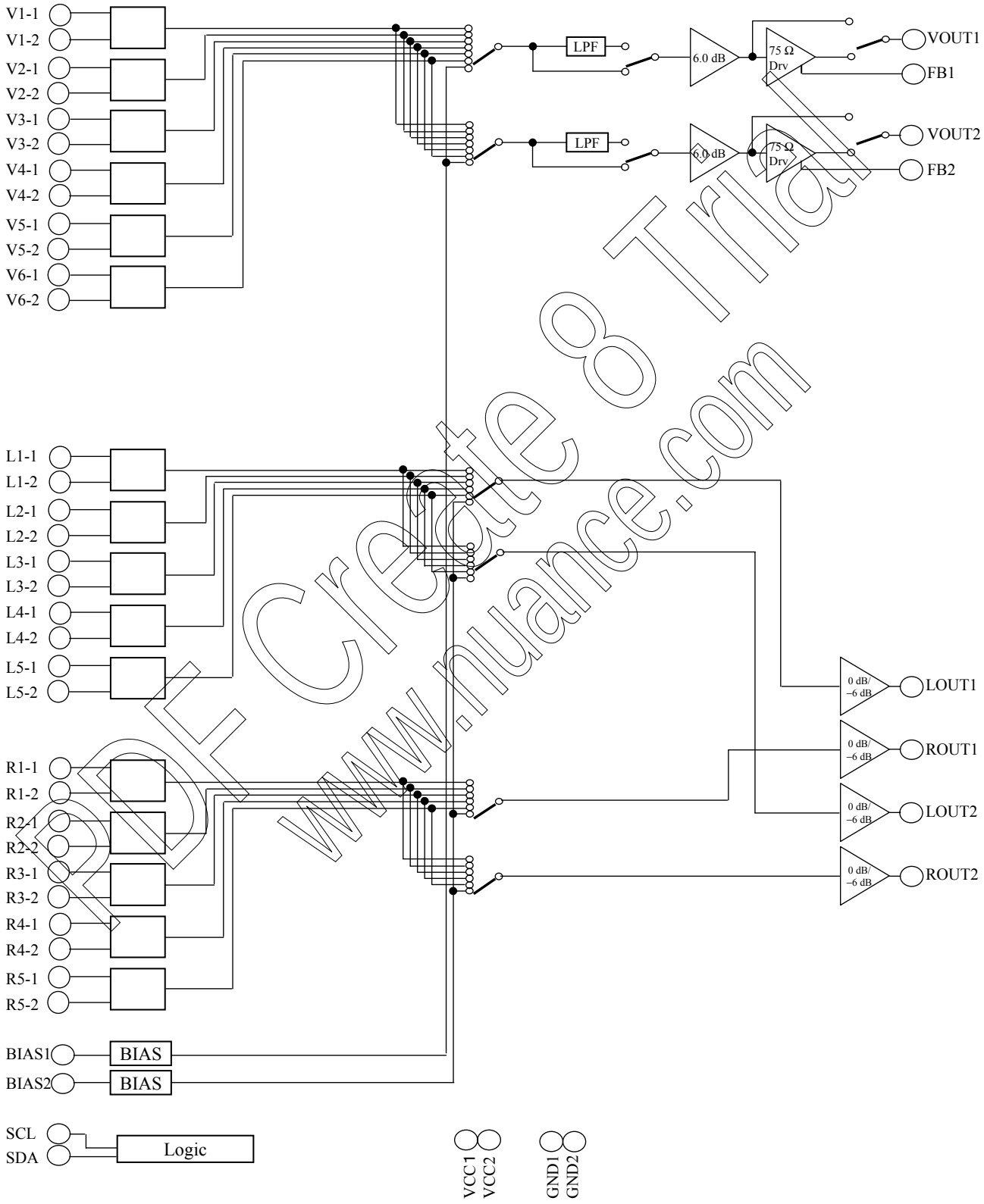
- Bi-CMOS IC

■ Application Circuit Example



Note) This application circuit is shown as an example but does not guarantee the design for mass production set.

■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin Name	Type	Description
1	VCC1	Power supply	9.0 V video power supply
2	BIAS1	Output	Video bias voltage 1
3	GND1	Ground	Video ground 1
4	L1-1	Input	Left audio signal input 1-1
5	L1-2	Input	Left audio signal input 1-2
6	R1-1	Input	Right audio signal input 1-1
7	R1-2	Input	Right audio signal input 1-2
8	L2-1	Input	Left audio signal input 2-1
9	L2-2	Input	Left audio signal input 2-2
10	VCC2	Power supply	9.0 V audio power supply
11	BIAS2	Output	Audio bias voltage 2
12	GND2	Ground	Audio ground 2
13	R2-1	Input	Right audio signal input 2-1
14	R2-2	Input	Right audio signal input 2-2
15	L3-1	Input	Left audio signal input 3-1
16	L3-2	Input	Left audio signal input 3-2
17	R3-1	Input	Right audio signal input 3-1
18	R3-2	Input	Right audio signal input 3-2
19	L4-1	Input	Left audio signal input 4-1
20	L4-2	Input	Left audio signal input 4-2
21	R4-1	Input	Right audio signal input 4-1
22	R4-2	Input	Right audio signal input 4-2
23	L5-1	Input	Left audio signal input 5-1
24	L5-2	Input	Left audio signal input 5-2
25	R5-1	Input	Right audio signal input 5-1
26	R5-2	Input	Right audio signal input 5-2
27	ROUT1	Output	Right audio signal output 1
28	LOUT1	Output	Left audio signal output 1
29	ROUT2	Output	Right audio signal output 2
30	LOUT2	Output	Left audio signal output 2
31	FB2	Input	VOUT2 signal sag correction input
32	VOUT2	Output	VOUT2 signal output
33	FB1	Input	VOUT1 signal sag correction input
34	VOUT1	Output	VOUT1 signal output
35	SDA	Input/Output	I^2C bus data input/output

■ Pin Descriptions (continued)

Pin No.	Pin Name	Type	Description
36	SCL	Input	I^2C bus clock input
37	V1-1	Input	Video composite signal input 1-1
38	V1-2	Input	Video composite signal input 1-2
39	V2-1	Input	Video composite signal input 2-1
40	V2-2	Input	Video composite signal input 2-2
41	V3-1	Input	Video composite signal input 3-1
42	V3-2	Input	Video composite signal input 3-2
43	V4-1	Input	Video composite signal input 4-1
44	V4-2	Input	Video composite signal input 4-2
45	V5-1	Input	Video composite signal input 5-1
46	V5-2	Input	Video composite signal input 5-2
47	V6-1	Input	Video composite signal input 6-1
48	V6-2	Input	Video composite signal input 6-2

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	V_{CC}	12.0	V	*1
2	Supply current	I_{CC}	—	A	—
3	Input voltage	V1	—	V	—
4	Power dissipation	P_D	340	mW	*2
5	Operating ambient temperature	T_{opr}	–40 to +85	°C	*3
6	Storage temperature	T_{stg}	–55 to +125	°C	*3

Note) *1: The range under absolute maximum ratings, power dissipation.

*2: Power dissipation shows the value of only package at T_a = 85°C.
When using this IC, refer to the 6. $P_D - T_a$ diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*3: Expect for the storage temperature and operating ambient temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	V_{CC}	7.5 to 9.5	V	—

Note) The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Electrical Characteristics at V_{CC} = 9 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
1	Quiescent current	I_{CQ}	No signal input, no load	43	50	57	mA	—
2	Voltage gain OUT	A_0	Gain setting = 0 dB 2.0 V[p-p] input at 1 kHz	–0.4	0	0.4	dB	—
		A_6	Gain setting = –6 dB 2.0 V[p-p] input at 1 kHz	–6.4	–6.0	–5.6	dB	—
3	Frequency response	f_{AI}	2.0 V[p-p] input at 50 kHz/1 kHz	–1.0	0	1.0	dB	*
4	Total harmonic distortion	THD_0	Gain setting = 0 dB 2.0 V[p-p] input at 1 kHz 400 Hz HPF + 80 kHz LPF	—	0.01	0.03	%	—
5	Residual noise	V_{NR0}	Gain setting = 0 dB All input pins grounded through Rg = 600 Ω (A-weighted noise filter)	—	8	15	μV[rms]	—
6	Source crosstalk	CT_A	2.0 V[p-p] input at 1 kHz (Din audio)	—	—	–75	dB	—
7	Channel crosstalk	CT_{LR}		—	—	–75	dB	—
8	Ripple rejection	A_{PSRR}	Apply 0.3 V[p-p] at 100 Hz to V_{CC}. All input pins grounded through capacitors (22 μF at bias pin) set at 0 dB	—	—	–45	dB	—
9	Input dynamic range	D_{IA5}	Gain setting = –6 dB f = 1 kHz input, THD < 0.5%	2.8	—	—	V[rms]	—
10	Video gain	G_V	f = 100 kHz, Vin = 1 V[p-p]	5.6	6.0	6.4	dB	—
11	Video frequency response	f_V	Input frequency where output amplitude is –3 dB (6.75 LPF OFF)	25	—	—	MHz	—
12	LPF characteristic 6.75 MHz (1)	f_{LPF11}	1.0 V[p-p] input at 6.75 MHz/500 kHz (6.75 LPF ON)	–1.5	0.0	1.5	dB	—
13	LPF characteristic 6.75 MHz (2)	f_{LPF12}	1.0 V[p-p] input at 27 MHz/500 kHz (6.75 LPF ON)	—	–33.0	–24.0	dB	—
14	Crosstalk	CT_V	1.0 V[p-p] input at 3.58 MHz	—	–55	–50	dB	—
15	Output DC level	dVD_O	Measure the difference from the output DC level while in mute mode	–0.4	—	0.4	V	—
16	Input dynamic range	V_{DR-V}	—	2.0	2.1	—	V[p-p]	—

Note) *: Audio frequency response is not guaranteed when external resistors components are used.

■ Electrical Characteristics at V_{CC} = 9 V (continued)

Note) T_a = 25°C±2°C unless otherwise specified.

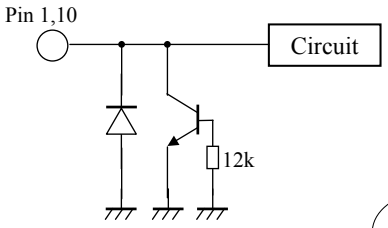
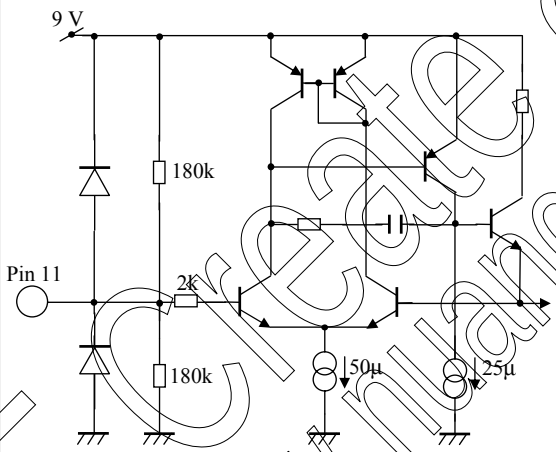
B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C Interface								
17	Suction current during ACK	I_{ACK}	Max. suction current value of SDA at 0.4 V	3.0	6.0	—	mA	*
18	SCL, SDA signal input high level	V_{IHI}	—	2.7	—	5.2		
19	SCL, SDA signal input low level	V_{ILO}	—	0	—	1.5		
20	Max. frequency allowable to input	f_{imax}	—	—	—	400		
21	Hysteresis of schmitt trigger inputs	V_{hys}	—	0.15	—	—		
22	Pulse width of spikes which must be suppressed by the input filter	t_{sp}	—	0	—	50		
23	Input current each I/O pin with an input voltage between 0.3 V and 2.7 V	Ii	—	−10	—	10		
24	Capacitance for each I/O pin	Ci	—	—	—	10		
25	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$T_{HD;STA}$	—	0.6	—	—		
26	Low period of the SCL clock	t_{LOW}	—	1.3	—	—		
27	High period of the SCL clock	t_{HIGH}	—	0.6	—	—	V	*
28	Set-up time for a repeated START condition	t	—	0.6	—	—	V	*
29	Data hold time; For I²C-bus devices	$t_{HD;DAT}$	—	0	—	0.9	Kbit/s	*
30	Data setup time	$t_{SU;DAT}$	—	100	—	—	V	*
31	Rise time of both SDA and SCL signals	t_r	—	—	—	300	ns	*
32	Fall time of both SDA and SCL signals	t_f	—	—	—	300	µA	*
33	Set-up time for STOP condition	$t_{SU;STO}$	—	0.6	—	—	pF	*
34	Bus free time between a STOP and start condition	t_{BUS}	—	1.3	—	—	µs	*
35	Capacitive load for each bus lines	Cb	—	—	—	400	µs	*

Note) *: All values referred to V_{IHmin} and V_{ILmax} levels.
Design software so that I²C communication should not freeze even if an I²C bit error occurs due to factors such as external noise.

■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

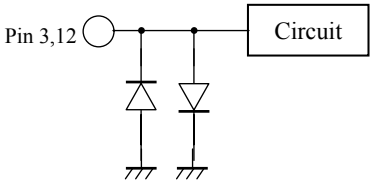
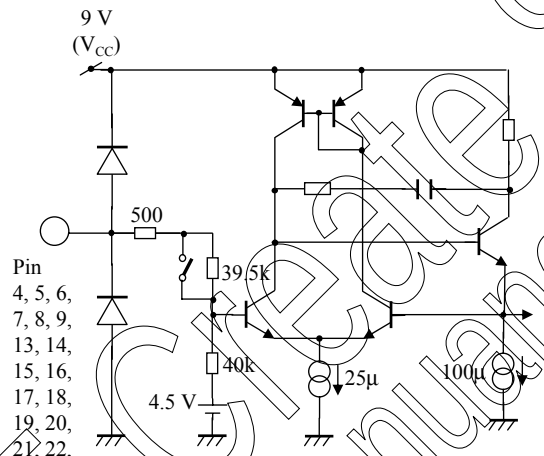
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1 10	9 V		—	9 V system power supply pins
11	4.5 V		90 kΩ	Reference bias pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

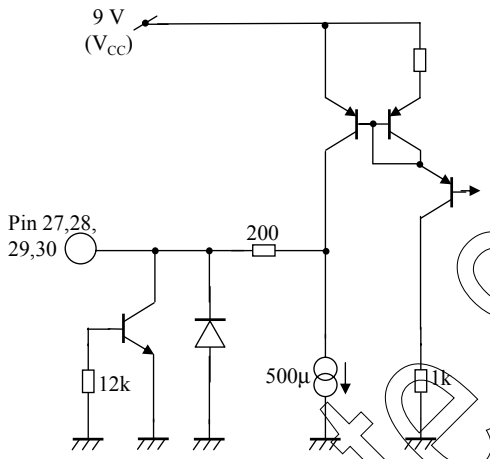
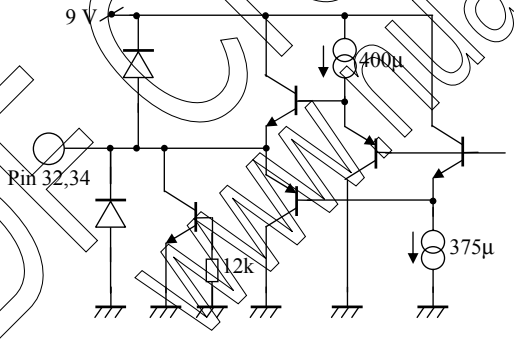
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
3 12	0 V			System ground pins
4 5 6 7 8 9 13 14 15 16 17 18 19 20 21 22 23 24 25 26	4.5 V		80 kΩ/41 kΩ	• Audio signal input pins • If audio signal input pin is not used, connect it with a capacitor to GND • L: Left channel • R: Right channel

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

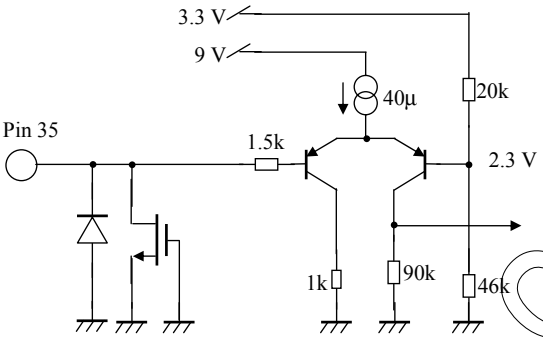
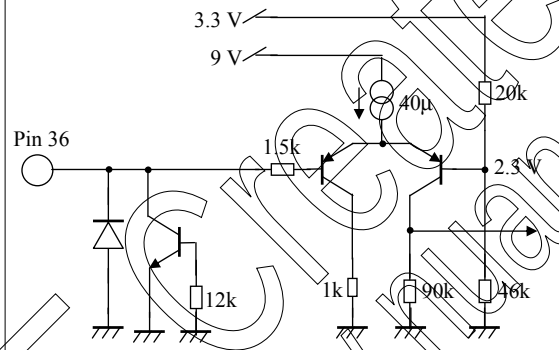
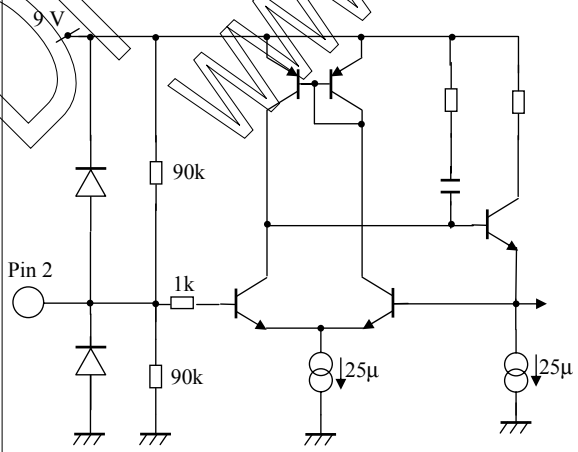
Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
27 28 29 30	4.5 V		E.F. *	Audio signal Output pins
32 34	3.7 V		E.F. *	Video composite, luminance, chrominance signal outputs.

Note) *: E.F. means emitter follower (low impedance).

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

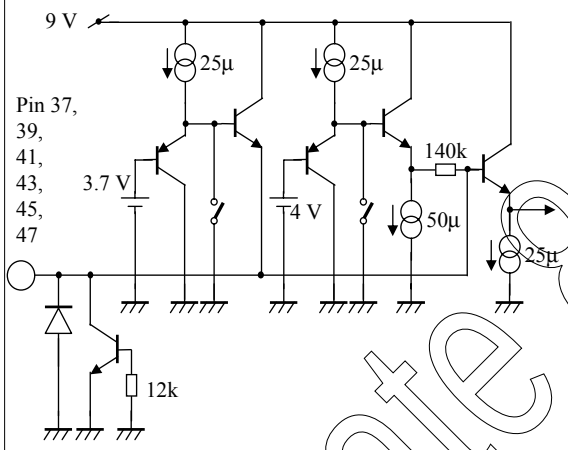
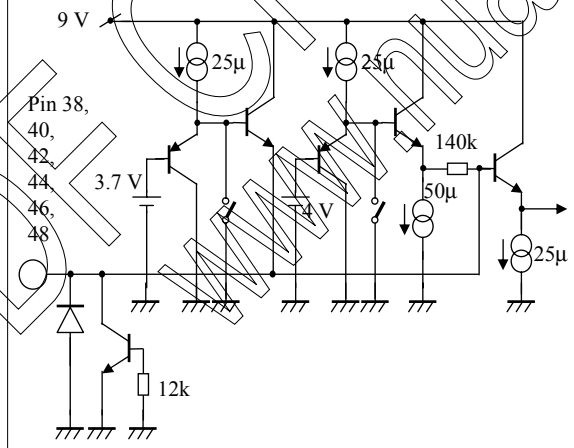
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
35	—		—	I^2C bus data input pin.
36	—		—	I^2C bus clock input pin.
2	4.5 V		45 kΩ	Reference bias pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
37 39 41 43 45 47	3.7 V		E.F. *	Video composite signal inputs
38 40 42 44 46 48	3.7 V		E.F. *	Video composite signal inputs

Note) *: E.F. means emitter follower (low impedance).

■Technical Data (continued)

2. I²C bus

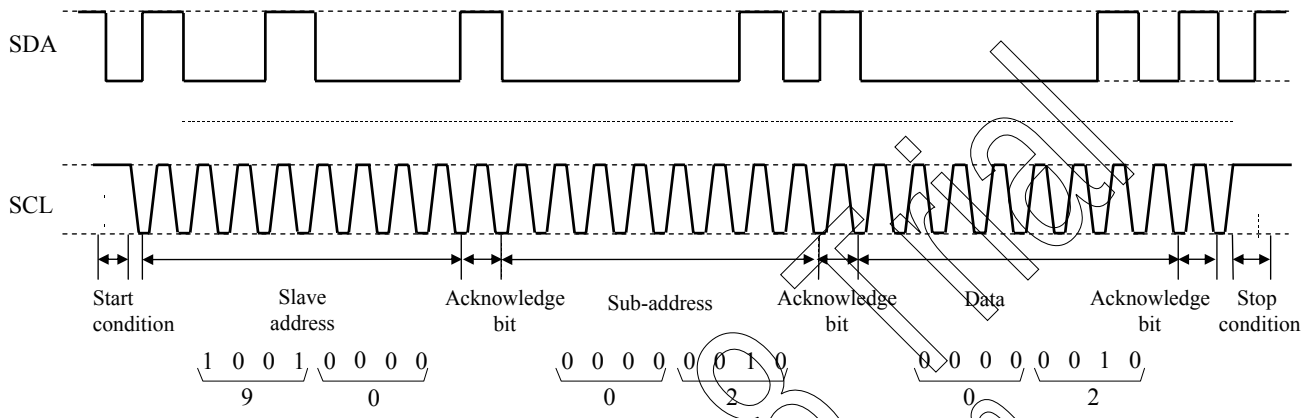


Fig. 1. Example of transmission message

For transmission messages, both SCL and SDA are transferred in the form of synchronized serial transmission. SCL is a clock of a specific frequency, and SDA indicates address data for controlling the receiving side and is transferred in parallel, being synchronized with SCL. Data is transferred in principle in 3 octets (bytes), and each one octet (one octet = 8 bits) includes one acknowledge bit. Frame structure is described below.

(a) Start condition — The receiver becomes possible to receive data when SDA changes from High to Low while SCL is High.

(b) Stop condition — The receiver halts receiving when SDA changes from Low to High while SCL is High.

(c) Slave address — This is an address which is determined for each device. If other device address is sent, receiving will be halted.

(d) Sub-address — This is an address which is determined for each function.

(e) Data — This is control data.

(f) Acknowledge bit — This is a bit by which the master acknowledges that data was successfully received in each octet. Master sends the High signal and the receiver sends back the Low signal as shown in Figure 1 with dotted line, causing the master to acknowledge the reception by the receiver. If the Low signal is not returned, communication will be halted.

Except start and stop conditions, SDA does not change while SCL is High.

■ Technical Data (continued)

2. I²C bus (continued)

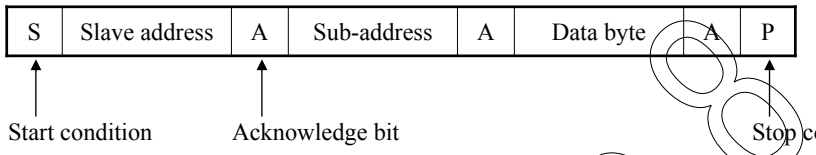
1) This contains 6 registers

2) Auto-increment function present:

- Sub-address 0*******: Auto-increment mode
  (When the data is sent in consecutive order, the Sub-address will be changed in consecutive order, as data is input)
- Sub-address 1*******: Data update mode
  (When the data is sent consecutively, it is sent to the same sub-address)

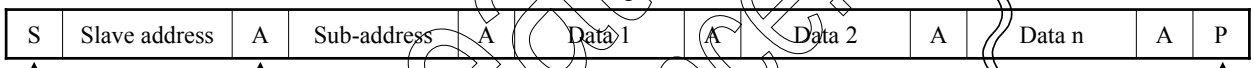
3) I²C bus protocol

- Slave address: 10010000 (90H)
- Format (usual)



Start condition Acknowledge bit Stop condition

- Auto-increment mode / data update mode



Start condition Acknowledge bit Stop condition

■ Technical Data (continued)

3. Video output synchronization

1) Video output synchronization with no resistor

At 9 V(25ºC) white signal input, the synchronization capability of the Video output is as follows in Figure 1:

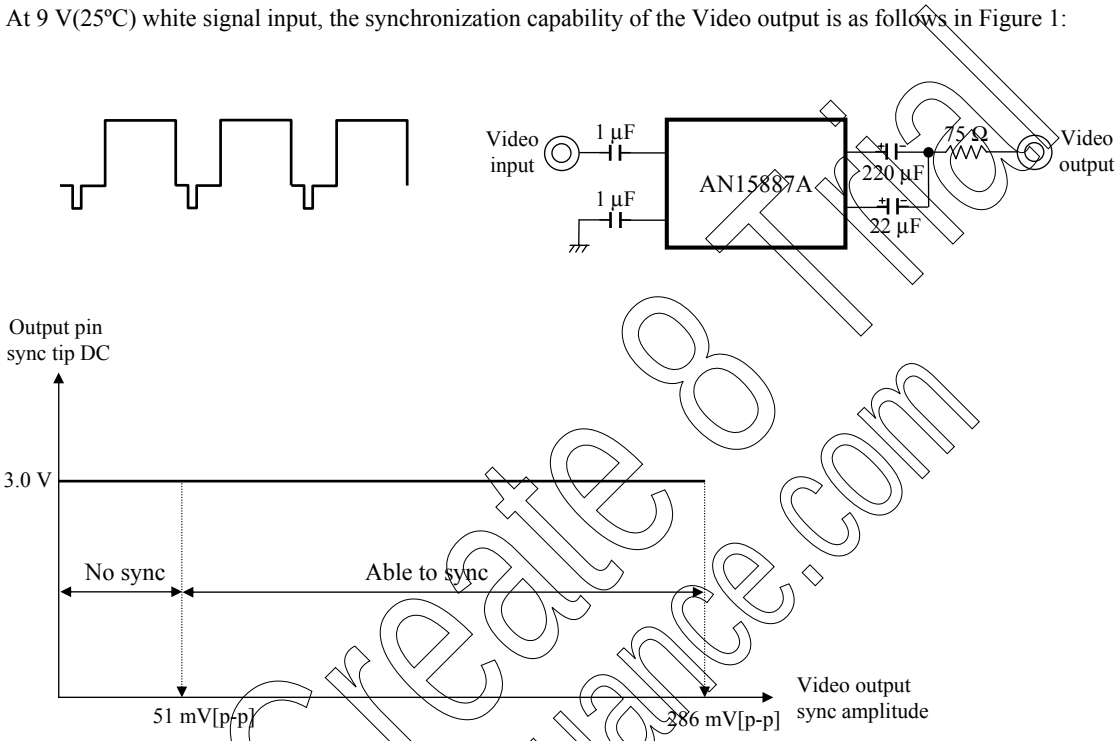


Fig. 1. Output sync capability.

At 9 V(25ºC) white signal input, for successful synchronization, the Video output sync amplitude must be at least 51 mV[p-p].

■ Technical Data (continued)

3. Video output synchronization (continued)

2) Video output synchronization with series input resistor

At 9 V (25ºC) white signal input, the synchronization capability of the video output (with series input resistor) is as follows in Figure 2 and Figure 3 :

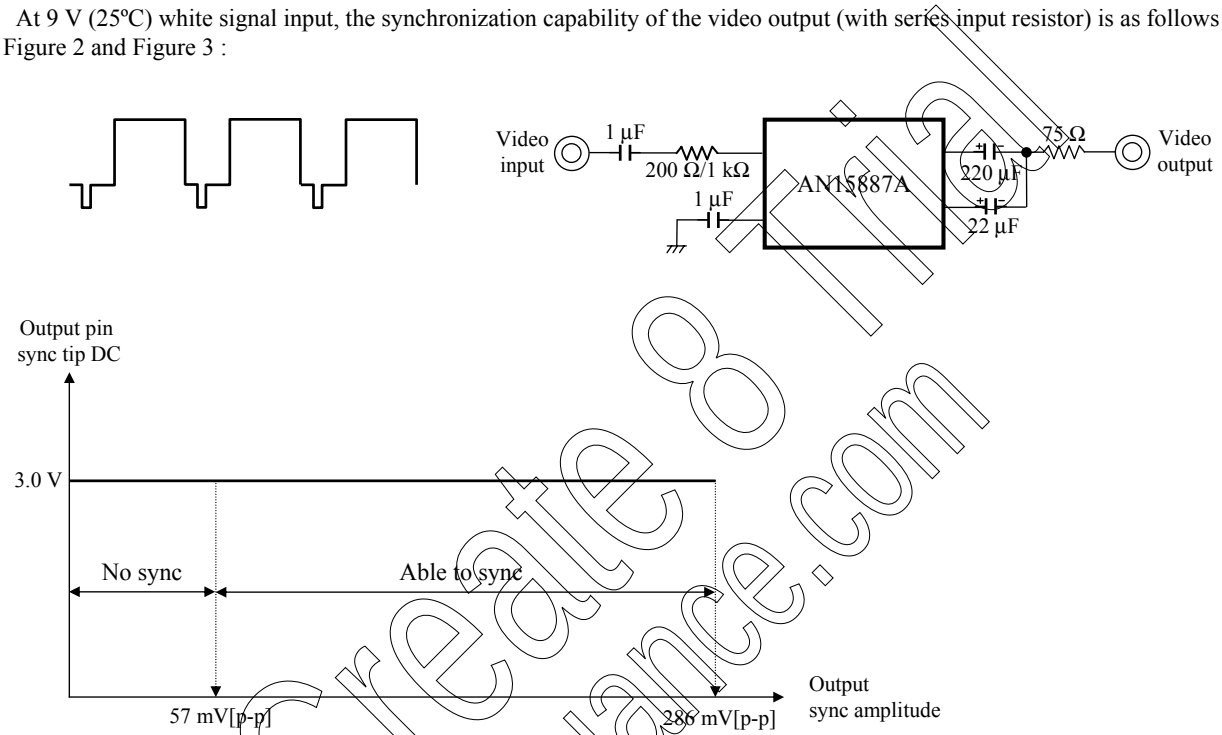


Fig. 2. Output sync capability with 200 Ω series input resistor.

At 9 V (25ºC) white signal input with 200 Ω series input resistor, for successful synchronization, the video output sync amplitude must be at least 57 mV[p-p].

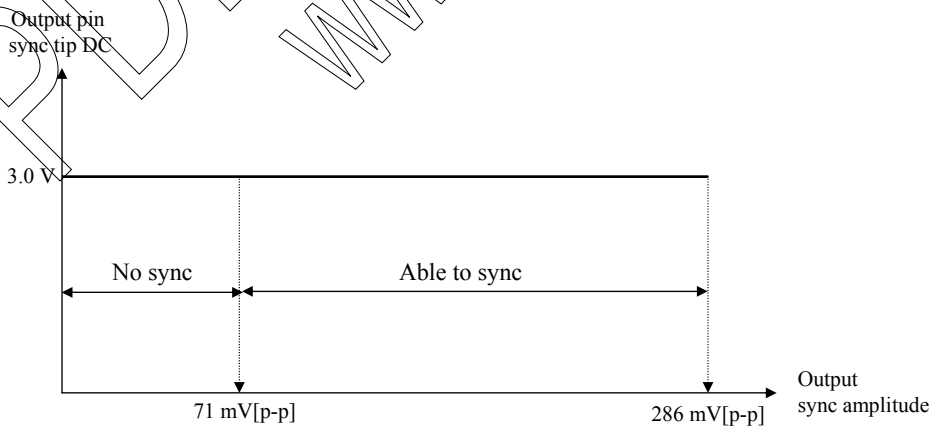


Fig 3. Output sync capability with 1 kΩ series input resistor.

At 9 V (25ºC) white signal input with 1 kΩ series input resistor, for successful synchronization, the video output sync amplitude must be at least 71 mV[p-p].

■ Technical Data (continued)

3. Video output synchronization (continued)

2) Video output synchronization with series input resistor (continued)

At 9 V (25ºC) alternate black and white signal input, the synchronization capability of the Video output (with series input resistor) is as follows in Figure 4 and Figure 5:

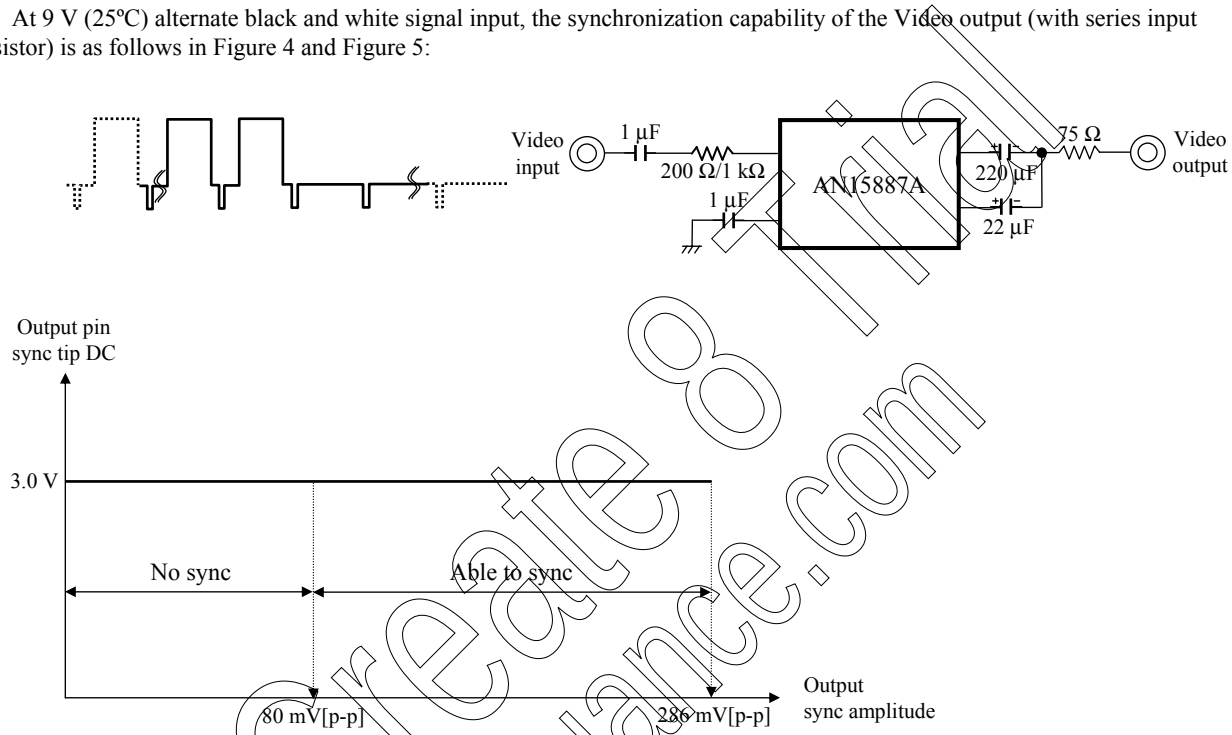


Fig 4. Output sync capability with 200 Ω series input resistor.

At 9 V (25ºC) alternate black and white signal input with 200 Ω series input resistor, for successful synchronization, the video output sync amplitude must be at least 80 mV[p-p].

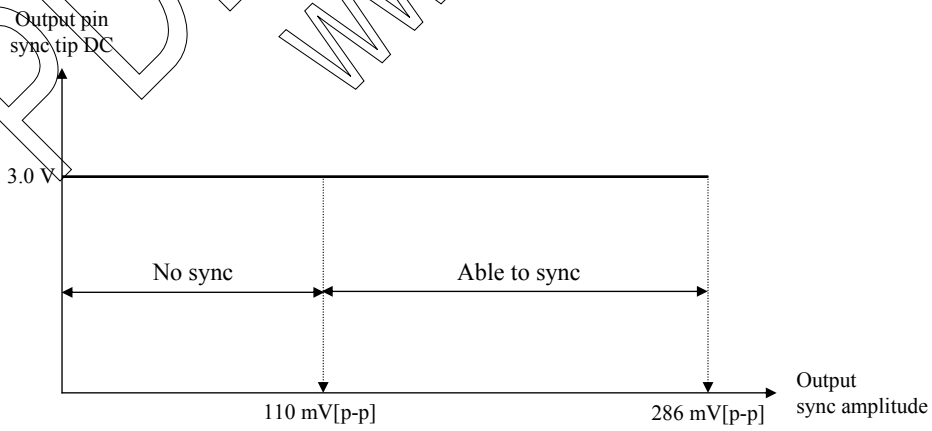


Fig 5. Output sync capability with 1 kΩ series input resistor.

At 9 V (25ºC) alternate black and white signal input with 1 kΩ series input resistor, for successful synchronization, the video output sync amplitude must be at least 110 mV[p-p].

■ Technical Data (continued)

4. BIAS1 (Pin 2) and BIAS2 (Pin 11) pins capacitors

For capacitors placed at the BIAS pins, please use capacitors with a low temperature coefficient so that the capacitor value will not fluctuate too much at different temperatures (see Figure 6 for capacitor placement).

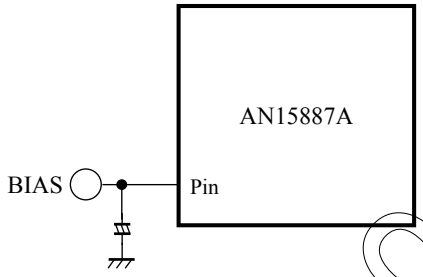


Fig. 6. BIAS pin capacitor placement.

5. GND1 (Pin 3) and GND2 (Pin 12) pin connection

It is not recommended to float either GND1 and GND2 during normal operation. Such a connection could compromise the reliabilities of the AN15887A. This is due to the internal ESD protection diode between GND1 and GND2 can be damaged by large current surge. If the abnormal operation require either GND1 and GND2 to be floated, it is advisable to connect external diodes between GND1 and GND2. The connection detail of external diodes is illustrated in Figure 7.

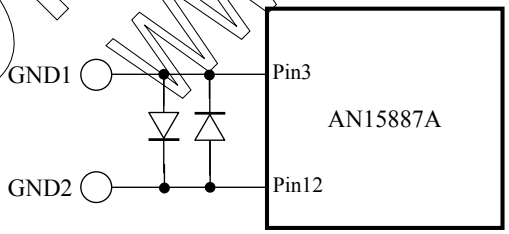


Fig. 7. External diodes

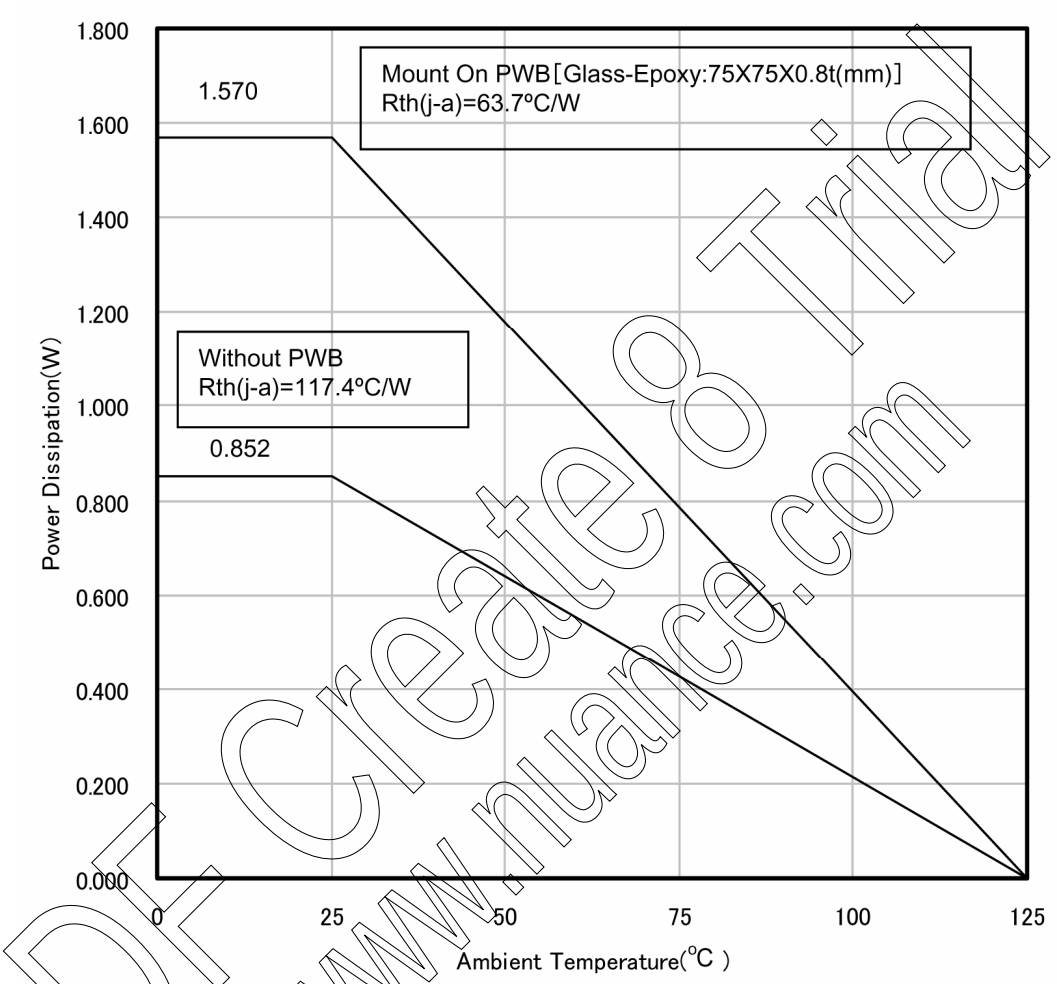
Recommended diode characteristics:

a. Forward Voltage (V_F) ≥ 1.1 V at 1.0 A

b. Junction Capacitance ≤ 12 pF at reverse voltage (V_R) = 4.0 V

■ Technical Data (continued)

6. P_D — T_a diagram



■ Usage Notes

1. This IC is intended to be used for general electronic equipment [car navigation].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Medical equipment for life support
     (3) Submarine transponder
     (4) Control equipment for power plant
     (5) Disaster prevention and security device
     (6) Weapon
     (7) Others : Applications of which reliability equivalent to (1) to (7) is required
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the ■ Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (power supply fault), output pin-GND short (ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When using the LSI for new models, verify the safety including the long-term reliability for each product.
7. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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