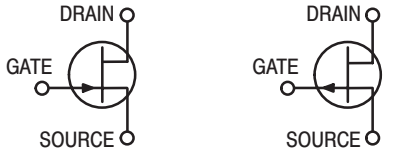
NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

AN211A

Field Effect Transistors in Theory and Practice

INTRODUCTION

There are two types of field-effect transistors, the Junction Field-Effect Transistor (JFET) and the "Metal-Oxide Semiconductor" Field-Effect Transistor (MOSFET), or Insulated-Gate Field-Effect Transistor (IGFET). The principles on which these devices operate (current controlled by an electric field) are very similar — the primary difference being in the methods by which the control element is made. This difference, however, results in a considerable difference in device characteristics and necessitates variances in circuit design, which are discussed in this note.



JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

In its simplest form the junction field-effect transistor starts with nothing more than a bar of doped silicon that behaves as a resistor (Figure 1a). By convention, the terminal into which current is injected is called the source terminal, since, as far as the FET is concerned, current originates from this terminal. The other terminal is called the drain terminal. Current flow between source and drain is related to the drain-source voltage by the resistance of the intervening material. In Figure 1b, p-type regions have been diffused into the n-type substrate of Figure 1a leaving an n-type channel between the source and drain. (A complementary p-type device is made by reversing all of the material types.) These p-type regions will be used to control the current flow between the source and the drain and are thus called gate regions.

As with any p-n junction, a depletion region surrounds the p-n junctions when the junctions are reverse biased (Figure 1c). As the reverse voltage is increased, the depletion regions spread into the channel until they meet, creating an almost infinite resistance between the source and the drain.

If an external voltage is applied between source and drain (Figure 1d) with zero gate voltage, drain current flow in the channel sets up a reverse bias along the surface of the gate, parallel to the channel. As the drain-source voltage increases, the depletion regions again spread into the channel because of the voltage drop in the channel which reverse biases the junctions. As V_{DS} is increased, the depletion regions grow until they meet, whereby any further increase in voltage is counterbalanced by an increase in the depletion region toward the drain. There is an effective increase in channel resistance that prevents any further increase in drain current. The drain-source voltage that causes this current limiting condition is called the "pinchoff" voltage (V_p). A further increase in drain-source voltage produces only a slight increase in drain current.

The variation in drain current (I_D) with drain-source voltage (V_{DS}) at zero gate-source voltage (V_{GS}) is shown in Figure 2a. In the low-current region, the drain current is linearly related to V_{DS}. As I_D increases, the "channel" begins to deplete and the slope of the I_D curve decreases. When the V_{DS} is equal to V_p, I_D "saturates" and stays relatively constant until drain-to-gate avalanche, $V_{BR(DSS)}$ is reached. If a reverse voltage is applied to the gates, channel pinch-off occurs at a lower I_D level (Figure 2b) because the depletion region spread caused by the reverse-biased gates adds to that produced by V_{DS}. Thus reducing the maximum current for any value of V_{DS}.

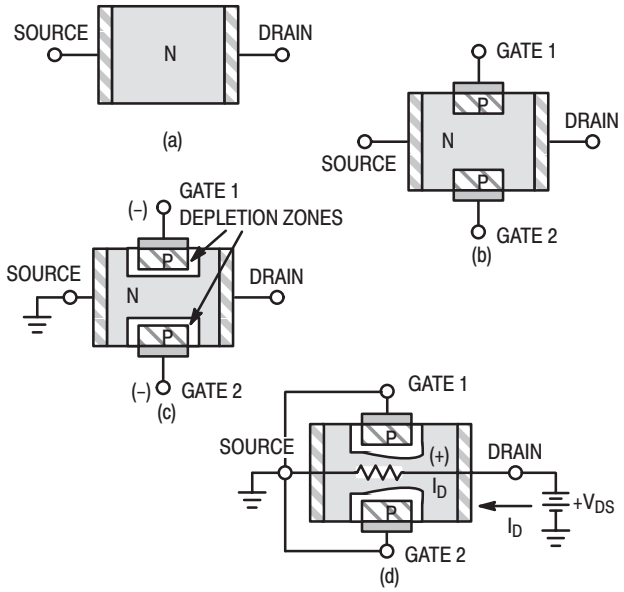


Figure 1. Development of Junction Field-Effect Transistors

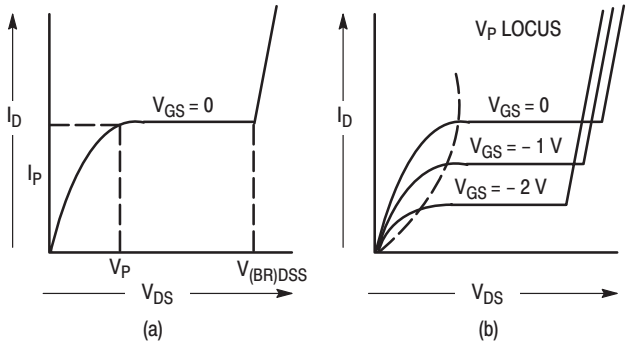
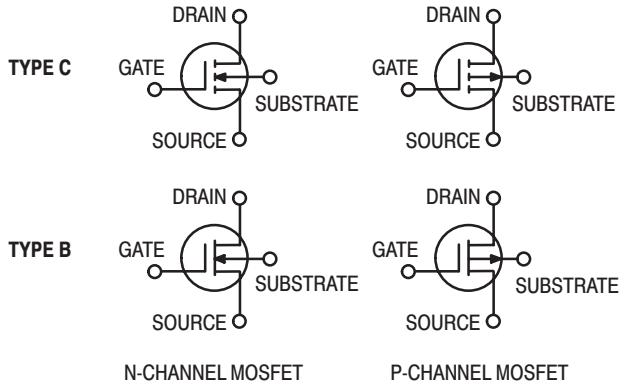


Figure 2. Drain Current Characteristics

Due to the difficulty of diffusing impurities into both sides of a semiconductor wafer, a single ended geometry is normally used instead of the two-sided structure discussed above. Diffusion for this geometry (Figure 3) is from one side only. The substrate is of p-type material onto which an n-type channel is grown epitaxially. A p-type gate is then diffused into the n-type epitaxial channel. Contact metallization completes the structure.

The substrate, which functions as Gate 2 of Figure 1, is of relatively low resistivity material to maximize gain. For the same purpose, Gate 1 is of very low resistivity material, allowing the depletion region to spread mostly into the n-type channel. In most cases the gates are internally connected together. A tetrode device can be realized by not making this internal connection.



MOS FIELD-EFFECT TRANSISTORS (MOSFET)

The metal-oxide-semiconductor (MOSFET) operates with a slightly different control mechanism than the JFET. Figure 4 shows the development. The substrate may be high resistivity p-type material, as for the 2N4351. This time two separate low-resistivity n-type regions (source and drain) are diffused into the substrate as shown in Figure 4b. Next, the surface of the structure is covered with an insulating oxide layer and a nitride layer. The oxide layer serves as a protective coating for the FET surface and to insulate the channel from the gate. However the oxide is subject to contamination by sodium ions which are found in varying quantities in all environments. Such contamination results in long term instability and changes in device characteristics. Silicon nitride is impervious to sodium ions and thus is used to shield the oxide layer from contamination. Holes are cut into the oxide and nitride layers allowing metallic contact to the source and drain. Then, the gate metal area is overlaid on the insulation, covering the entire channel region and, simultaneously, metal contacts to the drain and source are made as shown in Figure 4d. The contact to the metal area covering the channel is the gate terminal. Note that there is no physical penetration of the metal through the oxide and nitride into the substrate. Since the drain and source are isolated by the substrate, any drain-to-source current in the absence of gate voltage is extremely low because the structure is analogous to two diodes connected back to back.

The metal area of the gate forms a capacitor with the insulating layers and the semiconductor channel. The metal area is the top plate; the substrate material and channel are the bottom plate.

For the structure of Figure 4, consider a positive gate potential (see Figure 5). Positive charges at the metal side of the metal-oxide capacitor induce a corresponding negative charge at the semiconductor side. As the positive charge at the gate is increased, the negative charge “induced” in the semiconductor increases until the region beneath the oxide effectively becomes an n-type semiconductor region, and current can flow between drain and source through the “induced” channel. In other words, drain current flow is “enhanced” by the gate potential. Thus drain current flow can be modulated by the gate voltage; i.e. the channel resistance is directly related to the gate voltage. The n-channel structure may be changed to a p-channel device by reversing the material types.

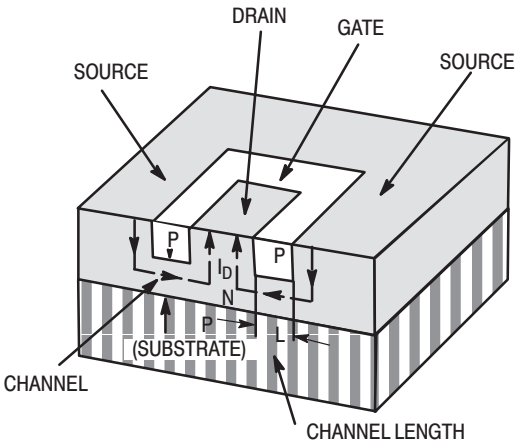


Figure 3. Junction FET with Single-Ended Geometry

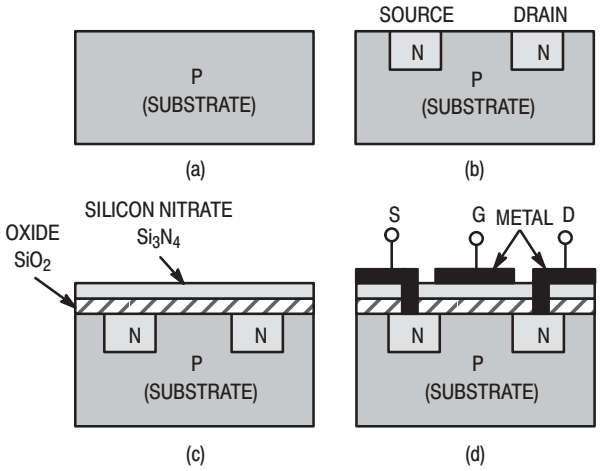


Figure 4. Development of Enhancement-Mode N-Channel MOSFET

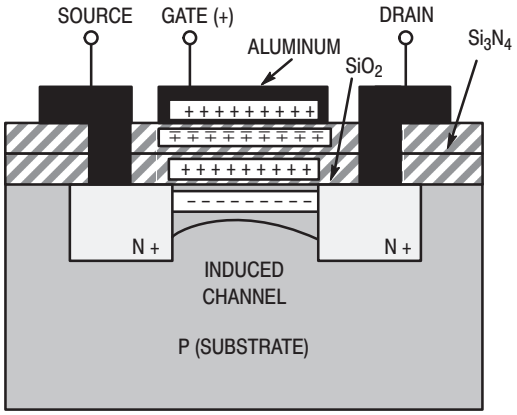


Figure 5. Channel Enhancement. Application of Positive Gate Voltage Causes Redistribution of Minority Carriers in the Substrate and Results in the Formation of a Conductive Channel Between Source and Drain

An equivalent circuit for the MOSFET is shown in Figure 6. Here, $C_{g(ch)}$ is the distributed gate-to-channel capacitance representing the nitride-oxide capacitance. C_{gs} is the gate-source capacitance of the metal gate area overlapping the source, while C_{gd} is the gate-drain capacitance of the metal gate area overlapping the drain. $C_{d(sub)}$ and $C_{s(sub)}$ are junction capacitances from drain to substrate and source to substrate. Y_{fs} is the transadmittance between drain current and gate-source voltage. The modulated channel resistance is r_{ds}. R_D and R_S are the bulk resistances of the drain and source.

The input resistance of the MOSFET is exceptionally high because the gate behaves as a capacitor with very low leakage ($r_{in} \approx 10^{14}\ \Omega$). The output impedance is a function of r_{ds} (which is related to the gate voltage) and the drain and source bulk resistances (R_D and R_S).

To turn the MOSFET "on", the gate-channel capacitance, $C_{g(ch)}$, and the Miller capacitance, C_{gd}, must be charged. In turning "on", the drain-substrate capacitance, $C_{d(sub)}$, must be discharged. The resistance of the substrate determines the peak discharge current for this capacitance.

The FET just described is called an enhancement-type MOSFET. A depletion-type MOSFET can be made in the following manner: Starting with the basic structure of Figure 4, a moderate resistivity n-channel is diffused between the source and drain so that drain current can flow when the gate potential is at zero volts (Figure 7). In this manner, the MOSFET can be made to exhibit depletion characteristics. For positive gate voltages, the structure enhances in the same manner as the device of Figure 4. With negative gate voltage, the enhancement process is reversed and the channel begins to deplete of carriers as seen in Figure 8. As with the JFET, drain-current flow depletes the channel area nearest the drain first.

The structure of Figure 7, therefore, is both a depletion-mode and an enhancement-mode device.

MODES OF OPERATION

There are two basic modes of operation of FET's — depletion and enhancement. Depletion mode, as previously mentioned, refers to the decrease of carriers in the channel due to variation in gate voltage. Enhancement mode refers to the increase of carriers in the channel due to application of gate voltage. A third type of FET that can operate in both the depletion and the enhancement modes has also been described.

The basic differences between these modes can most easily be understood by examining the transfer characteristics of Figure 9. The depletion-mode device has considerable drain-current flow for zero gate voltage. Drain current is reduced by applying a reverse voltage to the gate terminal. The depletion-type FET is not characterized with forward gate voltage.

The depletion/enhancement mode type device also has considerable drain current with zero gate voltage. This type device is defined in the forward region and may have usable forward characteristics for quite large gate voltages. Notice that for the junction FET, drain current may be enhanced by forward gate voltage only until the gate-source p-n junction becomes forward biased.

The third type of FET operates only in the enhancement mode. This FET has extremely low drain current flow for zero gate-source voltage. Drain current conduction occurs for a V_{GS} greater than some threshold value, $V_{GS(th)}$. For gate voltages greater than the threshold, the transfer characteristics are similar to the depletion/enhancement mode FET.

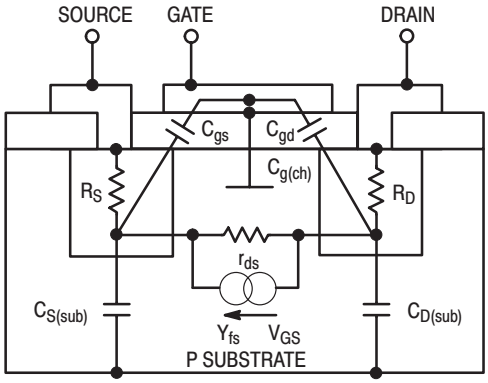


Figure 6. Equivalent Circuit of Enhancement-Mode MOSFET

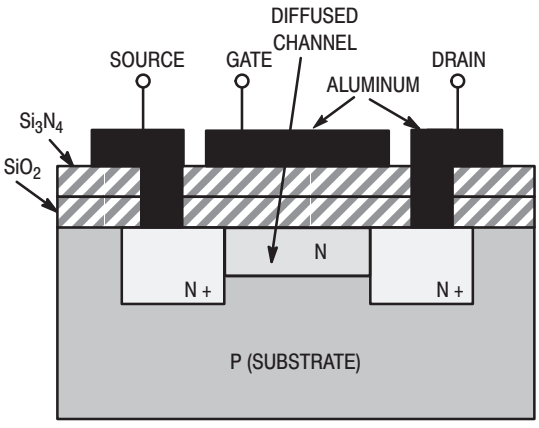


Figure 7. Depletion Mode MOSFET Structure. This Type of Device May Be Designed to Operate in Both the Enhancement and Depletion Modes

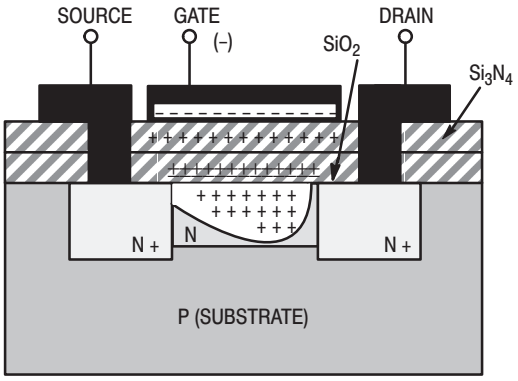


Figure 8. Channel Depletion Phenomenon. Application of Negative Gate Voltage Causes Redistribution of Minority Carriers in Diffused Channel and Reduces Effective Channel Thickness. This Results in Increased Channel Resistance.

ELECTRICAL CHARACTERISTICS

Because the basic mode of operation for field-effect devices differs greatly from that of conventional junction transistors, the terminology and specifications are necessarily different. An understanding of FET terminology and characteristics are necessary to evaluate their comparative merits from data-sheet specifications.

Static Characteristics

Static characteristics define the operation of an active device under the influence of applied dc operating conditions. Of primary interest are those specifications that indicate the effect of a control signal on the output current. The V_{GS} – I_D transfer characteristics curves are illustrated in Figure 9 for the three types of FETs. Figure 10 lists the data-sheet specifications normally employed to describe these curves, as well as the test circuits that yield the indicated specifications.

Of additional interest is the special case of tetrode-connected devices in which the two gates are separately accessible for the application of a control signal. The pertinent specifications for a junction tetrode are those which define drain-current cutoff when one of the gates is connected to the source and the bias voltage is applied to the second gate. These are usually specified as $V_{G1S(off)}$, Gate 1 — source cutoff voltage (with Gate 2 connected to source), and $V_{G2S(off)}$, Gate 2 — source cutoff voltage (with Gate 1 connected to source). The gate voltage required for drain current cutoff with one of the gates connected to the

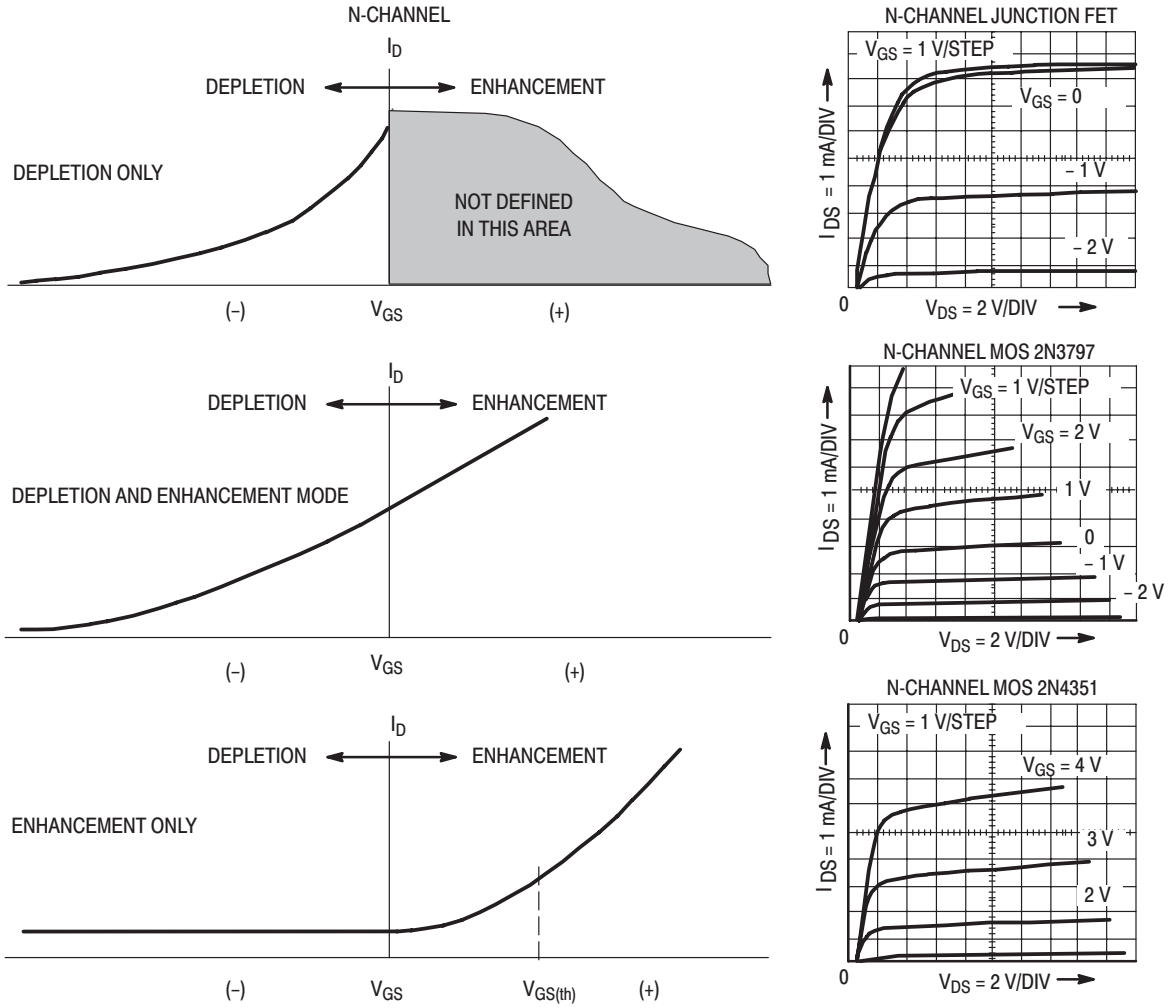


Figure 9. Transfer Characteristics and Associated Scope Traces for the Three FET Types

source is always higher than that for the triode-connected case where both gates are tied together.

Reach-through voltage is another specification uniquely applicable to tetrode-connected devices. This defines the amount of difference voltage that may be applied to the two gates before the depletion region of one spreads into the junction of the other — causing an increase in gate current to some small specified value. Obviously, reach-through is an undesirable condition since it causes a decrease in input resistance as a result of an increased gate current, and large amounts of reach-through current can destroy the FET.

Gate Leakage Current

Of interest to circuit designers is the input resistance of an active component. For FETs, this characteristic is specified in the form of I_{GSS} — the reverse-bias gate-to-source current with the drain shorted to the source (Figure 11). As might be expected, because the leakage current across a reverse-biased p-n junction (in the case of a JFET) and across a capacitor (in the case of a MOSFET) is very small, the input resistance is extremely high. At a temperature of 25°C, the JFET input resistance is hundreds of megohms while that of a MOSFET is even greater. For junction devices, however, input resistance may decrease by several orders of magnitude as temperature is raised to 150°C. Such devices, therefore, have gate-leakage current specified at two temperatures. Insulated-gate FETs are not drastically affected by temperature, and their input resistance remains extremely high even at elevated temperatures.

Gate leakage current may also be specified as I_{GDO} (leakage between gate and drain with the source open), or as I_{GSO} (leakage between gate and source with the drain open). These usually result in lower values of leakage current and do not represent worst-case conditions. The I_{GSS} specification, therefore, is usually preferred by the user.

Voltage Breakdown

A variety of specifications can be used to indicate the maximum voltage that may be applied to various elements of a FET. Among those in common use are the following:

$V_{(BR)GSS}$ = Gate-to-source breakdown voltage

$V_{(BR)DGO}$ = Drain-to-gate breakdown voltage

$V_{(BR)DSX}$ = Drain-to-source breakdown voltage (normally used only for MOSFETs)

In addition, there may be ratings and specifications indicating the maximum voltages that may be applied between the individual gates and the drain and source (for tetrode connected devices). Obviously, not all of these specifications are found on every data sheet since some of them provide the same information in somewhat different form. By understanding the various breakdown mechanisms, however, the reader should be able to interpret the intent of each specification and rating. For example:

In junction FETs, the maximum voltage that may be applied between any two terminals is the lowest voltage that will lead to breakdown or avalanche of the gate junction. To measure $V_{(BR)GSS}$ (Figure 12a), an increasingly higher reverse voltage is applied between the gate and the source. Junction breakdown is indicated by an increase in gate current (beyond I_{GSS}) which signals the beginning of avalanche.

Some reflection will reveal that for junction FETs, the $V_{(BR)DGO}$ specification really provides the same information as $V_{(BR)GSS}$. For this measurement, an increasing voltage is applied between drain and gate. When this applied voltage becomes high enough, the drain-gate junction will go into avalanche, indicated either by a significant increase in drain current or by an increase in gate current (beyond I_{DGO}). For both $V_{(BR)DGO}$ and $V_{(BR)GSS}$ specifications, breakdown should normally occur at the same voltage value.

From Figure 2 it is seen that avalanche occurs at a lower value of V_{DS} when the gate is reverse biased than for the zero-bias condition. This is caused by the fact that the reverse-bias gate voltage adds to the drain voltage, thereby increasing the effective voltage across the junction. The maximum amount of drain-source voltage that may be applied $V_{DS(max)}$ is, therefore, equal to $V_{(BR)DGO}$ minus V_{GS}, which indicates avalanche with reverse bias gate voltage applied.

For MOSFETs, the breakdown mechanism is somewhat different. Consider, for example, the enhancement-mode structure of Figure 5. Here, the gate is completely insulated from the drain, source, and channel by an oxide-nitride layer. The breakdown voltage between the gate and any of the other elements, therefore, is dependent on the thickness and purity of this insulating layer, and represents the voltage that will physically puncture the layer. Consequently, the voltage must be specified separately.

The drain-to-source breakdown is a different matter. For enhancement mode devices, with the gate connected to the source (the cutoff condition) and the substrate floating, there is no effective channel between drain and source and the applied drain-source voltage appears across two opposed series diodes, represented by the source-to-substrate and substrate-to-drain junctions. Drain current remains at a very low level (picoamperes) as drain voltage is increased until the drain voltage reaches a value that causes reverse (avalanche) breakdown of the diodes. This particular condition, represented by $V_{(BR)DSS}$, is indicated by an increase in I_D above the I_{DSS} level, as shown in Figure 12b.

For depletion/enhancement mode devices, the $V_{(BR)DSS}$ symbol is sometimes replaced by $V_{(BR)DSX}$. Note that the principal difference between the two symbols is the replacement of the last subscript s with the subscript x. Whereas the s normally indicates that the gate is shorted to the source, the x indicates that the gate is biased to cutoff or beyond. To achieve cutoff in these devices, a depleting bias voltage must be applied to the gate, Figure 12b.

An important static characteristic for switching FETs is the "on" drain-source voltage $V_{DS(on)}$. This characteristic for the MOSFETs is a function of V_{GS}, and resembles the $V_{CE(sat)}$ versus I_B characteristics of junction transistors. The curve for these characteristics can be used as a design guide to determine the minimum gate voltage necessary to achieve a specified output logic level.

Dynamic Characteristics

Unlike the static characteristics, the dynamic characteristics of field-effect transistors apply equally to all FETs. The conditions and presentation of the dynamic characteristics, however, depend largely upon the intended application. For example, the following table indicates the dynamic characteristics needed to adequately describe a FET for various applications.

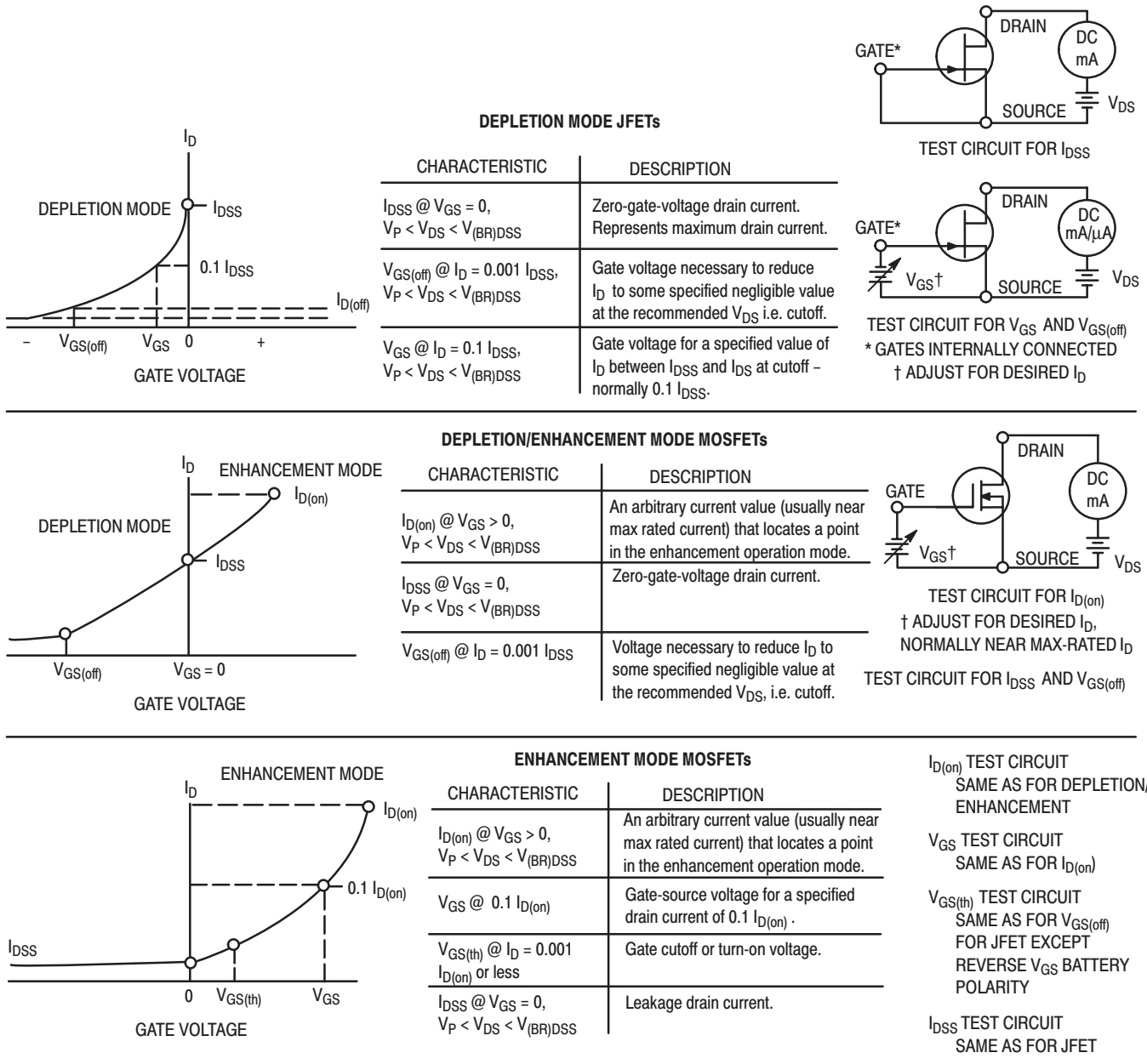


Figure 10. Static Characteristics for the Three FET Types Are Defined by the Above Curves, Tables, and Test Circuits

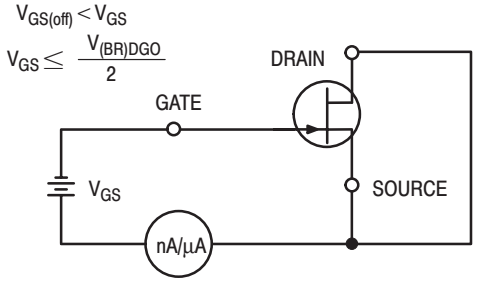


Figure 11. Test Circuit for Leakage Current

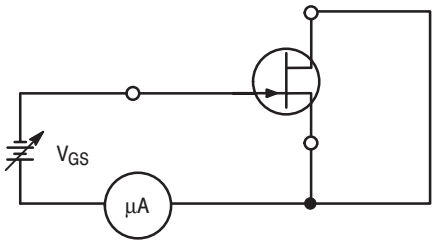


Figure 12a. $V_{(BR)GSS}$ Test Circuit

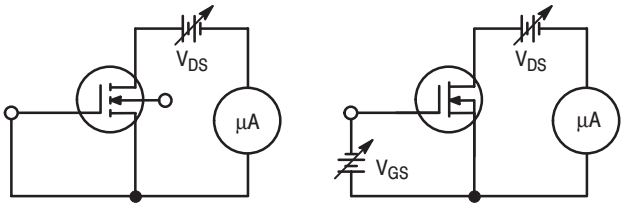


Figure 12b. $V_{(BR)DSS}$ and $V_{(BR)DSX}$ Test Circuit (Usually Used for MOSFETs Only).

Audio	RF-IF	Switching	Chopper
y_{fs} (1 kHz)	y_{fs} (1 kHz)		
C_{iss}	C_{iss}	C_{iss}	C_{iss}
C_{rss}	C_{rss}	C_{rss}	C_{rss}
y_{os} (1 kHz)	GP	$Cd_{(sub)}$	$Cd_{(sub)}$
NF	$Re(y_{is})$ (HF)	$r_{ds(on)}$	$r_{ds(on)}$
	$Re(y_{os})$ (HF)	t_{d1}, t_{d2}	
	NF	t_r, t_f	

y_{fs} The forward transadmittance is a key dynamic characteristic for field-effect transistors. It serves as a basic design parameter in audio and rf circuits and is a widely accepted figure of merit for devices.

Because field-effect transistors have many characteristics similar to those of vacuum tubes, and because many engineers still are more comfortable with tube parameters, the symbol g_m used for tube transconductance is often specified instead of y_{fs}. To further confuse things, the "g" school also uses a variety of subscripts. In addition to g_m, some data sheets show g_{fs} while others even show g_{21}.

Regardless of the symbol used, y_{fs} defines the relation between an input signal voltage and an output signal current:

$$y_{fs} = \Delta I_D / \Delta V_{GS} \Big|_{V_{DS} = K}$$

The unit is the mho — current divided by voltage. Figure 13 is a typical y_{fs} test circuit for a junction FET.

As a characteristic of all field-effect devices, y_{fs} is specified at 1 kHz with a V_{DS} the same as that for which $I_{D(on)}$ or I_{DSS} is characterized. Since y_{fs} has both real and imaginary components, but is dominated by the real component at low frequency, the 1 kHz characteristic is given as an absolute magnitude and indicated as $|y_{fs}|$.

It is interesting to note that y_{fs} varies considerably with I_D due to nonlinearity in the $I_D - V_{GS}$ characteristics. This variation, for a typical n-channel, JFET is illustrated in Figure 14. Obviously, the operating point must be carefully selected to provide the desired y_{fs} and signal swing.

For tetrode-connected FETs, three y_{fs} measurements are usually specified on data-sheet tables. One of these, with the two gates tied together, provides a y_{fs} value for the condition where a signal is applied to both gates simultaneously; the others provide the y_{fs} for the two gates individually. Generally, with the two gates tied together, y_{fs} is higher and more gain may be realized in a given circuit. Because of the increased capacitance, however, gain-bandwidth product is much lower.

For rf field-effect transistors, an additional value of y_{fs} is sometimes specified at or near the highest frequency of operation. This value should also be measured at the same voltage conditions as those used for $I_{D(on)}$ or I_{DSS}. Because of the importance of the imaginary component at radio frequencies, the high frequency y_{fs} specification should be a complex representation, and should be given either in the specifications table or by means of curves showing typical variations, as in Figure 15 for the MPF102 JFET.

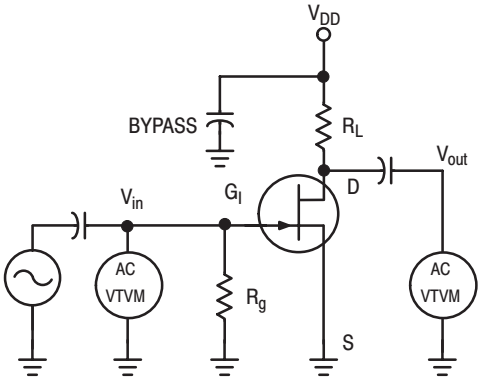
The real portion of this high-frequency y_{fs}, Re (y_{fs}) or G_{21}, is usually considered a significant figure of merit.

y_{os} Another FET parameter that offers a direct vacuum tube analogy is y_{os}, the output admittance:

$$y_{os} = \Delta I_D / \Delta V_{DS} \Big|_{V_{GS} = K}$$

In this case, the analogous tube parameter is r_p — i.e., $y_{os} = 1/r_p$. For depletion mode devices, y_{os} is measured with gate and source grounded (see Figure 16). For enhancement mode units, it is measured at some specified V_{GS} that permits substantial drain-current flow.

As with y_{fs}, many expressions are used for y_{os}. In addition to the obvious parallels such as y_{22}, g_{os}, and g_{22}, it is also sometimes specified as r_d, where $r_d = 1/y_{os}$.



$$Y_{fsl} = \frac{V_{out}}{V_{in}\ R_L}$$

R_g TYPICALLY 1 MΩ
R_L OF SUCH VALUE AS TO CAUSE NEGLIGIBLE DC DROP AT I_{DSS}

Figure 13. Typical y_{fs} Test Circuit

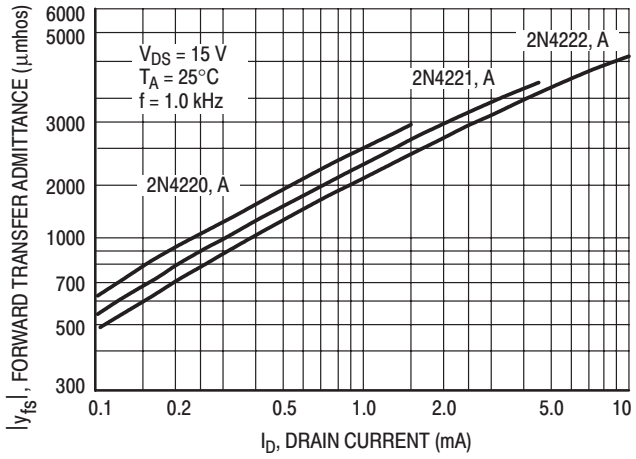


Figure 14. Forward Transfer Admittance versus Drain Current for Typical JFETs

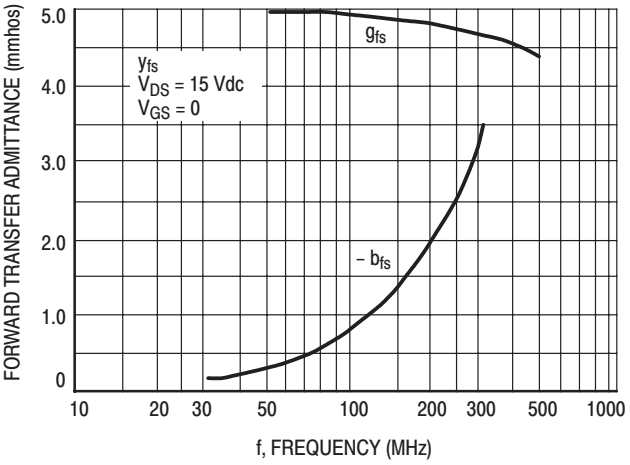
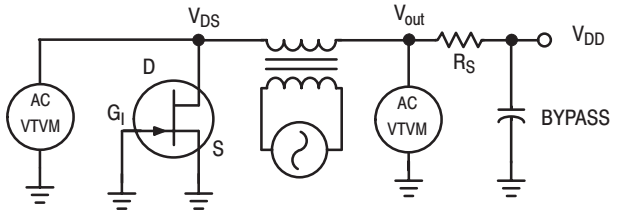


Figure 15. Forward Transfer Admittance versus Frequency



$$Y_{OS} = \frac{V_{out}}{V_{DS}\ R_S}$$

R_S OF SUCH VALUE AS TO CAUSE NEGLIGIBLE DC DROP.
R_S SENSES AC DRAIN CURRENT

Figure 16. y_{os} Measurement Circuit for Depletion FETs

Voltages and frequencies for measuring y_{os} should be exactly the same as those for measuring y_{fs}. Like y_{fs}, it is a complex number and should be specified as a magnitude at 1 kHz and in complex form at high frequencies.

μ Closely related to y_{os} and y_{fs} is the amplification factor, μ:

$$\mu = \Delta V_{DS}/\Delta V_{GS} \Big|_{I_D = K}$$

The amplification factor does not appear on the field-effect transistor registration format but can be calculated as y_{fs}/y_{os}. For most small-signal applications, μ has little circuit significance. It does, however, serve as a general indication of the quality of the field-effect manufacturing process.

C_{iss} The common-source-circuit input capacitance, C_{iss}, takes the place of y_{is} in low-frequency field-effect transistors. This is because y_{is} is entirely capacitive at low frequencies. C_{iss} is conveniently measured in the circuit of Figure 17 for the tetrode JFET. As with y_{fs}, two measurements are necessary for tetrode-connected devices.

At very high frequencies, the real component of y_{is} becomes important so that rf field-effect transistors should have y_{is} specified as a complex number at the same conditions as other high-frequency parameters. For tetrode-connected rf FETs, reading of both Gate 2 to source and Gate 1 tied to Gate 2 are necessary.

In switching applications C_{iss} is of major importance since a large voltage swing at the gate must appear across C_{iss}. Thus, C_{iss} must be charged by the input voltage before turn-on effectively begins.

C_{rss} Reverse transfer admittance (y_{rs}) does not appear on FET data sheets. Instead C_{rss}, the reverse transfer capacitance, is specified at low frequency. Since y_{rs} for a field-effect transistor remains almost completely capacitive and relatively constant over the entire usable FET frequency spectrum, the low-frequency capacitance is an adequate specification. C_{rss} is measured by the circuit of Figure 18. For tetrode FETs, values should be specified for Gate 1 and for both gates tied together.

Again, for switching applications C_{rss} is a critical characteristic. Similar to the C_{ob} of a junction transistor, C_{rss} must be charged and discharged during the switching interval. For a chopper application, C_{rss} is the feedthrough capacitance for the chopper drive.

$C_{d(sub)}$ For the MOSFET, the drain-substrate junction capacitance becomes an important characteristic affecting the switching behavior. $C_{d(sub)}$ appears in parallel with the load in a switching circuit and must be charged and discharged between the two logic levels during the switching interval.

Noise Figure (NF) Like all other active components, field-effect transistors generate a certain amount of noise. The noise figure for field-effect transistors is normally specified on the data sheet as “spot noise”, referring to the noise at a particular frequency. The noise figure will vary with frequency and also with the resistance at the input of the device. Typical graphs of such variations are illustrated in Figure 19 for the 2N5458. From graphs of this kind the designer can anticipate the noise level inherent in his design.

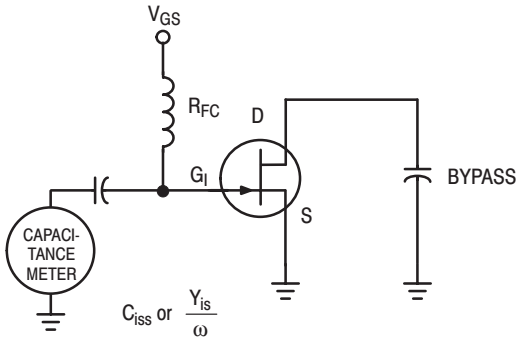
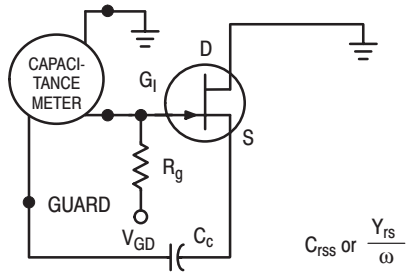


Figure 17. C_{iss} Measurement Circuit



(a) $V_{GD} = -V_{DS}$
R_g TYPICALLY 1 MΩ
C_c AC SOURCE TO GUARD SIGNAL.

Figure 18. Recommended C_{rss} Test Circuit

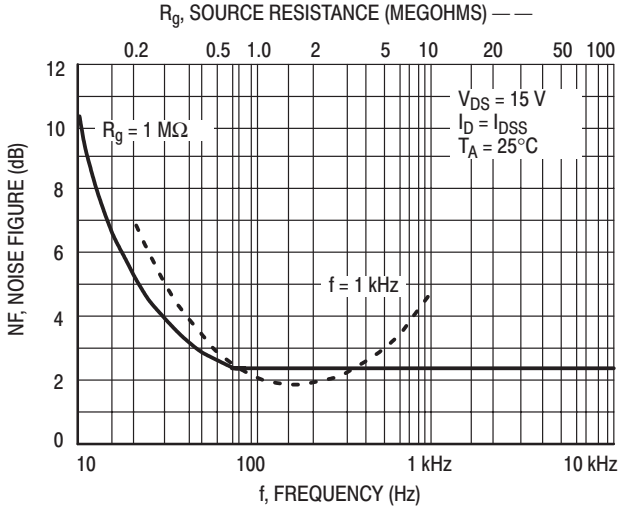


Figure 19. Typical Variations of FET Noise Figure with Frequency and Source Resistance

$r_{ds(on)}$ Channel resistance describes the bulk resistance of the channel in series with the drain and source. From an applications standpoint, it is important primarily for switching and chopper circuits since it affects the switching speed and determines the output level. To complete the confusion of multiple symbols for FET parameters, channel resistance is sometimes indicated as $r_{d(on)}$ and also as r_{DS} and r_{ds}. In either case, however, it is measured, for JFETs, by tying the gates to the source, setting all terminals equal to 0 Vdc, and applying an ac voltage from drain to source (see Figure 20). The magnitude of the ac voltage should be kept low so that there will be no pinchoff in the channel. Insulated-gate FETs may be measured with dc gate bias in the enhancement mode.

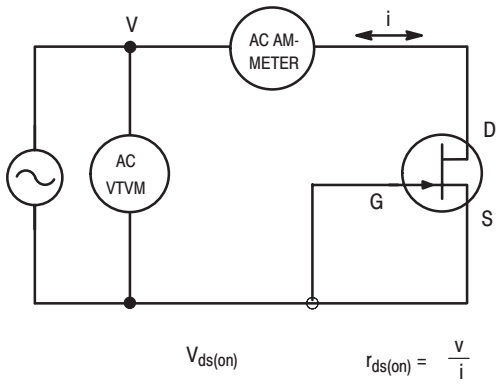


Figure 20. Circuit for Measuring JFET Channel Resistance

APPLICATIONS

Device Selection

Obviously, different applications call for special emphasis on specific characteristics so that a simple figure of merit that compares devices for all potential uses would be hard to formulate. Nevertheless, an attempt to pinpoint the characteristics that are most significant for various applications has been made* to permit a rapid, first-order evaluation of competitive devices.

The most important single FET parameter, one that applies for any amplifier application, is y_{fs}. This parameter, or one of its many variations, is specified on most data sheets, yet some evaluation is required to come up with a reasonable comparison. For example, in the table of electrical characteristics on most JFET data sheets, y_{fs} is specified at I_{DSS} (V_{GS} = 0) where, for JFETs devices, y_{fs} is maximum. This is illustrated in Figure 14, where typical variations of y_{fs} as a function of I_D are plotted. For some small-signal applications, the I_{DSS} (V_{GS} = 0) point can actually be used as a dc operating point because small-signal excursions into the forward bias region will not actually cause the gate-source junction to become forward-biased. However, in most practical uses, some bias is necessary to allow for the anticipated signal swing; and it must be recognized the y_{fs} goes down as the bias is increased.

It is seen, also, that maximum y_{fs} increases as I_{DSS} increases so that, where maximum y_{fs} is important, a device with a high I_{DSS} specification is normally desirable.

On the other hand, where power dissipation is a factor to be considered, the figure of merit $y_{fs}/V_{GS(off)}$ I_{DSS} has been proposed. This term factors in not only I_{DSS}, which should be low if power dissipation is to be low, but also $V_{GS(off)}$, which indicates maximum input voltage swing. Since the signal peaks are represented by $V_{GS} = V_{GS(off)}$ and V_{GS} = 0, the lower $V_{GS(off)}$, the higher the figure of merit. And, for amplifier applications requiring a large signal swing, $V_{(BR)GSS}/V_{GS(off)}$ (assuming that $V_{GS(off)}$ is the "pinch-off" voltage) is a satisfactory merit figure because it indicates the ratio of maximum and minimum drain voltages.

* Christiansen, Donald, "Semiconductors: The New Figures of Merit," EEE, October, 1965.

For high-frequency circuits, the input capacitance (C_{iss}) and the Miller-effect capacitance (C_{rss}) become important, so $y_{fs}/(C_{iss} + C_{rss})$ indicates a relative measure of device performance. For switching and chopper circuits, a figure of merit is not often useful. Here the magnitudes of C_{iss}, C_{rrs}, $C_{d(sub)}$ and r_{ds} are of primary interest.

Circuits

The types of circuits that can utilize FETs are practically unlimited. In fact, many circuits designed to utilize small–signal pentode tubes can utilize FETs with only minor modifications. For example, the circuit in Figure 21 shows a typical rf stage for a broadcast-band auto radio. In this circuit, a MPF102 n-channel JFET has replaced the 12BL6 pentode normally employed. The specifications for the two devices, including the AGC characteristics, are similar enough to perform adequately in the circuit of Figure 21.

In an audio application, a field-effect transistor such as the 2N5460 can be combined with a high voltage bipolar transistor to make a simple line-operated phonograph amplifier such as that shown in Figure 22. The ceramic pickup is connected through a potentiometer volume control to the field-effect transistor. Collector current of the transistor, in turn, is set by the potentiometer in the source of the FET. With the proper bipolar output transistor, the circuit can be driven directly from the rectified line voltage, while the low voltage for the FET can be derived from a voltage divider in the power supply line.

Figure 23 shows three basic chopper circuits. The advantage of the more complex series-shunt circuit (24c) is that it balances out the leakage currents of the FETs in order to reduce voltage error and is used to attain high chopping frequencies. From an applications standpoint, the FET circuit is superior to a junction transistor circuit in that there is no offset voltage with the FET turned on. On the minus side, however, the field-effect-transistor chopper generally has a higher series resistance ($r_{ds(on)}$) than the junction transistor.

As newer and better FETs are introduced and as a larger number of designers learn to use them, the range of applications of FETs should broaden considerably.

With its high input impedance, the field-effect transistor will play an important role in input circuitry for instrumentation and audio applications where low-impedance junction transistors have generally been least successful.

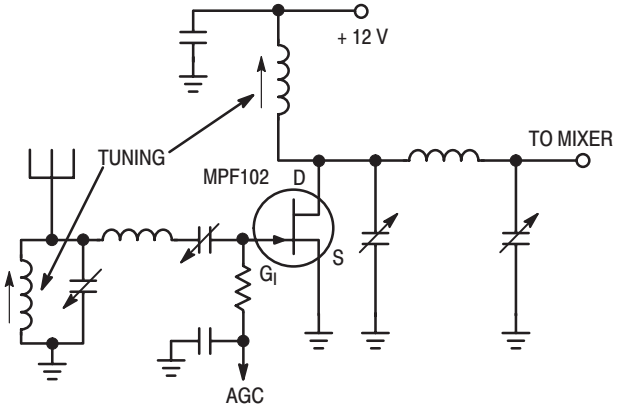


Figure 21. RF Stage of Broadcast Auto Radio

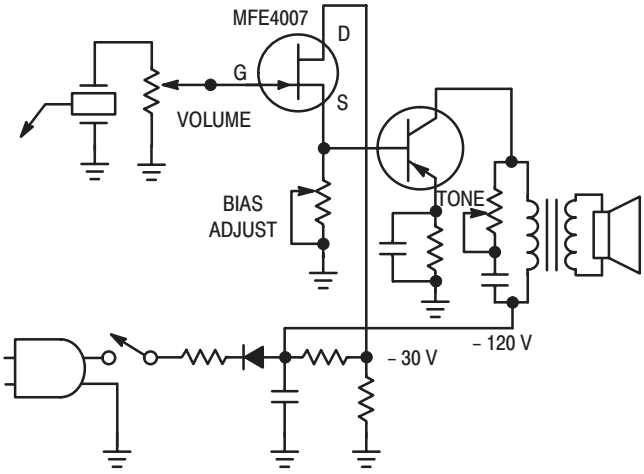


Figure 22. Line Operated Phono Amplifiers

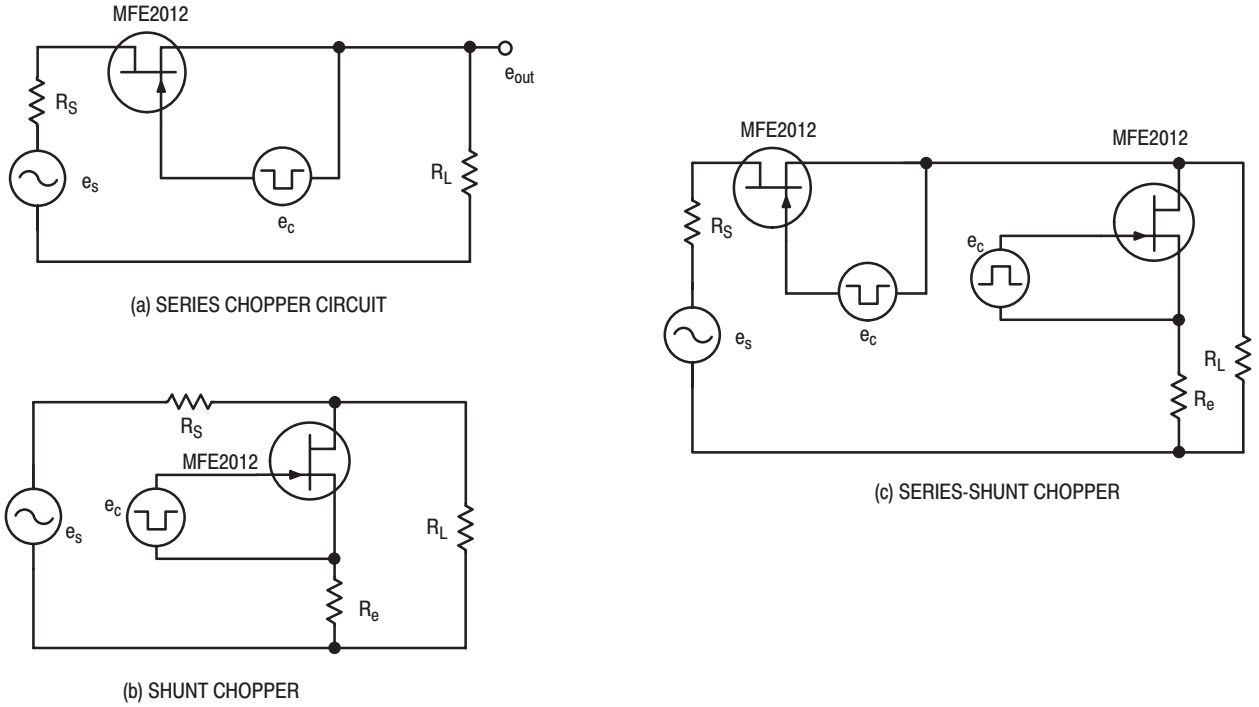


Figure 23. FET Chopper Circuits

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