APPLICATION NOTE

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Metastability tests for the 74F786 – a 4-input asynchronous bus arbiter

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INTRODUCTION

Under contract with Signetics, Mr. Thomas J. Chaney of Washington University, St. Louis tested a set of nineteen 74F786 samples (packages) to determine the metastable state recovery statistics for the circuits. The tests were conducted using a procedure described in a paper entitled *"Characterization and Scaling of MOS Flip-Flop Performance"*, (section IV), by T. Chaney and F. Rosenberger, presented at the CalTech Conference on VLSI, January 1979. The general test procedure was to test all 19 packages under one condition, then test the best, worst, and an average package in more detail. According to Mr. Chaney, the test results from the 19 packages formed one of the tightest groupings that he has ever seen. As the parts were numbered, package No. 7 had the fastest resolving times, No. 11 produced some of the slowest resolving times, and No. 1 had resolving times near the middle of the test results. This ranking of the test results from 3 packages remained the same throughout the balance of the test program, which supports the complete testing of only 3 packages. In general, the poorest performance resulted when the packages were heated to near 75°C with $V_{CC} = 4.5V_{DC}$ and the best performance resulted when the packages were cooled to near 0°C with $V_{CC} = 5.5V_{DC}$. The variation within one package caused by the temperature and V_{CC} changes was greater than the variation from package to package. It must be noted that none of the packages tested even approached the data sheet input to output worst case propagation delay of 10.5ns. All the packages tested for a single active output, had propagation delays of about 6ns. Typically, the parts with longer propagation delays also have slower resolving times. Thus, one would expect that the delay time needed to have only one failure in 32 years using a 10ns propagation delay part would be much longer than a value derived from just adding 10–6 = 4ns to the above calculations. thus it appears that the poorest performance measured in this study should be considered a measurement at the edge of the typical range for 74F786 parts.

It must also be noted that the tight grouping of this set of packages means that, when comparing differences between these test results, the measured error, as outlined in *"Measured Flip-Flop Responses to Marginal Triggering"*, IEETC, December 1983, is significant. This is illustrated in association with Table 5.

Test Program and Data

Throughout the test period, the connections to some of the package pins was as shown in Figure 1. The 4 input pins (1, 2, 3, and 15) to the AND gate were all grounded. The output of the AND, Pin 14, was left open. The output enable $\overline{EN}$ pin (9) was grounded. The power ground pin (8) was grounded and the V_{CC} power pin (16) was connected to V_{CC}. The 4 input pins to the arbiter (4, 5, 6, and 7) were treated as a group with two of the pins always receiving an input from the tester and the other two inputs always connected to V_{CC} through 1KΩ resistors. For any arbiter input pair configuration, there are two output (of the set: Pins 10, 11, 12, and 13) active. These two active output pins are each connected to a grounded 510Ω resistor, a grounded 30pF silvered mica capacitor, and a grounded scope probe (13pF). Thus each active output pin has a load of approximately 500Ω to ground and 50pF to ground (43pF plus 5 to 10pF wiring capacitor). In addition, the active output pin being tested was connected to the input of a comparator (3pF max.). The other input to this comparator was referenced to $1.5V_{DC}$. The $1.5V_{DC}$ reference voltage was not varied with V_{CC}. The two arbiter input signals generated by the tester were negative going pulses, each of the same width (approximately 100ns), which were time shifted relative to each other to produce metastable behavior in the arbiter circuit. This form of input causes only one of the two possibly active outputs to switch low.

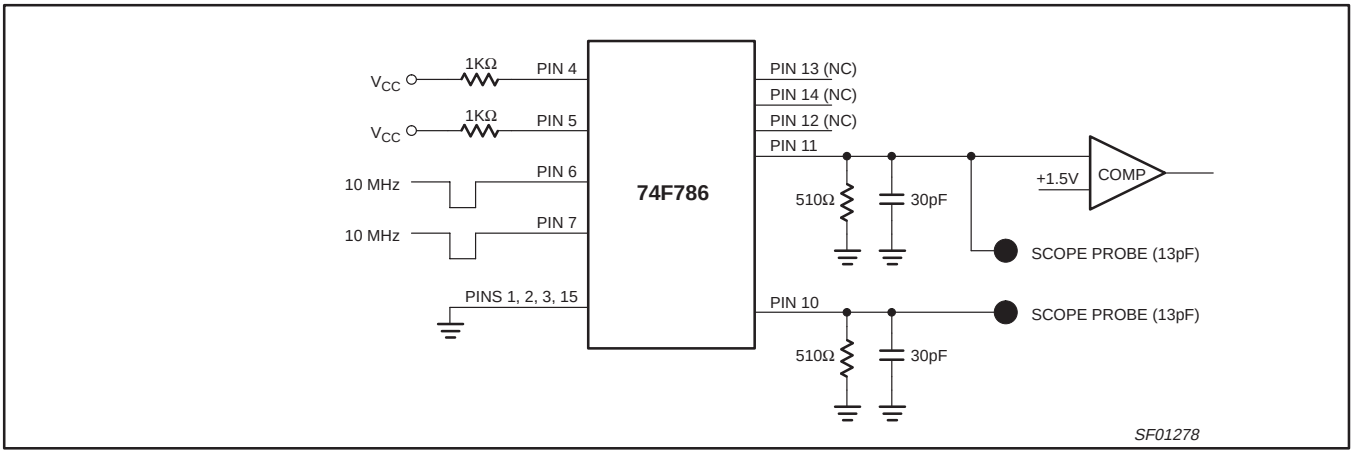

Figure 1. Test Setup for the 74F786

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First Pass Through Packages

The test conditions used for the selection process from the 19 packages is shown in Figure 1 with the results shown in Table 1. The values reported in Table 1 were calculated with t′ (defined later) at 7.60 and 9.93ns. Note that the active inputs are Pins 6 and 7, and the output tested is Pin 11. The last column of this table is the period, after two requests, required to assure that the package would fail to resolve less than once per century. These numbers are based on the assumption that the 2 inputs are not synchronized and both are running at 10MHz (a 100ns clock period). It is assumed that the relative arrival times of the two input signal transitions are uniformly distributed over the clock period. The Mean Time Between Package Unresolved (MTBPU) is then:

$$MTBPU = \{\exp(t'/\tau]/[(T_0)\ (Input1\ rate)\ (Input2\ rate)]$$

where:

t′ = Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ = A function of the rate at which a latch in a metastable state resolves that condition, and

T_0 = A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device. Also one century = 3E9 seconds.

Solving to t′, the resolving time measured from the arrival of the first request, and setting up the equation so the value of T_0 in Table 1 (given in ns) can be substituted directly gives:

$$t' = (\tau)\ 1n\ [(T_0)\ (3E14)]$$

As a result of the first round of tests, three packages were selected for further testing. Package 7 was selected as the fastest, package 11 as the slowest, and package 1 as a typical package.

Second Set of Tests

Using the logic diagram of the 74F786 (Figure 2), it is possible to construct Table 2. Note from Table 2 that thus far, all testing has been conducted on latch 3–4 (Pins 6 and 7). The second set of tests, conducted only on the 3 packages selected from the first set of tests, involved testing each of the 6 latches in the package to select the poorest performing latch in each package. This step also included testing each of the two active output pins for each input condition to select the path with the longest propagation delay.

The results of this comparison testing is shown in Table 3. The results from the table indicate that latches 1–2 and 3–4 have longer propagation delays than the middle four latches. This propagation delay difference is less than 0.4ns. For each of the conditions tested and reported in Table 3, there is a second active pin that could have been used to measure the performance of the latch under test. For package 1 only, the other active pin was tested for each of the latches. The results of this test are shown in Table 4. In theory, the results should be the same except for possible differences in propagation delay. The value of τ should be the same, but the value of T_0 could be different. In all 6 cases, the active pin previously not tested had a shorter propagation delay (function of T_0) than the active pin that was tested.

Table 4 also indicates something else. That is the accuracy with which the data in this report can be interpreted. Note that τ varies as much as 0.05ns, which is within the 0.06ns measurement error range of the test equipment used.

The results of the second set of tests are:

1. The 6 latches in each of the 3 selected packages behaved the same, relative to each other.
2. In all 3 packages, the latch selected is of little importance, therefore, Latch 1–2 was selected at random for further testing.
3. It was reasonable to continue with the 3 selected packages and to restrict further testing to Latch 1–2 and to only record data from Pin 13.

Table 1. Test Results for Inputs on Pins 6 & 7 and Output Measured at Pin 11

$V_{CC} = 5.0V_{DC}$ at room temperature. t′ = 7.60 and 9.93ns

PACKAGE NUMBER	τ (ns)	T_0 (ns)	h (ns)	t′ FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
1	0.44	17E2	6.6	17.8
2	0.44	15E2	6.6	18.0
3	0.39	12E2	6.6	16.6
4	0.46	9E2	6.6	18.5
5	0.44	9E2	6.6	17.7
6	0.40	63E2	6.6	16.9
7	0.39	103E2	6.6	16.6
8	0.46	8E2	6.6	18.6
9	0.44	22E2	6.6	18.1
10	0.45	9E2	6.6	18.4
11	0.45	18E2	6.6	18.5
12	0.45	14E2	6.6	18.3
13	0.45	11E2	6.6	18.3
14	0.45	15E2	6.6	18.2
15	0.45	11E2	6.6	18.2
16	0.43	30E2	6.6	17.6
17	0.44	16E2	6.6	18.0
18	0.39	126E2	6.6	16.9
19	0.43	31E2	6.6	17.8

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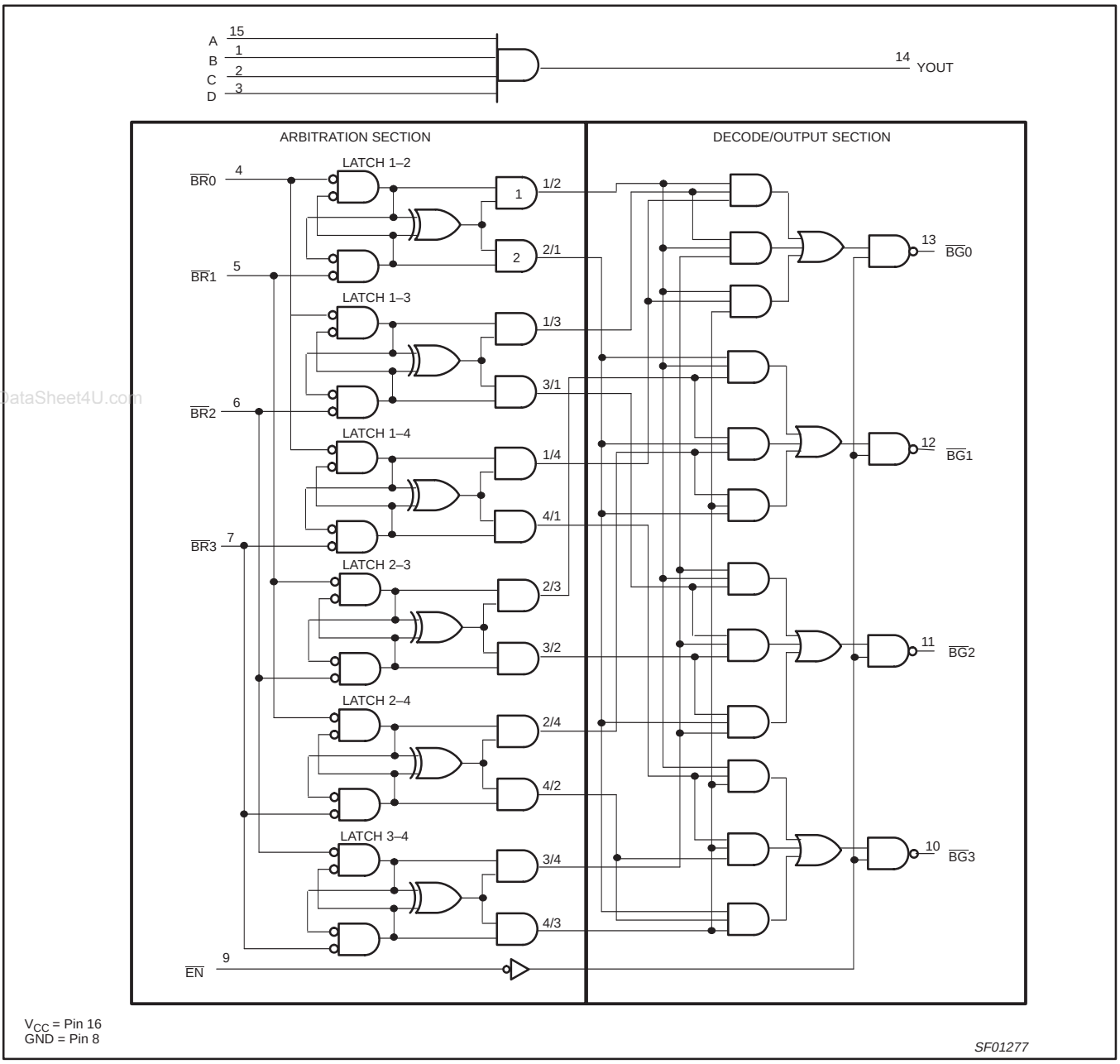

Figure 2. 74F786 Logic Diagram

Table 2. Arbiter Inputs and Corresponding Latches and Output Mapping

INPUT PINS	LATCH UNDER TEST	OUTPUT PINS ACTIVE
4,5	Latch 1–2	13,12 – test pin 13
4,6	Latch 1–3	13,11 – test pin 13
4,7	Latch 1–4	13,10 – test pin 13
5,6	Latch 2–3	12,11 – test pin 12
5,7	Latch 2–4	12,10 – test pin 12
6,7	Latch 3–4	11,10 – test pin 11

Table 3. Test Results for All 6 Latches from Packages 7, 11, and 1

All tests with V_{CC} = 5.0V_{DC} and at room temperature.

PACKAGE NUMBER	LATCH	OUTPUT MEASURED	τ (ns)	T_0 (ns)	h (ns)	t′ FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
7	1–2	13	0.38	175E2	6.6	16.6
7	1–3	13	0.39	79E2	6.6	16.4
7	1–4	13	0.39	69E2	6.6	16.4
7	2–3	12	0.38	109E2	6.6	16.1
7	2–4	12	0.39	68E2	6.6	16.5
7	3–4	11	0.38	181E2	6.6	16.3
11	1–2	13	0.44	34E2	6.6	18.1
11	1–3	13	0.44	17E2	6.6	18.0
11	1–4	13	0.43	26E2	6.6	17.8
11	2–3	12	0.44	16E2	6.6	17.9
11	2–4	12	0.46	8E2	6.6	18.5
11	3–4	11	0.44	29E2	6.6	18.2
1	1–2	13	0.41	56E2	6.6	17.2
1	1–3	13	0.42	24E2	6.6	17.2
1	1–4	13	0.43	17E2	6.6	17.5
1	2–3	12	0.43	18E2	6.6	17.4
1	2–4	12	0.39	72E2	6.6	16.6
1	3–4	11	0.41	49E2	6.6	17.2

Table 4. Test Results for All 6 Latches from Package 1, Measured and/or Computed Different Ways

All tests with V_{CC} = 5.0V_{DC} and at room temperature.

PACKAGE NUMBER	LATCH	OUTPUT MEASURED	τ (ns)	T_0 (ns)	h (ns)	t′ FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
1	1–2	13	0.41	156E2	6.6	17.3
1	1–2	*13	0.39	160E2	6.6	16.8
1	1–2	12	0.36	390E2	6.6	15.8
1	1–3	13	0.42	24E2	6.6	17.2
1	1–3	*13	0.39	101E2	6.6	16.5
1	1–3	11	0.36	137E2	6.6	15.6
1	1–4	13	0.43	17E2	6.6	17.5
1	1–4	*13	0.40	77E2	6.6	16.7
1	1–4	10	0.35	201E2	6.6	15.3
1	2–3	12	0.43	18E2	6.6	17.4
1	2–3	*12	0.40	63E2	6.6	16.7
1	2–3	11	0.37	88E2	6.6	15.5
1	2–4	12	0.39	72E2	6.6	16.6
1	2–4	*12	0.39	79E2	6.6	16.6
1	2–4	10	0.36	96E2	6.6	15.5
1	3–4	11	0.41	49E2	6.6	17.2
1	3–4	*11	0.40	99E2	6.6	16.9
1	3–4	10	0.36	246E2	6.6	15.7

NOTE:

* These values were computed using the subset of sample times used to measure the response from the other active pin in each case.

Temperature and Power Supply Variation Testing

The temperature and power supply variation testing was conducted on packages 1, 7, and 11. These tests were conducted on latch 1–2 only of each package (inputs 4 and 5, results measured at Pin 13). The results are shown in Table 5. The poorest performance was measured again from package 11. The worst case condition was measured at V_{CC} = 4.5V_{DC} and the case temperature at 75°C and is shown in Table 5 as a **bold** entry. this line gives what could be considered the worst case measured performance from the 19 packages tested.

Table 5. Test Results for Latch 1–2 from Packages 7, 11 and 1

All tests with V_{CC} = 4.5V_{DC} – 5.0V_{DC} and temperatures from 0°C to 75°C.

PACKAGE NUMBER	V_{CC}	TEMPERATURE	τ (ns)	T_0 (ns)	h (ns)	t′ FOR 1 FAILURE/CENTURY (INPUTS AT 10E6hz)
7	4.5	3°C	0.37	260E2	6.6	16.3
7	5.5	3°C	0.38	67E2	6.6	15.8
7	4.5	75°C	0.44	70E2	6.6	18.4
7	5.5	75°C	0.43	37E2	6.6	17.7
11	4.5	3°C	0.41	88E2	6.6	17.4
11	5.5	3°C	0.39	64E2	6.6	16.6
11	4.5	Room Temp.	0.42	76E2	6.6	17.9
11	5.5	Room Temp.	0.42	30E2	6.6	17.5
11	4.5	75°C	0.50	15E2	6.6	20.3
11	**4.5**	**75°C**	**0.51**	**8E2**	**6.6**	**20.6**
11	5.5	75°C	0.47	19E2	6.6	19.3
1	4.5	Room Temp.	0.42	93E2	6.6	17.7
1	5.5	Room Temp.	0.42	48E2	6.6	17.1
1	4.5	75°C	0.44	69E2	6.6	18.7
1	5.5	75°C	0.44	37E2	6.6	18.3

NOTES

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Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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