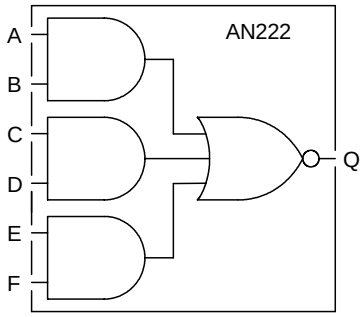
AN222 is an AND/NOR circuit providing the logical function Q = NOT (A.B+C.D+E.F).

Truth Table

A	B	C	D	E	F	Q
L	X	L	X	L	X	H
L	X	L	X	X	L	H
L	X	X	L	X	L	H
L	X	X	L	L	X	H
X	L	L	X	L	X	H
X	L	L	X	X	L	H
X	L	X	L	L	X	H
X	L	X	L	X	L	H
X	X	X	X	H	H	L
X	X	H	H	X	X	L
H	H	X	X	X	X	L



Capacitance

	Ci (pF)
A	0.054
B	0.058
C	0.053
D	0.059
E	0.066
F	0.071

Area

0.95 mils^2

Power

3.72 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.72	2.08	2.80	0.83	2.18	2.86
	tpdaf	0.61	1.55	2.00	0.66	1.56	2.01
Delay B to Q	tpdbr	0.68	2.03	2.77	0.78	2.13	2.86
	tpdbf	0.59	1.53	1.98	0.79	1.66	2.12
Delay C to Q	tpdcr	0.66	2.02	2.79	0.81	2.11	2.82
	tpdcf	0.49	1.43	1.86	0.57	1.44	1.88
Delay D to Q	tpddr	0.64	1.99	2.78	0.77	2.09	2.79
	tpddf	0.47	1.41	1.84	0.69	1.53	1.98
Delay E to Q	tpder	0.46	1.85	2.60	0.74	2.00	2.70
	tpdef	0.33	1.26	1.66	0.39	1.27	1.71
Delay F to Q	tpdfr	0.43	1.83	2.57	0.71	1.97	2.65
	tpdff	0.31	1.25	1.65	0.51	1.36	1.79

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Output Slope A to Q	op_slar	1.61	5.78	7.97	1.73	5.82	7.93
	op_slaf	1.38	4.02	5.30	1.50	4.02	5.38
Output Slope B to Q	op_slbr	1.55	5.90	7.97	1.67	5.77	8.06
	op_slbf	1.38	4.03	5.27	1.65	4.08	5.37
Output Slope C to Q	op_slcr	1.62	5.67	7.93	1.77	5.85	7.90
	op_slcf	1.11	3.75	5.06	1.30	3.80	5.08
Output Slope D to Q	op_sldr	1.56	5.83	7.98	1.72	5.76	7.91
	op_sldf	1.12	3.76	5.07	1.43	3.82	5.12
Output Slope E to Q	op_sler	1.53	5.78	8.01	1.77	5.77	7.86
	op_slef	0.86	3.52	4.87	1.11	3.58	4.91
Output Slope F to Q	op_slfr	1.51	5.83	7.97	1.66	5.68	7.95
	op_slff	0.83	3.53	4.87	1.20	3.68	4.96