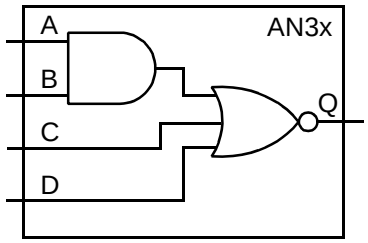
Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.0	1.0	1.0	2.1
D	1.0	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	2.0	TBD	2.5
AN32	4.0	TBD	9.1
AN34	4.0	TBD	8.0
AN36	8.0	TBD	16.6

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.20	0.29 0.25	0.43 0.34	0.58 0.43	0.72 0.52
AN32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.48 0.43	0.59 0.54	0.71 0.68	0.85 0.84	0.96 0.96
AN34	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.40	0.50 0.53	0.61 0.64	0.70 0.75	0.80 0.87
AN36	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.39	0.48 0.49	0.58 0.59	0.67 0.70	0.75 0.82

Delay will vary with input conditions. See page 2-17 for interconnect estimates.