Panasonic

AN34092B

Single-Channel GaN-Tr High-Speed Gate Driver

Features

- Single-Channel High-Speed Gate Driver specialized to driving GaN-Tr.
- Able to drive GaN-Tr easily with a small number of external components
- Integrate constant source current circuitry for turn ON. Source current is adjustable with an external resistor (2.5 mA ~ 25 mA)
- Integrate negative voltage circuitry to avoid erroneous turn ON. Negative voltage is adjustable with an external resistor (– 5.5V ~ – 3V)
- Turn ON / OFF slew rate is controllable with external resistors.
- Integrate active miller clamp function
- Integrate quick gate charging function
- 30 ns typical propagation delay
- Gate clamping function during non supply voltage
- TTL / CMOS compatible inputs
- Support both non-inverting and inverting inputs
- Integrate FAULT function which notifies abnormal condition
- 4.75 V ~ 24 V Supply Range
- Protection : Under Voltage Lockout (UVLO)
  VR Pin Voltage Monitoring Circuitry (VRDET)
  Negative Voltage Monitoring Circuitry (VEEDET)
  Thermal Shutdown (TSD)
- 16 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN type, size 4.0 mm x 4.0 mm, 0.65 mm pitch)

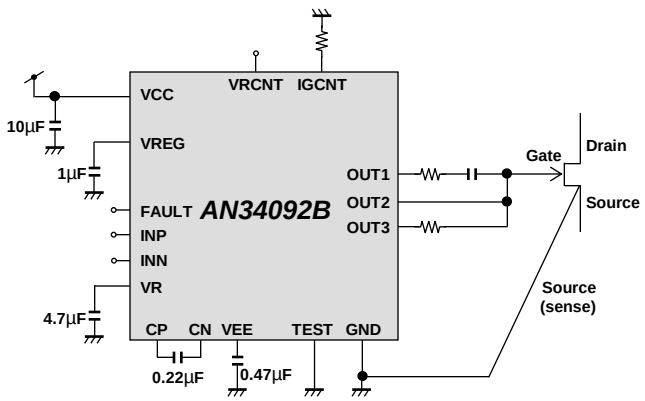
Description

AN34092B is a single-channel high-speed gate driver specialized to driving GaN Power Transistor (GaN-Tr). The IC integrates a sourcing constant current circuitry for turn ON and negative voltage circuitry to avoid erroneous turn on. This allows driving of GaN-Tr easy with a small number of external components. The components between the driver and GaN-Tr are especially less, which allows PCB trace of the driver loop to be short and make PCB design easier.
The sourcing current and negative voltage are configurable with external resistors which allows optimization of the IC according to applications. The IC also integrates the function to quickly charge gate and turn ON at high slew rate. This function maximizes GaN-Tr's high-speed response characteristics.
Slew rate can be adjusted with external resistors for both turn ON and OFF.

Applications

- Gate Driver for Panasonic GaN-Tr
- Switching Power Supplies
- Motor Drives
- Power Conditioner

Typical Application Diagrams



Note : The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
AN34092B-VB	GaN-Tr Gate Driver	16 pin HQFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	V_{CC}	28	V	*1
Operating Free-Air Temperature	T_{opr}	– 40 to + 125	°C	*2
Operating Junction Temperature	T_j	– 40 to + 150	°C	*2
Storage Temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	V_{VRCNT}, V_{IGCNT}, V_{TEST}	– 0.3 to (V_{VREG} + 0.3)	V	*1 *3
	V_{INP}, V_{INN}	– 0.3 to (V_{CC} + 0.3)	V	*5
Output Voltage Range	V_{OUT1}, V_{OUT2}, V_{OUT3}	– 6.0 to (V_{CC} + 0.3)	V	*1 *4
	V_{FAULT}	– 0.3 to (V_{CC} + 0.3)	V	*1 *4
Input Current Range	I_{FAULT}	– 0.3 to 10	mA	*1
Output Current Range	I_{OUT1}	– 1.5 to 6.0	A	*1
	I_{OUT2}	– 6.0 to 2.0	A	*1
	I_{OUT3}	– 3.0 to 0.3	A	*1
ESD	HBM	2	kV	—

Notes : This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
Do not apply external currents and voltages to any pin not specifically mentioned.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25 °C.

*3 :(V_{REG} + 0.3) V must not exceed 6 V.

*4 : (V_{CC} + 0.3) V must not exceed 28 V.

*5 : (V_{CC} + 0.3) V must not exceed 24 V.

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POWER DISSIPATION RATING

Package	$\theta_{j\text{-}a}$	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Note
16 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	62.3 °C / W	2.008 W	1.044 W	*1

Notes : For the actual usage, please follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1:Glass Epoxy Substrate (4 Layers) [50 × 50 × 0.8 t (mm)], heat spreader soldered

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage Range	V_{CC}	4.75	12	24	V	—
Input Voltage Range	V_{VRCNT}	– 0.3	—	V_{VREG} + 0.3	V	*1
	V_{IGCNT}	– 0.3	—	V_{VREG} + 0.3	V	*1
	V_{TEST}	– 0.3	—	V_{VREG} + 0.3	V	*1
	V_{INP}	– 0.3	—	V_{CC} + 0.3	V	*3
	V_{INN}	– 0.3	—	V_{CC} + 0.3	V	*3
Output Voltage Range	V_{OUT1}	– 6.0	—	V_{CC} + 0.3	V	*2
	V_{OUT2}	– 6.0	—	10	V	—
	V_{OUT3}	– 6.0	—	10	V	—
	V_{FAULT}	– 0.3	—	V_{CC} + 0.3	V	*2
Input Current Range	I_{FAULT}	– 0.3	—	10	mA	—
Output Current Range	I_{OUT1}	– 1.5	—	6.0	A	—
	I_{OUT2}	– 6.0	—	2.0	A	—
	I_{OUT3}	– 3.0	—	0.3	A	—

Notes : Voltage values, unless otherwise specified, are with respect to GND.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (V_{REG} + 0.3) V must not exceed 6 V.
*2 : (V_{CC} + 0.3) V must not exceed 28 V.
*3 : (V_{CC} + 0.3) V must not exceed 24 V.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, VRCNT = OPEN (V_{VR} = 5 V , V_{VEE} = – 5 V)
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Standby Current	I_{STB}	V_{INP} = V_{INN} = 0 V	—	1.6	2.2	mA	—
Active Current	I_{ATV}	V_{INP} = 0 V ↔ 5 V @ 50 kHz, Duty 50% V_{INN} = 0 V OUT1 = 1 nF OUT2 = OUT3 = 1 nF IGCNT = 39 kΩ	—	5.5	—	mA	*1
Logic Pin Characteristics							
INP Pin Low-Level Input Voltage	V_{INPL}	—	—	—	0.9	V	—
INP Pin High-Level Input Voltage	V_{INPH}	—	2.7	—	—	V	—
INP Pin Input Voltage Hysteresis	ΔV_{INP}	—	—	1.2	—	V	*1
INP Pin Input Current	I_{IPTINP}	V_{INP} = 12 V	—	900	1200	µA	—
INN Pin Low-Level Input Voltage	V_{INNL}	—	—	—	0.9	V	—
INN Pin High-Level Input Voltage	V_{INNH}	—	2.7	—	—	V	—
INN Pin Input Voltage Hysteresis	ΔV_{INN}	—	—	1.2	—	V	*1
INN Pin Input Current	I_{IPTINN}	V_{INN} = 12 V	—	900	1200	µA	—
Internal Regulator Characteristics							
VREG Output Voltage	V_{REGO}	V_{INP} = V_{INN} = 0 V	—	5	—	V	*1
VR Output Voltage 1	V_{RO1}	V_{INP} = V_{INN} = 0 V VRCNT = OPEN	—	5	—	V	*1
VR Output Voltage 2	V_{RO2}	V_{INP} = V_{INN} = 0 V VRCNT = 12 kΩ	—	5	—	V	*1
VEE Output Voltage 1	V_{EEO1}	V_{INP} = V_{INN} = 0 V VRCNT = OPEN I_{VEE} = 1 mA CP-CN Capacitor = 0.22µF	– 5.3	– 5	– 4.7	V	—
VEE Output Voltage 2	V_{EEO2}	V_{INP} = V_{INN} = 0 V VRCNT = 12 kΩ I_{VEE} = 1 mA CP-CN Capacitor = 0.22µF	– 5.2	– 5	– 4.8	V	—
Under Voltage Lockout (UVLO)							
UVLO Detect Voltage	V_{UVLODE}	V_{CC} = 5 V → 0 V	4.38	4.50	4.59	V	—
UVLO Release Voltage	V_{UVLORE}	V_{CC} = 0 V → 5 V	4.52	4.65	4.74	V	—
UVLO Hysteresis	ΔV_{UVLO}	—	100	150	200	mV	—

Note : *1 : Typical design value

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 12 V, VRCNT = OPEN (V_{VR} = 5 V , V_{VEE} = – 5 V)
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Gate Driver Characteristics (DC)							
OUT1 Pin Pull-up Resistance	R_{ON1U}	V_{INP} = 5 V V_{INN} = 0 V I_{OUT1} = 100 mA	—	0.8	1.2	Ω	—
OUT1 Pin Pull-down Resistance	R_{ON1D}	V_{INP} = V_{INN} = 0 V V_{VEE} = – 5 V I_{OUT1} = 100 mA	—	2.1	2.6	Ω	—
OUT2 Pin Output Source Current	I_{OUT2O}	V_{INP} = 5 V V_{INN} = 0 V V_{OUT2} = 4.2 V IGCNT = 39 kΩ	9	10	11	mA	—
OUT2 Pin Negative Voltage Pull-down Resistance	R_{ON2DN}	V_{INP} = V_{INN} = 0 V V_{VEE} = – 5 V I_{OUT2} = 100 mA	—	0.5	0.75	Ω	—
OUT2 Pin GND Pull-down Resistance	R_{ON2DG}	V_{INP} = V_{INN} = 0 V I_{OUT2} = 1 mA	—	200	300	Ω	—
OUT2 Pin Clamp Voltage	$V_{CLMPOUT2}$	V_{CC} = OPEN I_{OUT2} = 10 µA	—	0.7	1.0	V	—
OUT3 Pin Negative Voltage Pull-down Resistance	R_{ON3DN}	V_{INP} = V_{INN} = 0 V V_{VEE} = – 5 V I_{OUT3} = 100 mA	—	1	1.5	Ω	—

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 12 V, VRCNT = OPEN (V_{VR} = 5 V , V_{VEE} = – 5 V)
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Gate Driver Characteristics (AC)							
INP Pin Propagation Delay 1	$T_{DLYHINP}$	OUT1 = 1 nF V_{INP} = 0 V → 5 V @ 10 ns V_{INN} = 0 V V_{INP} = 90 % → V_{OUT1} = 10 %	24	32	48	ns	—
INP Pin Propagation Delay 2	$T_{DLYLINP}$	OUT3 = 1 nF VRCNT = OPEN V_{INP} = 5 V → 0 V @ 10 ns V_{INN} = 0 V V_{INP} = 10 % → V_{OUT3} = 90 %	23	30	45	ns	—
INN Pin Propagation Delay 1	$T_{DLYHINN}$	OUT1 = 1 nF V_{INN} = 5 V → 0 V @ 10 ns V_{INP} = 5 V V_{INN} = 10 % → V_{OUT1} = 10 %	28	36	52	ns	—
INN Pin Propagation Delay 2	$T_{DLYLINN}$	OUT3 = 1 nF VRCNT = OPEN V_{INN} = 0 V → 5 V @ 10 ns V_{INP} = 5 V V_{INN} = 90 % → V_{OUT3} = 90 %	20	27	42	ns	—
Output Rise Time	T_{RISE}	OUT1 = 1 nF V_{INP} = 0 V → 5 V V_{INN} = 0 V V_{OUT1} = 10 % → 90 %	—	7	—	ns	*1
Output Fall Time	T_{FALL}	OUT3 = 1 nF V_{INP} = 5 V → 0 V V_{INN} = 0 V V_{OUT3} = 90 % → 10 %	—	5	—	ns	*1
OUT1 Pin Peak Source Current	I_{SCPKO1}	OUT1 = 330 pF + 3.3 Ω V_{OUT1} = – 5 V → V_{CC}	—	1.0	—	A	*1
OUT3 Pin Peak Sink Current	I_{SNPKO3}	OUT3 = 470 pF + 1 Ω V_{OUT3} = 4 V → – 5 V	—	1.3	—	A	*1

Note : *1 : Typical design value

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 12 V, VRCNT = OPEN (V_{VR} = 5 V , V_{VEE} = – 5 V)
T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Active Miller Clamp Function							
Active Miller Clamp Threshold	V_{AMC}	—	—	0	—	V	*1
FAULT Function							
FAULT Pin Pull-down Resistance	R_{FLT}	—	—	1	1.5	kΩ	—
Thermal Shutdown (TSD)							
TSD Threshold	T_{TSDTH}	—	—	150	—	°C	*1
TSD Hysteresis	T_{TSDHYS}	—	—	30	—	°C	*1
VR Pin Voltage Monitoring Function (VRDET)							
VRDET Detect Voltage	V_{VRDE}	—	—	75	—	%	*1
VRDET Release Voltage	V_{VRRE}	—	—	85	—	%	*1
VRDET Hysteresis	ΔV_{VR}	—	—	10	—	%	*1
Negative Voltage Monitoring Function (VEEDET)							
VEEDET Detect Voltage	V_{VEEDE}	—	—	60	—	%	*1
VEEDET Release Voltage	V_{VEERE}	—	—	70	—	%	*1
VEEDET Hysteresis	ΔV_{VEE}	—	—	10	—	%	*1

Note : *1 : Typical design value

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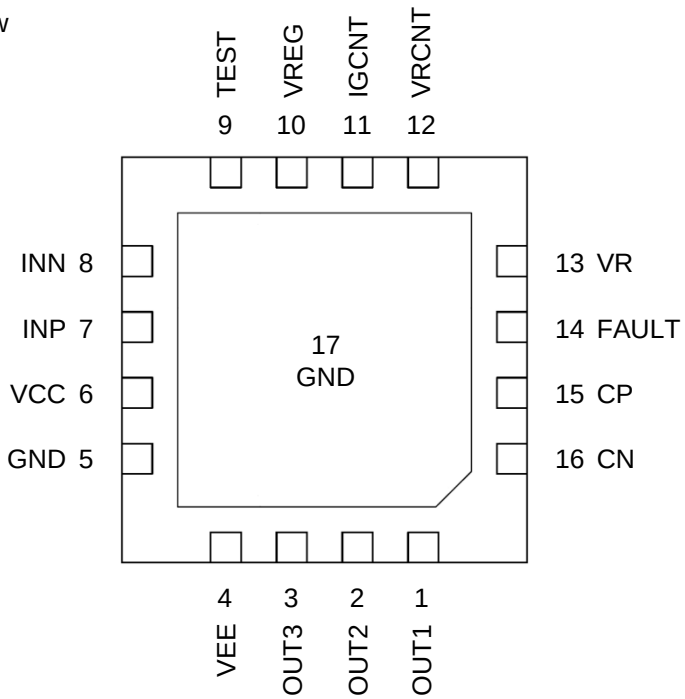
PIN CONFIGURATION

Bottom View



PIN FUNCTIONS

Pin No.	Pin Name	Type	Description
1	OUT1	Output	Quick Gate Charge and Speed-up Capacitor Discharging Output During ON period of GaN-Tr, a power MOSFET switch between VCC and OUT1 turns ON and this pin swings up to Vcc level. By connecting a resistor and a speed-up capacitor between this pin and gate of GaN-Tr, fast turn ON of GaN-Tr is achieved. During OFF period, this pin pulls down to V_{VEE} and discharges the speed-up capacitor. Make PCB trace as short as possible to minimize effect of parasitic elements.
2	OUT2	Output	Sourcing Gate Current and Active Miller Clamp Output During ON period of GaN-Tr, this pin outputs sourcing constant current and maintains ON of GaN-Tr. During OFF period, this pin functions as active miller clamp output and pulls down to V_{VEE} when this pin falls below a certain threshold voltage. Connect to gate of GaN-Tr. Make PCB trace as short as possible to minimize effect of parasitic elements.
3	OUT3	Output	Gate Pull-down Output This pin is pulled down to V_{VEE} during OFF period of GaN-Tr. By connecting a resistor between this pin and gate of GaN-Tr, turn OFF slew rate can be adjusted. Make PCB trace as short as possible to minimize effect of parasitic elements.
4	VEE	Output	Negative Voltage Output Output of an inverting charge pump. This pin outputs $-V_{VR}$. Bypass a capacitor from this pin to ground.

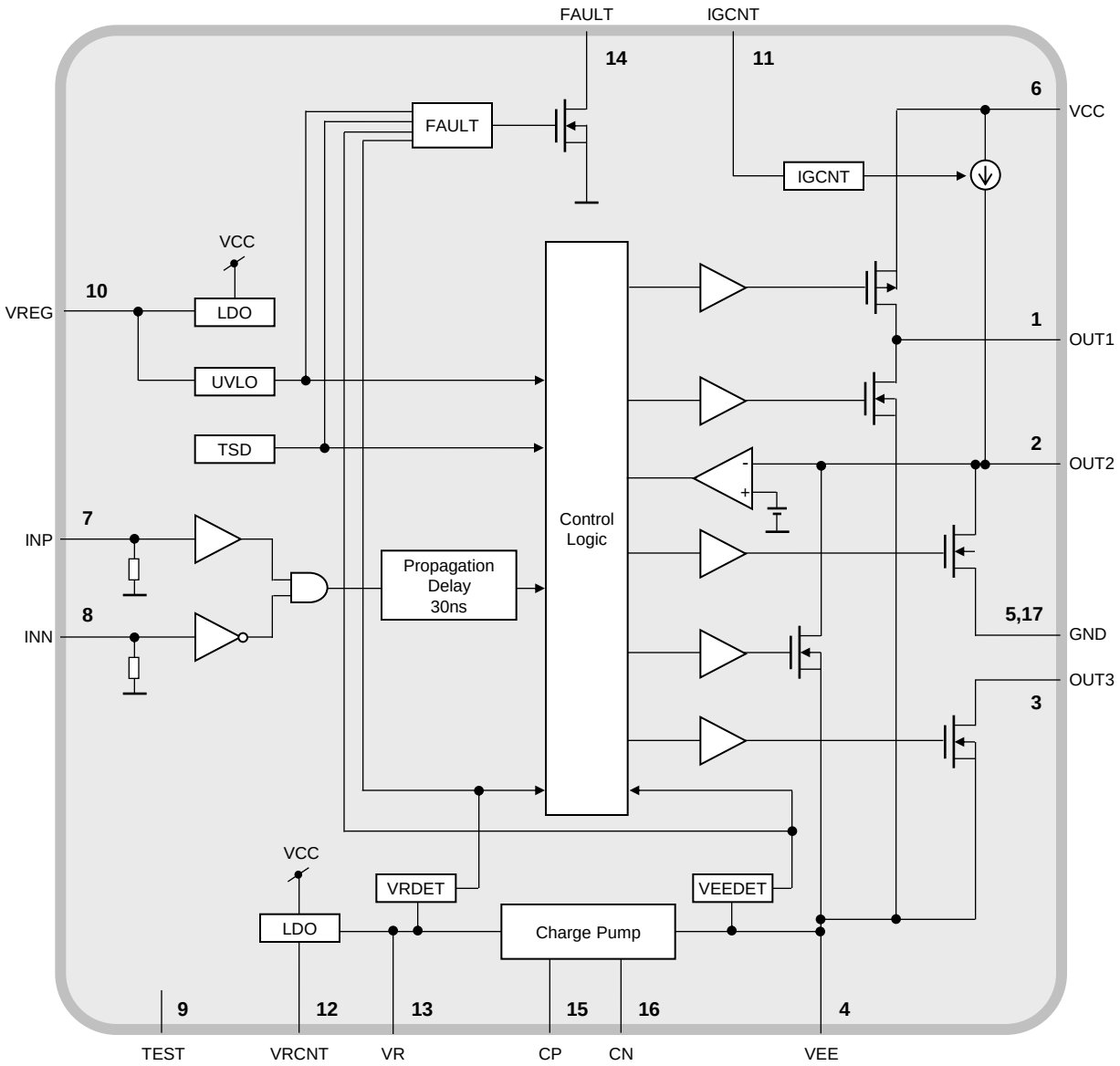
Note : Detailed pin descriptions are provided in the OPERATION section.

PIN FUNCTIONS (Continued)

Pin No.	Pin Name	Type	Description
5	GND	Ground	GND pin
6	VCC	Power Supply	Main Supply Input Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
7	INP	Input	Gate Drive Logic Input (non-inverting input) By a logic input to this pin, gate of GaN-Tr is driven. High input turns ON GaN-Tr, low input turns OFF GaN-Tr.
8	INN	Input	Gate Drive Logic Input (inverting input) By a logic input to this pin, gate of GaN-Tr is driven. High input turns OFF GaN-Tr, low input turns ON GaN-Tr.
9	TEST	Input	Test Pin Connect to ground.
10	VREG	Output	LDO Regulator Output This output pin powers the internal control circuitry. Bypass a capacitor from this pin to GND.
11	IGCNT	Input	OUT2 Sourcing Current Control Pin By connecting a resistor from this pin to ground, sourcing current supplied to GaN-Tr gate during ON period can be adjusted.
12	VRCNT	Input	VR and Negative Voltage Control Pin By connecting a resistor from this pin to ground, VR output voltage and negative voltage (V_{VEE}) can be adjusted. When the pin is OPEN, VR output voltage is set at 5V and V_{VEE} is set at –5V.
13	VR	Output	LDO Regulator Output This pin is output of a reference linear regulator for an inverting charge pump. Bypass a capacitor from this pin to GND.
14	FAULT	Output	FAULT Indicator Pin This pin is Nch MOSFET open-drain output which is pulled to ground when abnormal operation is detected. By connecting a resistor from this pin to supply voltage, the pin can be used as logic low output during fault condition. This pin can also drive photo-coupler directly by the connection via a resistor.
15	CP	Output	Charge Pump Capacitor Connection Pin This pin is to connect a capacitor for an inverting charge pump. This pin switches between V_{VR} and GND. Connect a capacitor from this pin to CN.
16	CN	Output	Charge Pump Capacitor Connection Pin This pin is to connect a capacitor for an inverting charge pump. This pin switches between V_{VEE} and GND. Connect a capacitor from this pin to CP.
17	GND	Ground	GND Pin for Heat Radiation Connect to GND(pin 5)

Note : Detailed pin descriptions are provided in the OPERATION section.

FUNCTIONAL BLOCK DIAGRAM



Note : This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Startup Sequence

The following figure shows startup sequence of the IC.

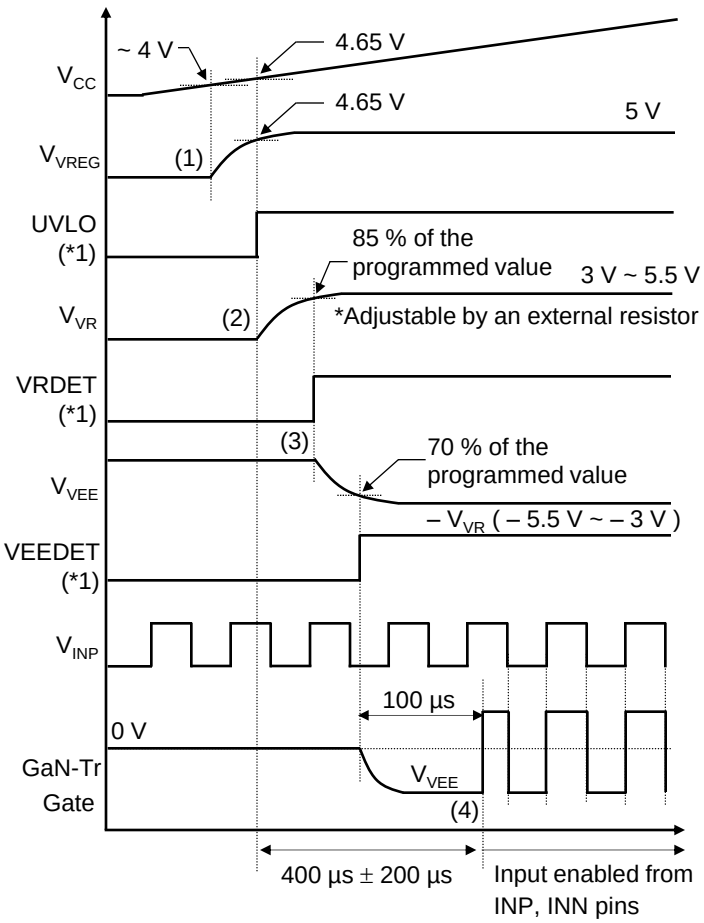


Figure : Startup Sequence (*1 : internal signal)

(1) When V_{CC} is above 4 V, an internal LDO regulator (VREG) powers up.

(2) When V_{VREG} is above 4.65 V, UVLO is released and a reference LDO regulator for an inverting charge pump (VR) powers up.
V_{VR} is adjustable from 3 V ~ 5.5 V by a resistor from the VRCNT pin to ground.

(3) When V_{VR} rises above 85 % of the programmed value, the inverting charge pump starts its operation and negative voltage – V_{VR} appears at the VEE pin.

(4) The gate control of the INP, INN pins get activated 100 µs after V_{VEE} drops below 70 % of the programmed value. The time from UVLO release to activation of gate control is 400 µs ± 200 µs.

2. Protection

(1) Under Voltage Lockout (UVLO)
When voltage of the VREG pin (V_{VREG}) falls below 4.5 V, UVLO is detected. Then gate of GaN-Tr is pulled down and simultaneously, an inverting charge pump and the reference LDO regulator (VR) shut off. Once V_{VREG} rises above 4.65 V, UVLO is released.

(2) VR Pin Voltage Monitoring Circuitry (VRDET)
When voltage of the VR pin (V_{VR}) falls below 75 % of the programmed value, VRDET is detected. Then gate of GaN-Tr is pulled down and simultaneously, an inverting charge pump shuts off. Once V_{VREG} rises above 85 % of the programmed value, VRDET is released.

(3) Negative Voltage Monitoring Circuitry (VEEDET)
When voltage of the VEE pin (V_{VEE}) rises above 60 % of the programmed value, VEEDET is detected and gate of GaN-Tr is pulled down. Once V_{VEE} falls below 70 % of the programmed value, VEEDET is released.

(4) Thermal Shutdown (TSD)
TSD is detected once the internal temperature of the IC is above 150 °C. Then gate of GaN-Tr is pulled down and simultaneously, an inverting charge pump and the reference LDO regulator (VR) shut off. Once the internal temperature cools down below 120 °C, TSD is released.

The above protections (1) ~ (4) are all auto recovery, which means the IC recovers to normal operation automatically once abnormal operation is released. Also, if any of the above protection is activated, the FAULT pin gets pulled down. As shown in figure (A), by pulling up to supply voltage through a resistor, the pin can be used to output low during abnormal operation. Or the pin can drive photo-coupler by connecting like figure (B). For resistors shown in below figures, please select resistance that limits input current to the FAULT pin below 10 mA.

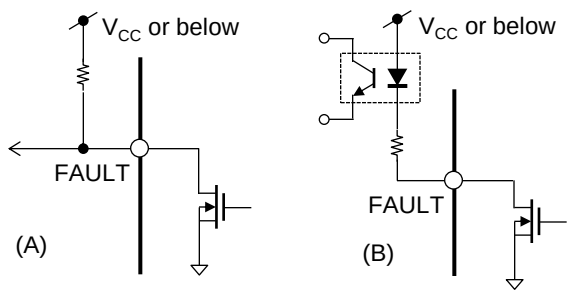


Figure : FAULT Function

OPERATION (continued)

3. Gate Control Function

(1) Control Between Driver and GaN-Tr

Gate control waveform and a schematic of the IC is shown below. (example is for operation using the INP pin)

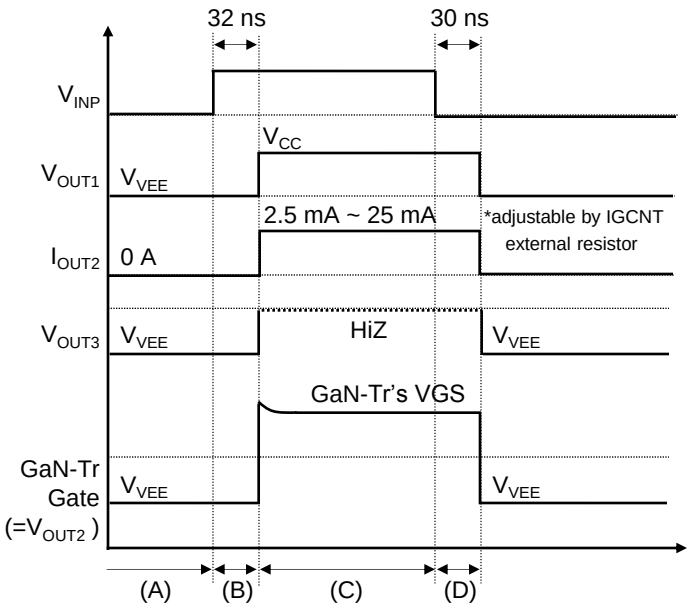


Figure : Gate Control Waveform

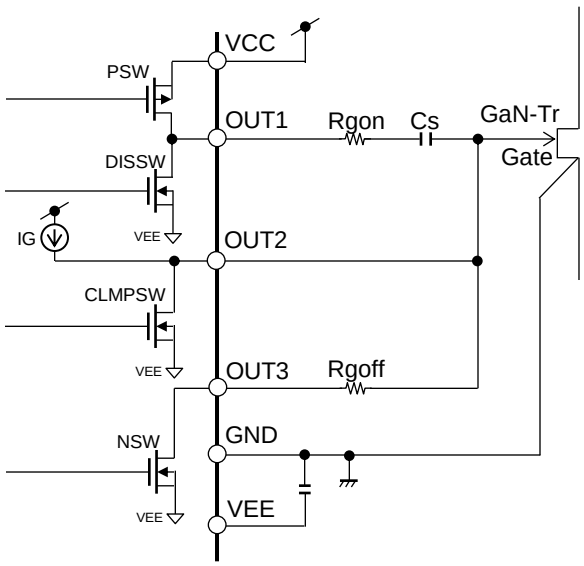


Figure : Gate Control Schematic

The IC drives GaN-Tr by repeating the operation (A) ~ (D) shown in left figure. The detail explanation of (A) ~ (D) is described below:

(A) V_{INP} = Low
NSW and CLMPSW turn ON and gate is pulled down to V_{VEE}. At the moment, DISSW also turns ON and discharges a speed-up capacitor, Cs.

(B) 32 ns Interval After V_{INP} = Low → High
Operation (A) is kept during the rising propagation delay of 32 ns.

(C) V_{INP} = High
NSW, CLMPSW, and DISSW turn OFF and PSW turns ON. By the turn ON, V_{OUT1} = V_{VEE} → V_{CC} and gate is quickly charged through Cs, which turns ON GaN-Tr.
At the same time, the current source IG turns ON and maintains ON of GaN-Tr. During ON state, gate voltage is clamped at VGS of GaN-Tr.

(D) 30 ns Interval After V_{INP} = High → Low
Operation (C) is kept during the falling propagation delay of 30 ns.
After 30 ns, PSW and IG turn OFF, NSW, CLMPSW, DISSW turn ON and operation goes back to (A). At the moment, by the active miller clamp function, CLMPSW turns ON after NSW by some delay.

OPERATION (continued)

3. Gate Control Function (continued)

(2) Active Miller Clamp Function

The IC can achieve both turn OFF slew rate control and prevention of erroneous turn ON by the active miller clamp function.
As shown in below figure, when turning OFF GaN-Tr, OUT3 pin is pulled down by NSW first. At this moment, by an external resistor, Rgoff, at the OUT3 pin, turn OFF slew rate can be adjusted (A).
When gate voltage (=OUT2 pin voltage) falls below 0 V, CLMPSW at the OUT2 pin turns ON and gate gets pulled down without passing through Rgoff. A typical on-resistance of CLMPSW is 0.5 Ω so erroneous turn ON can be prevented (B).

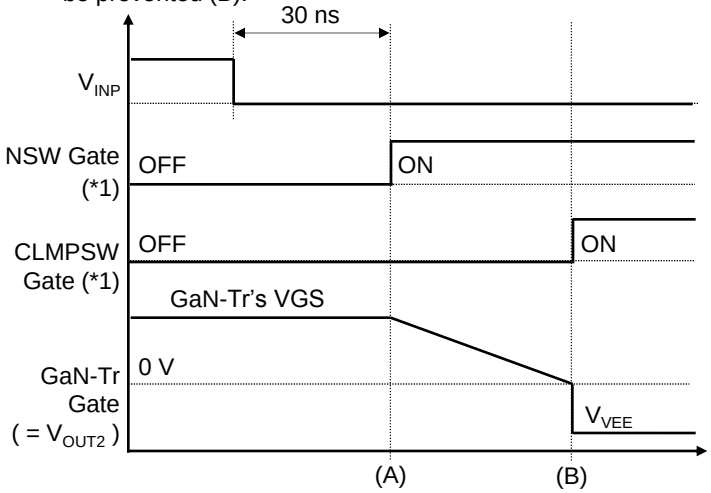


Figure : Waveform During Turn OFF (*1 : internal signal)

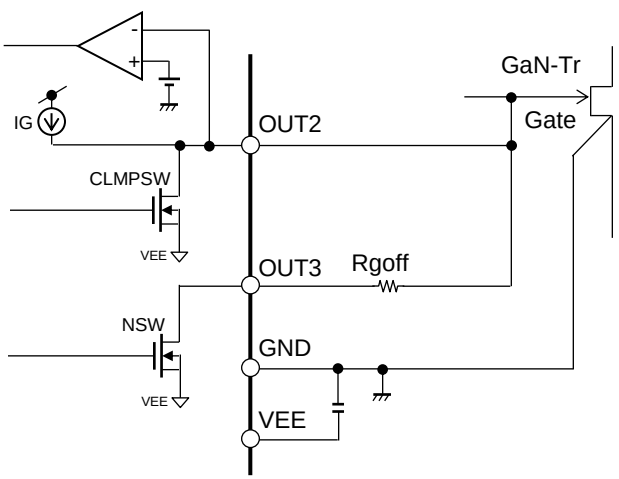


Figure : Gate Control Circuit
(Extrapolated circuits related to turn OFF)

(3) Quick Gate Charge Function

By connecting a capacitor between the OUT1 pin and gate of GaN-Tr, the IC can quickly charge gate during ON and achieves turn ON of GaN-Tr at high slew rate.
As shown in bottom figure, when turning ON GaN-Tr, PSW turns ON, and OUT1 voltage changes from $V_{VEE} \rightarrow V_{CC}$. This voltage difference is imposed to the speed-up capacitor, Cs, and delivers large instantaneous charging current to gate of GaN-Tr which allows quick charge of gate.

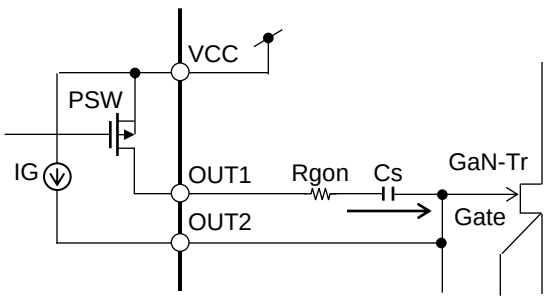


Figure : Gate Control Circuit
(Extrapolated circuits related to turn ON)

Established : 2016-06-23
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OPERATION (continued)

3. Gate Control Function (continued)

(4) Gate Control by INP, INN Pins

The IC features two input pins, INP and INN pins, implementing both non-inverting (INP pin) and inverting (INN pin) configuration. If the IC is used in non-inverting configuration, set INN low and use INP as an input pin. If the IC is used in inverting configuration, set INP high and use INN as an input pin.
Below is the truth table of the input pins, as well as the control of output pins (OUT1, OUT2, OUT3) by protection functions.

Input			Output			GaN-Tr
Protection	INP	INN	OUT1	OUT2	OUT3	
Non-detect	Low	X	V_{VEE}	V_{VEE}	V_{VEE}	OFF
Non-detect	X	High	V_{VEE}	V_{VEE}	V_{VEE}	OFF
Non-detect	High	Low	V_{CC}	Constant current	OPEN	ON
Detect	X	X	OPEN	0 V	OPEN	OFF

X = High or Low
Protection : UVLO, VRDET, VEEDET, TSD

Table : Truth Table of Output Pins Control

Internal circuit of the input pin is shown below:

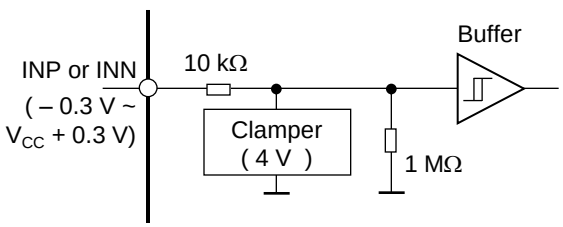

Figure : Internal Circuit of the Input Pin

The INP, INN pins are connected to clamper circuit (4 V) through 10 kΩ resistor internally, so the current equals to voltage difference between forced voltage at input and 4 V divided by 10 kΩ flows into the pins.
The buffer at input is a hysteresis buffer with high threshold = 2.4 V, low threshold = 1.2 V, hysteresis = 1.2 V which offers improvement of noise immunity. These thresholds are independent of V_{CC} and take almost constant values.

(5) Adjustment of Gate Current by IGCNT Pin

Amount of constant current supplied from the OUT2 pin to gate of GaN-Tr during turn ON is proportional to the current at IGCNT pin.
IGCNT pin outputs typical voltage of 1.25 V which allows adjustment of gate constant current by connecting a pull-down resistor to IGCNT pin. The table shows typical values of gate current (I_G) and pull-down resistor (R_{IGCNT}).

I_G	R_{IGCNT}
2.5 mA	180 kΩ
5.5 mA	82 kΩ
10 mA	39 kΩ
15 mA	18 kΩ
20 mA	9.1 kΩ
25 mA	2.7 kΩ

Table : I_G vs R_{IGCNT}

R_{IGCNT} can be calculated as:

$$I_G[mA] = \frac{668}{R_{IGCNT} + 22.6[k\Omega]} - 0.83$$

$$R_{IGCNT}[k\Omega] = \frac{668}{I_G[mA] + 0.83} - 22.6[k\Omega]$$

The relationship of R_{IGCNT} to I_G is shown in next figure.
Adjustable range of I_G is 2.5 mA ~ 25 mA.

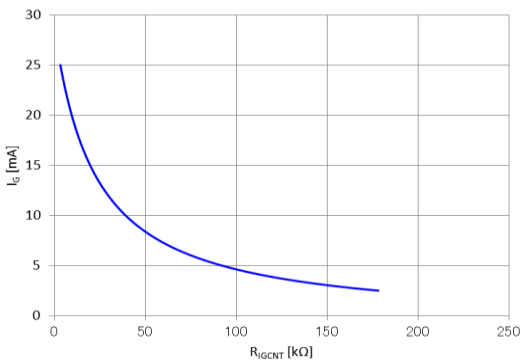

Figure : Relationship Between I_G and R_{IGCNT}

Recommended I_G settings for Panasonic GaN-Tr are shown below:

GaN-Tr Part Number	I_G	R_{IGCNT}
PGA26E19BA	5.5 mA	82 kΩ
PGA26E07BA	10 mA	39 kΩ

Table : Recommended I_G settings for GaN-Tr

Established : 2016-06-23
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OPERATION (continued)

3. Gate Control Function (continued)

(6) Adjustment of Negative Voltage by VRCNT Pin

Threshold level of GaN-Tr is generally low voltage of about 1 V, so during OFF period, GaN-Tr may erroneously turn ON from high dVDS/dt. However, the IC is immune to erroneous turn ON because the IC pulls down gate of GaN-Tr to negative voltage with low impedance during OFF period.
Negative voltage is proportional to the current at VRCNT pin. VRCNT pin outputs typical voltage of 1.25 V which allows adjustment of negative voltage by connecting a pull-down resistor at VRCNT pin.
Adjustable range of V_{VEE} is – 5.5 V ~ – 3 V. The table shows typical values of negative voltage (V_{VEE}) and pull-down resistor (R_{VRCNT}).

V_{EE}	R_{VRCNT}
– 3 V	56 kΩ
– 4 V	27 kΩ
– 5 V	12 kΩ or OPEN
– 5.5 V	5.6 kΩ

Table : V_{VEE} vs R_{VRCNT}

R_{VRCNT} can be calculated as:

$$V_{VEE}[V] = -\frac{363}{R_{VRCNT} + 57.1[k\Omega]} + 0.2$$

$$R_{VRCNT}[k\Omega] = -\frac{363}{V_{VEE}[V] - 0.2} - 57.1[k\Omega]$$

The relationship of R_{VRCNT} to V_{VEE} is shown in next figure.
If VRCNT pin is left open, V_{VEE} is – 5 V.

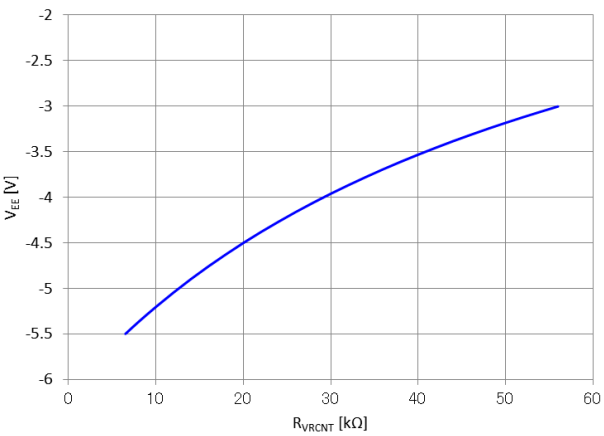

Figure : Relationship between V_{VEE} and R_{VRCNT}

(7) Gate Clamp Function During No Power Supply

The IC can clamp gate voltage of GaN-Tr to less than certain voltage even when no power supply is connected to the VCC pin. When voltage is applied between source and drain of GaN-Tr, gate leak current appears but due to this gate clamp function, rising of gate voltage from leak current can be suppressed and can maintain off state.
Clamping is done by the OUT2 pin and the clamping voltage is 0.7 V (at 10 µA leak current).

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
13. Verify the risks which might be caused by the malfunctions of external components.
14. Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

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