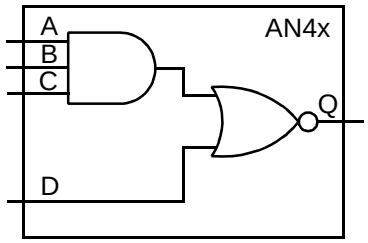
Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.0	1.0	1.0	2.1
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	2.0	TBD	2.7
AN42	4.0	TBD	7.6
AN44	4.0	TBD	7.8
AN46	8.0	TBD	15.5

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.15 0.21	0.22 0.29	0.33 0.42	0.44 0.56	0.54 0.69
AN42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.50	0.51 0.61	0.63 0.74	0.77 0.88	0.88 0.99
AN44	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.47	0.52 0.61	0.63 0.72	0.73 0.83	0.83 0.94
AN46	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.51	0.49 0.60	0.60 0.69	0.70 0.80	0.79 0.92

Delay will vary with input conditions. See page 2-17 for interconnect estimates.