Panasonic

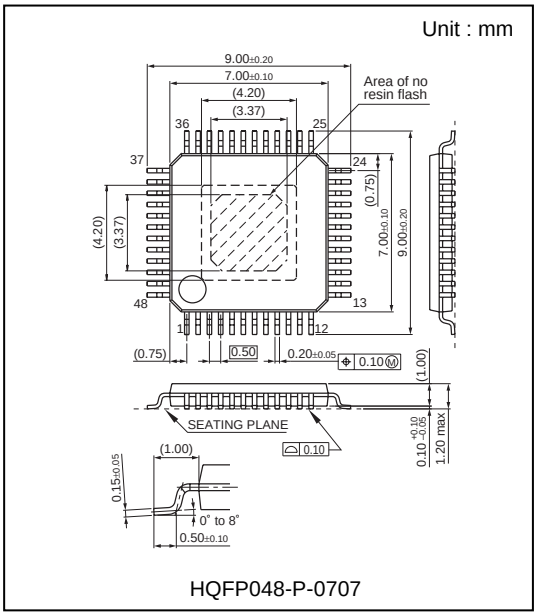
Product News

Achieving a 1-chip motor drive.

Optical Disc Motor Drive IC AN41204A

■ Overview

The AN41204A optical disc motor drive IC incorporates a 1-channel 3-phase full-wave PWM motor driver featuring low vibration and noise as well as a 5-channel PWM output driver for linear input. Integrating a spindle driver and channel driver on a single chip and using small, thin packaging reduces the mounting area. This helps to develop equipment that is more compact, slim and lightweight.



HQFP048-P-0707

■ Feature

- All-channel PWM driving power consumption is among the lowest of its kind.
- Low-vibration and low-noise sinewave PWM is used to drive the spindle section.
- Dead zone-less PWM driving for focus, tracking and tilt.
- Stepper motor drivers on two channels.
- Built-in thermal shutdown function.
- Compact, slim package.

■ Applications

Slim DVD recording units (RAM/+RW/-RW), optical disc units such as slim combination drives and car navigation systems.

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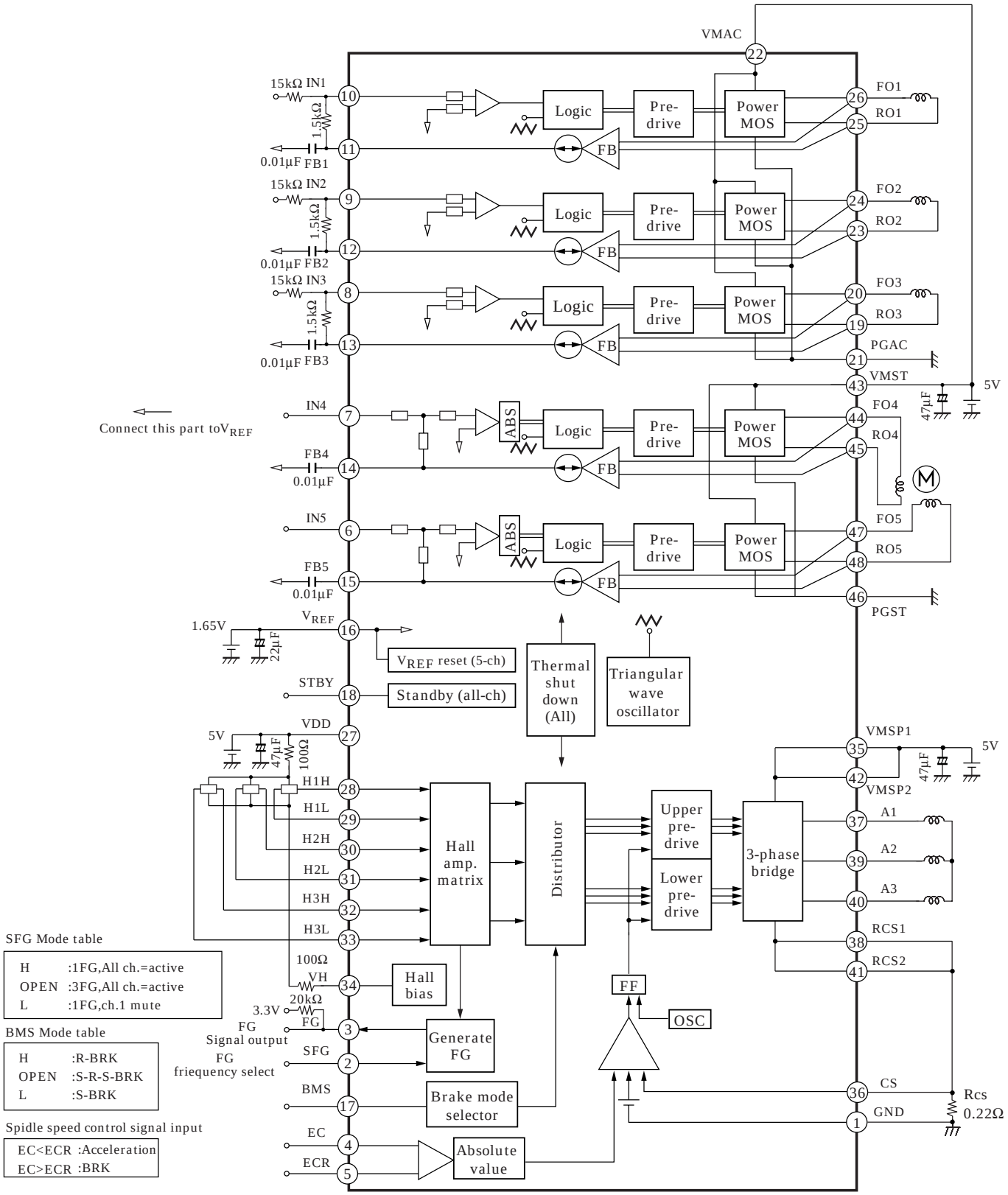
■ Block Diagram



SFG Mode table

H	:1FG,All ch.=active
OPEN	:3FG,All ch.=active
L	:1FG,ch.1 mute

BMS Mode table

H	:R-BRK
OPEN	:S-R-S-BRK
L	:S-BRK

Spidle speed control signal input

EC<ECR	:Acceleration
EC>ECR	:BRK

■ Pin Descriptions

No	Symbol	Description	No	Symbol	Description
1	GND	Control circuit GND	25	RO1	Ch.1 inverted output
2	SFG	SP FG mode select input	26	FO1	Ch.1 non-inverted output
3	FG	SP FG signal input	27	VDD	Control circuit power supply
4	EC	SP control signal input	28	H1H	SP Hall element 1 positive input
5	ECR	SP reference voltage input	29	H1L	SP Hall element 1 negative input
6	IN5	Ch.5 control signal input	30	H2H	SP Hall element 2 positive input
7	IN4	Ch.4 control signal input	31	H2L	SP Hall element 2 negative input
8	IN3	Ch.3 control signal input	32	H3H	SP Hall element 3 positive input
9	IN2	Ch.2 control signal input	33	H3L	SP Hall element 3 negative input
10	IN1	Ch.1 control signal input	34	VH	Hall-bias output
11	FB1	Ch.1 feedback output	35	VMSP1	SP Motor drive power supply
12	FB2	Ch.2 feedback output	36	CS	SP current detection
13	FB3	Ch.3 feedback output	37	A1	SP Driver output 1
14	FB4	Ch.4 feedback output	38	RCS1	SP Driver common Source output
15	FB5	Ch.5 feedback output	39	A2	SP Driver output 2
16	VREF	Ch reference voltage input	40	A3	SP Driver output 3
17	BMS	SP Break mode select input	41	RCS2	SP Driver common Source output
18	STBY	Total shutdown input	42	VMSP2	SP Motor drive power supply
19	RO3	Ch.3 inverted output	43	VMST	Ch.4 and 5 Motor drive power supply
20	FO3	Ch.3 non-inverted output	44	FO4	Ch.4 non-inverted output
21	PGAC	Ch.1 to 3 Coil drive GND	45	RO4	Ch.4 inverted output
22	VMAC	Ch1 to 3 Coil drive power supply	46	PGST	Ch4 and 5 Motor drive GND
23	RO2	Ch.2 inverted output	47	FO5	Ch.5 non-inverted output
24	FO2	CH2 non-inverted output	48	RO5	CH5 inverted output

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Storage temperature	Tstg	–55 to 150	°C	1
Operating ambient temperature	Topr	–30 to 85	°C	1
Supply voltage	VMST,VMAC VDD	6.0	V	
Supply current	IVMSP	1200	mA	2
	IVMAC	3000		
	IVMST	2000		
	IVDD	100		
Supply voltage applied range	VMSP,VMST, VMAC,VDD	-0.3 to 6.0	V	
Power dissipation	PD	307.9	mW	3
Drive power supply/output instantaneous current spindle	I (o)	± 3000	mA	Note) 4 o=37,38,39,40,41
Drive output current for ch.1,2 and ch.3	I (p)	± 1000	mA	p=19,20,23,24,25,26
Drive output current for ch.4 and ch.5	I (q)	± 1000	mA	q=44,45,47,48
Drive output voltage	V (l)	7.0	V	l=19,20,23,24,25,26, 44,45,47,48
Drive output voltage	V (m)	7.0	V	m=37,39,40
Control signal input voltage	V (n)	GND to VDD	V	n=2,3,4,5,6,7,8,9,10,1 1,12,13,14,15,16,17,18 ,28,29,30,31,32,33
Hall bias current	IHB(x)	30	mA	x=34

Note)1: Ta = 25°C except storage temperature and operating ambient temperature.
2: Make sure that channels 1 to 5 do not have a current flow exceeding 1000 mA.
3: Power dissipation shows the value of only package at Ta = 85°C.
4: The above drive output current (± 3000 mA) is permissible for a period exceeding 1 ms.
Note) Do not apply current or voltage from outside to any pin not listed above other than power supply and ground pin.
In the current circuit, (+) means current flowing into IC and (-) means current flowing out of IC.

■ Operating Supply Voltage Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage Range	VDD	4.0	5.0	5.5	V
	VMAC VMST VMSP	3.5	5.0	5.5	V

■ Electrical Characteristics V_{DD}=VMSP=VMAC=VMSL=5.0V,ECR=V_{REF}=1.65V,STBY=3.3V,R_L=8Ω
Note) 1, Ta=25°C±2°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current in standby mode	IVMS	STBY=L	—	—	20	μA
Control supply current in standby mode	IDDS	STBY=H	—	—	20	μA
Control supply current under no input	IDDA	STBY=H	—	12	16	mA
[Standby operation]						
STBY high-level input voltage	VSBH	(Active)	1.8	—	—	V
STBY low-level input voltage	VSBL	(Reset)	—	—	0.7	V
[VREF Rest]						
High-level input voltage	VRRH	(Active)	1.1	—	—	V
Low-level input voltage	VRRL	(Reset)	—	—	0.5	V
[SP Driver block]						
<Hall bias>						
Hall bias resistance	R_{HB}	I_{BH}=20mA	20	40	60	Ω
<Hall amp.>						
Input bias current	I_{BH}		—	—	3	μA
Common-mode input voltage range	V_{HBR}		1.5	2.5	4.0	V
Allowable Input current	V_{INH}		50	200	1000	mVp-p
<Torque control>						
Reference input voltage range	INECR		1.1	—	2.2	V
Dead zone (+)	$INSP_{DZ(+)}$		7	50	88	mV
Dead zone (+)	$INSP_{DZ(-)}$		7	50	88	mV
Input/Output gain	A_{CS}	R_{CS}=0.22Ω	1.07	1.33	1.59	A/V
Input bias current	I_{BH}		-1	—	1	μA
<Output>						
Upper-side output-ON resistance	R_{OH}	I_O=−500mA	—	0.32	0.50	Ω
Lower-side output-ON resistance	R_{OH}	I_O= 500mA	—	0.29	0.45	Ω
Torque limit current	I_{TL}	R_{CS}=0.22Ω	800	1000	1200	mA

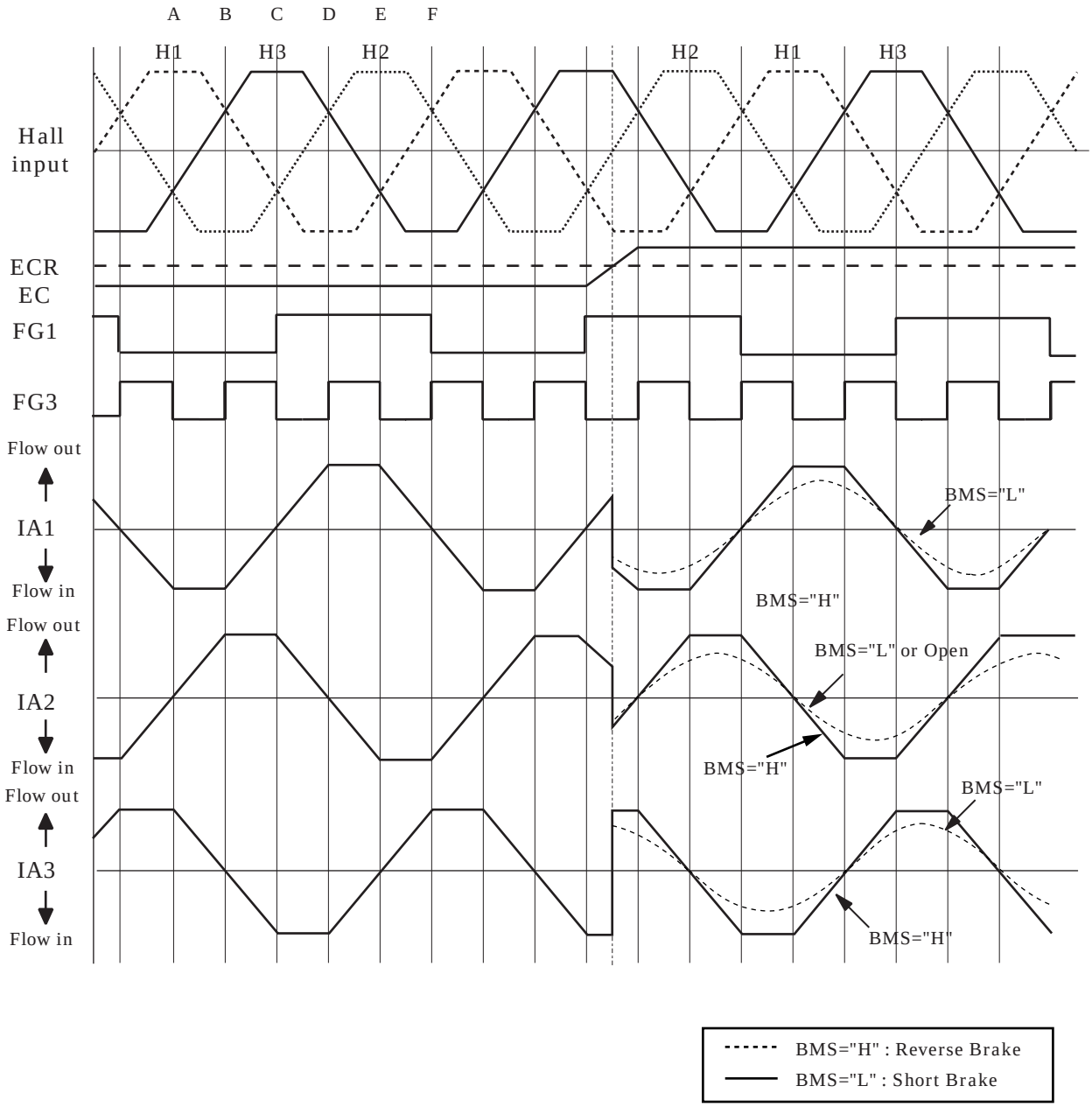
■ Electrical Characteristics V_{DD}=VMSP=VMAC=VMSL=5.0V,ECR=V_{REF}=1.65V,STBY=3.3V,R_L=8Ω
Note) 1, Ta=25°C±2°C unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<FG>						
High-level FG output	FGH	V_{FG}=3.3V,I_{FG}= −0.01mA R_{FG}=20kΩ	2.6	—	—	V
Low-level FG output	FGL	V_{FG}=3.3V,I_{FG}= −0.01mA R_{FG}=20kΩ	—	—	0.2	V
High-level SFG input voltage	VSFGH		2.6	—	—	V
Low-level SFG input voltage	VSFGL		—	—	0.5	V
<Brake mode selection switch>						
High-level BMS input voltage	VBMGH	(Reverse Brake)	2.6	—	—	V
Low-level BMS input voltage	VBMGL	(Short Brake)	—	—	0.5	V
[ch. Driver block]						
Ch.1 output-ON resistance (Upper + Lower)	RON1	RL=8Ω	—	1.5	2.3	Ω
Ch.2 and ch.3 output-ON resistance (Upper + Lower)	RON2, 3	RL=8Ω	—	1.3	2.0	Ω
Ch.4 and ch.5 output-ON resistance (Upper + Lower)	RON4, 5	RL=8Ω	—	1.1	1.7	Ω
Ch.1 to ch.3 output offset voltage	VOFS1 to 3	RL=8Ω VIN=VREF=1.65V	-70	—	+70	mV
Ch.4 and ch.5 output offset voltage	VOFS4 ,5	RL=8Ω VIN=VREF=1.65V	-50	—	+50	mV
Ch.1 to ch.3 voltage gain(+)	G1,2,3	RL=8Ω,RIN=15kΩ	14.3	16.3	18.3	dB
Ch.4 and ch.5 voltage gain(+)	G4,5	RL=8Ω,RIN=0Ω	16.0	18.0	20.0	dB
(+)/(–) relative gain	GR1to5	RL=8Ω	-1.5	—	+1.5	dB
Ch4,5 input conversion dead zone	VZD4,5	RL=8Ω,RIN=0Ω	10	25	40	mV
PWM frequency	FTR		172	230	288	kHz

(Reference values for design)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
[Thermal shutdown]						
Thermal shutdown circuit operating temperature	TTSD		—	160	—	°C
Thermal shutdown hysteresis width	ΔTTSD		—	30	—	°C

■ Phase Conditions of Hall Input and Output Current



■ Package Dissipation