

Panasonic

# DATA SHEET

Part No.	AN44060A
Package Code No.	HSOP042-P-0400D

SEMICONDUCTOR COMPANY  
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

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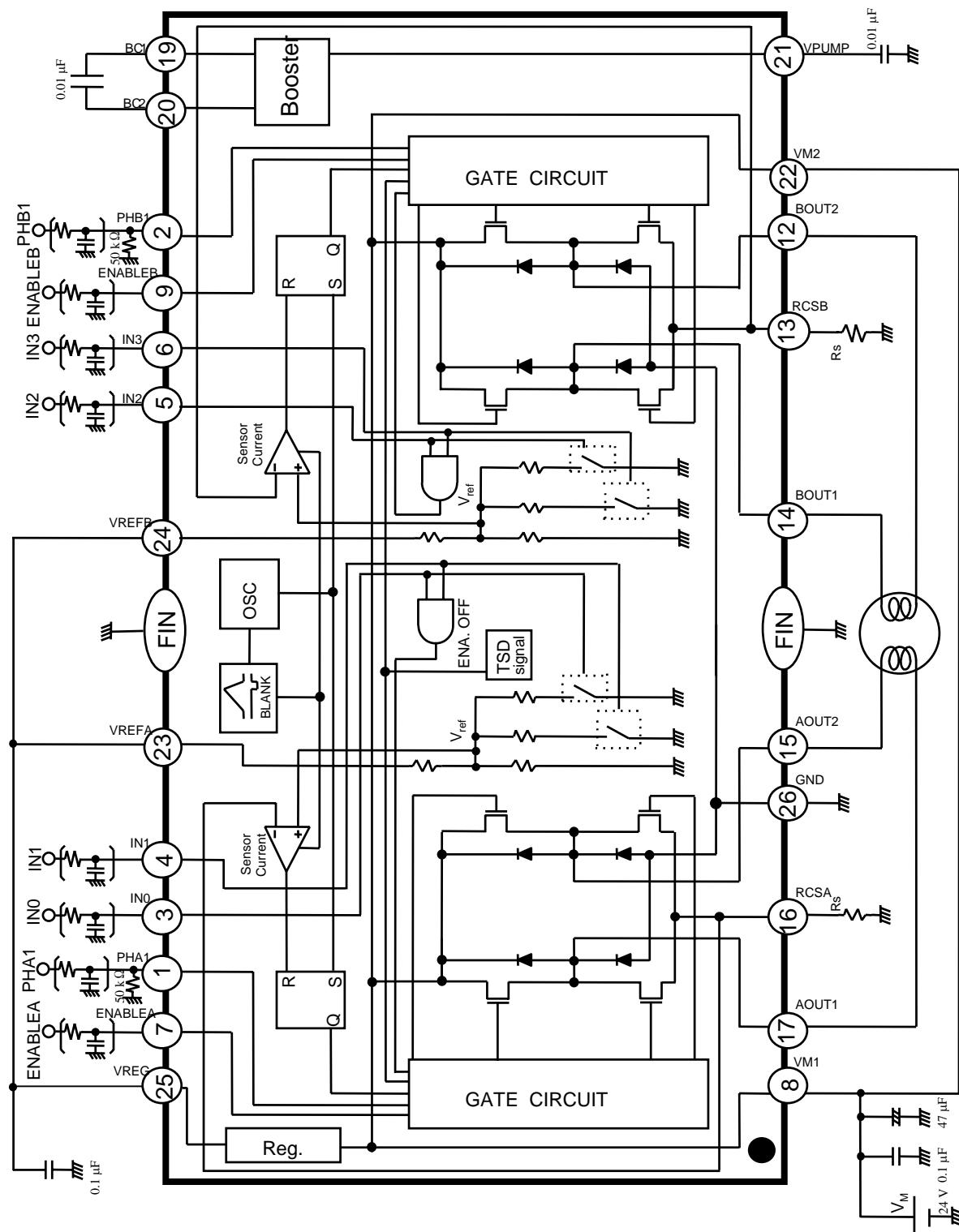
# AN44060A

## IC for Stepping Motor Drives

### ■ Function

- 4-phase input (W 1- and 2-phase excitation enabled; exclusive OR function incorporated for simultaneous-ON prevention)
- Built-in CR chopping (with frequency fixed)
- Built-in thermal protection circuit
- Built-in 5-V power supply

## ■ Block Diagram



Note) : Recommendable values are shown in the diagram.

## ■ Pin Descriptions

Pin No.	Function		Pin No.	Function	
1	PHA1	Phase A phase selection input	16	RCSA	Phase A current detection
2	PHB1	Phase B phase selection input	17	AOUT1	Phase A motor drive output 1
3	IN0	Phase A output torque control 1	18	N.C.	
4	IN1	Phase A output torque control 2	19	BC1	Booster capacitor connection 1
5	IN2	Phase B output torque control 1	20	BC2	Booster capacitor connection 2
6	IN3	Phase B output torque control 2	21	VPUMP	Boost circuit output
7	ENABLEA	Phase A start/stop signal input	22	VM2	Motor power supply 2
8	VM1	Motor power supply 1	23	VREFA	Phase A torque reference voltage input
9	ENABLEB	Phase B start/stop signal input	24	VREFB	Phase B torque reference voltage input
10	N.C.		25	VREG	Internal reference voltage (5-V output)
11	N.C.		26	GND	Signal ground
12	BOUT2	Phase B motor drive output 2	27	N.C.	
13	RCSB	Phase B current detection	28	N.C.	
14	BOUT1	Phase B motor drive output 1	FIN	GND	Signal ground
15	AOUT2	Phase A motor drive output 2			

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■ Absolute Maximum Ratings

Absolute Maximum Ratings					
No.	Parameter	Symbol	Rating	Unit	Note
1	Storage temperature	T <sub>stg</sub>	-55 to +150	°C	1
2	Operating ambient temperature	T <sub>opr</sub>	-20 to +70	°C	1
3	Operating ambient atmospheric pressure	P <sub>opr</sub>	$1.013 \times 10^5 \pm 0.61 \times 10^5$	Pa	
4	Operating constant gravity	G <sub>opr</sub>	9810	m/s <sup>2</sup>	
5	Operating shock	S <sub>opr</sub>	4900	m/s <sup>2</sup>	
6	Supply voltage	V <sub>M</sub>	30	V	
7	Power dissipation	P <sub>D</sub>	1.04	W	T <sub>a</sub> = 25°C

Notes) 1: Except for the storage temperature, operating ambient temperature, and power dissipation all ratings are for T<sub>a</sub> = 25°C.

■ Absolute Maximum Ratings

Absolute Maximum Ratings					
No.	Parameter	Symbol	Rating	Unit	Pin No.
8	Output pin voltage	$V_{OUT}$	30	V	12, 14, 15, 17
9	Motor drive current	$I_{OUT}$	1.8	A	12, 14, 15, 17
10	Flywheel diode current	$I_f$	1.8	A	12, 14, 15, 17
11	Boost circuit output voltage	$V_{PUMP}$	40	V	21
12	Voltage applied to the pins	PHA1, PHB1, IN0, IN1, IN2, IN3, ENABLEA, ENABLEB	-0.3 , 7	V	1, 2, 3, 4, 5, 6, 7, 9

Note) : Do not apply current or voltage from outside to any pin not listed above. In the circuit current, (+) means the current flowing into IC and (-) means the current flowing out of IC.

■ Recommended Operating Range

Operating supply voltage range	$V_M$	18.0 V to 28.0 V
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■ Electrical Characteristics

B		Electrical Characteristics ( $T_a = 25^\circ C \pm 2^\circ C$ unless otherwise specified)							
No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
	[Power Block]								
1	High-level output saturation voltage	$V_{OH}$	3	$I = -1.2 \text{ A}$	$V_M$ -0.38	$V_M$ -0.25	—	V	
2	Low-level output saturation voltage	$V_{OL}$	3	$I = 1.2 \text{ A}$	—	0.50	0.75	V	
3	Flywheel diode forward voltage	$V_{DI}$	4	$I = 1.2 \text{ A}$	0.5	1.0	1.5	V	
4	Output leakage current 1	$I_{LEAK1}$	1	OUT = 30 V, RCS = 0 V	—	10	50	$\mu\text{A}$	
5	Supply current (with two circuits turned on)	$I_M$	1	ENABLEA = ENABLEB = 5 V	—	10	20	mA	
	[I/O Block]								
6	High-level IN input voltage	$V_{INH}$	1		2.0	—	$V_{REG}$	V	
7	Low-level IN input voltage	$V_{INL}$	1		GND	—	0.6	V	
8	High-level IN input current	$I_{INH}$	1	IN0=IN1=IN2=IN3=5V	-10	0	10	$\mu\text{A}$	
9	Low-level IN input current	$I_{INL}$	1	IN0=IN1=IN2=IN3=0V	-80	-40	-20	$\mu\text{A}$	
10	High-level PHA1/PHB1 input voltage	$V_{PHAH}$ $V_{PHBH}$	1		2.0	—	$V_{CC}$	V	
11	Low-level PHA1/PHB1 input voltage	$V_{PHAL}$ $V_{PHBL}$	1		GND	—	0.6	V	
12	High-level PHA1/PHB1 input current	$I_{PHAH}$ $I_{PHBH}$	1	PHA1 = PHB1 = 5 V	-10	0	10	$\mu\text{A}$	
13	Low-level PHA1/PHB1 input current	$I_{PHAL}$ $I_{PHBL}$	1	PHA1 = PHB1 = 0 V	-150	-100	-50	$\mu\text{A}$	

Note) :  $V_M = 24 \text{ V}$  unless otherwise specified.

**■ Electrical Characteristics**

B		Electrical Characteristics ( $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified)							
No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
14	High-level ENABLEA/ ENABLEB input voltage	$V_{\text{ENABLEAH}}$ $V_{\text{ENABLEBH}}$	1		2.0	—	$V_{\text{REG}}$	V	
15	Low-level ENABLEA/ ENABLEB input voltage	$V_{\text{ENABLEAL}}$ $V_{\text{ENABLEBL}}$	1		GND	—	0.6	V	
16	High-level ENABLEA/ ENABLEB input current	$I_{\text{ENABLEAH}}$ $I_{\text{ENABLEBH}}$	1	ENABLEA = ENABLEB = 5 V	-10	0	10	$\mu\text{A}$	
17	Low-level ENABLEA/ ENABLEB input current	$I_{\text{ENABLEAL}}$ $I_{\text{ENABLEBL}}$	1	ENABLEA = ENABLEB = 0 V	-15	-2	15	$\mu\text{A}$	
	[Torque Control Block]								
18	Input bias current	$I_{\text{REFA}}$ $I_{\text{REFB}}$	1	$V_{\text{REFA}} = V_{\text{REFB}} = 5 \text{ V}$	67	90	150	$\mu\text{A}$	
19	PWM frequency	$f_{\text{PWM}}$	2		25.1	33.5	41.9	kHz	
20	Pulse blanking time	$T_B$	2	$V_{\text{REFA}} = V_{\text{REFB}} = 0 \text{ V}$	1.0	2.0	3.0	$\mu\text{s}$	
21	Cmp threshold H (100%)	$VT_H$	1	$IN0 = IN1 = 0 \text{ V}$ $IN2 = IN3 = 0 \text{ V}$	0.479	0.503	0.528	V	
22	Cmp threshold C (67%)	$VT_C$	1	$IN0 = 5 \text{ V}, IN1 = 0 \text{ V}$ $IN2 = 5 \text{ V}, IN3 = 0 \text{ V}$	0.305	0.330	0.356	V	
23	Cmp threshold L (33%)	$VT_L$	1	$IN0 = 0 \text{ V}, IN1 = 5 \text{ V}$ $IN2 = 0 \text{ V}, IN3 = 5 \text{ V}$	0.151	0.167	0.185	V	
	[Reference Voltage Block]								
24	Reference voltage	$V_{\text{REG}}$	1	$VM = 24 \text{ V}$	4.5	5.0	5.5	V	
25	Output impedance	$Z_{\text{REG}}$	1	$VM = 24 \text{ V}, I_{\text{SREG}} = -10 \text{ mA}$	—	8	20	$\Omega$	

■ Electrical Characteristics

B		Electrical Characteristics ( $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified)							
No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
	[Output Block]								
26	Output sleue rate 1	$VT_r$		Rising edge	—	240	—	V/ $\mu$ s	
27	Output sleue rate 2	$VT_f$		Falling edge	—	-240	—	V/ $\mu$ s	
28	Dead time	$T_D$			—	1.5	—	$\mu$ s	
	[Thermal Protection]								
29	Thermal protection operating temperature	$TSD_{on}$			—	160	—	°C	
30	Thermal protection hysteresis width	$\Delta TSD$			—	45	—	°C	

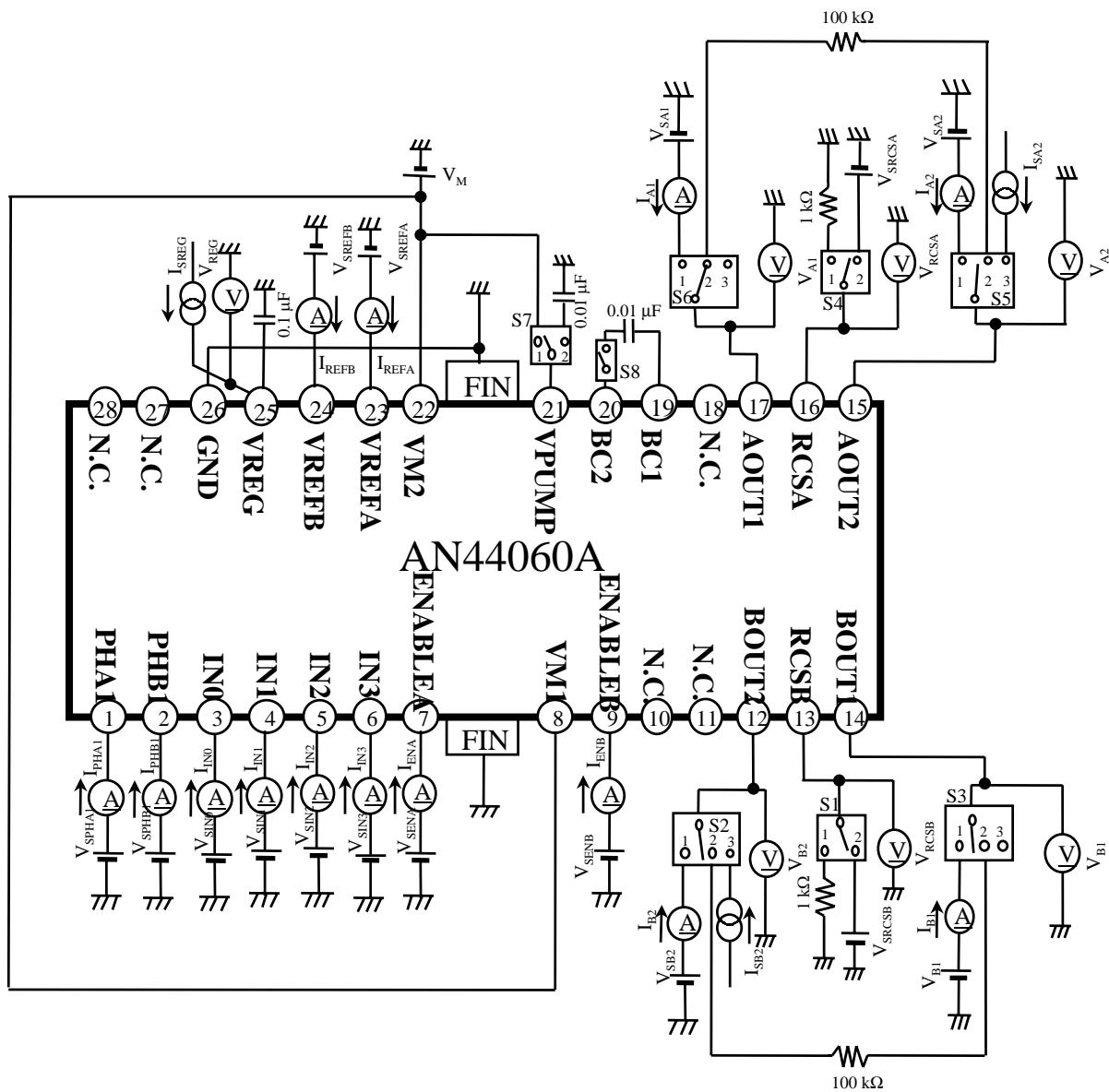
Note) : The characteristics listed above are reference values based on the IC design and not guaranteed.

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## ■ Test Circuit Diagram 1

Test Circuit 1



■ Electrical Characteristics Test Procedures 1

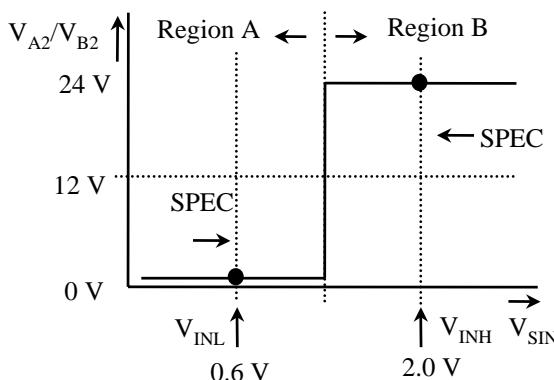
Test Circuit 1 Testing Conditions

No.	Measuring Pin	Relay Conditions						Voltage Conditions					
		S1 /S4	S2 /S5	S3 /S6	S7	S8		V <sub>SREFA</sub> /V <sub>SREFB</sub>	I <sub>SREG</sub>	Hi-Z	Hi-Z	Hi-Z	Hi-Z
4	12, 14, 15, 17	2	1	1	1			V <sub>SREFA</sub> /V <sub>SREFB</sub>	5 V	30 V	30 V	30 V	-10mA
4	14, 17	2	3	1	1			I <sub>S2</sub> /I <sub>S3</sub>	Hi-Z	Hi-Z	Hi-Z	24 V	5 V
4	12, 15	2	1	3	1			V <sub>SA1</sub> /V <sub>SB1</sub>	0 V	30 V	Hi-Z	Load R	5 V
5, 9, 13, 17, 18	1, 2, 3, 4, 5, 6, 7, 9, 23, 24, 25	1	2	2	2			V <sub>SA2</sub> /V <sub>SB2</sub>	0 V	Hi-Z	30 V	Load R	5 V
1, 25	25	1	2	2	2			V <sub>SENA</sub> /V <sub>SENB</sub>	5 V	0 V	0 V	Load R	5 V
8, 12, 16	1, 2, 3, 4, 5, 6, 7, 9	1	2	2	2			V <sub>SINA</sub> /V <sub>SINB</sub>	5 V	0 V	0 V	Load R	5 V
6, 7	12, 15	1	3	3	2			V <sub>SIN1</sub> /V <sub>SIN3</sub>	5 V	0 V	0 V	0 V	5 V
10, 11	12, 15	1	3	3	2			V <sub>SIN2</sub> /V <sub>SIN4</sub>	5 V	0 V	0 V	0 V	5 V
14, 15	12, 15	1	3	3	2			V <sub>SINH1</sub> /V <sub>SINH3</sub>	5 V	0 V	0 V	0 V	5 V
21	12, 15	2	3	3	2			V <sub>SINH2</sub> /V <sub>SINH4</sub>	5 V	0 V	0 V	0 V	5 V
22	12, 15	2	3	3	2			V <sub>SINL1</sub> /V <sub>SINL3</sub>	5 V	0 V	0 V	0 V	5 V
23	12, 15	2	3	3	2			V <sub>SINL2</sub> /V <sub>SINL4</sub>	5 V	0 V	0 V	0 V	5 V

■ Electrical Characteristics Test Procedures 1

6. High-level IN input voltage  $V_{INH}$

7. Low-level IN input voltage  $V_{INL}$



Check the conditions by measuring the  $V_{OUT}$  voltage with the input voltage set to high level and low level respectively.

Region A: Power transistor on the flow-in side turned on.

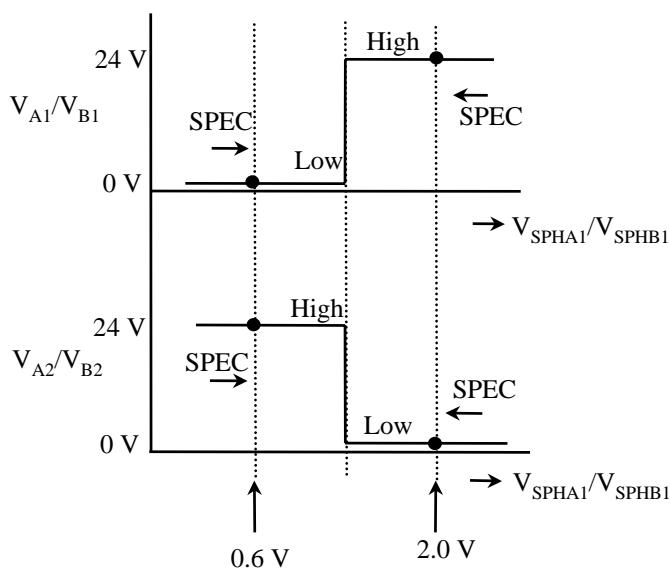
Region B : Power transistor on the flow-in side turned off.

The power transistor on the flow-out side is turned off in the above regions.

Measuring Pin	Voltage Conditions			Status
	$V_{SPHA1}/V_{SPHB1}$	$V_{IN0}/V_{IN2}$	$V_{IN1}/V_{IN3}$	
$V_{AOUT2}/V_{BOUT2}$	5.0 V	0.6 V	5.0 V	AOUT2/BOUT2 = 0 V
	5.0 V	2.0 V	5.0 V	AOUT2/BOUT2 = 24 V
$V_{AOUT2}/V_{BOUT2}$	5.0 V	5.0 V	0.6 V	AOUT2/BOUT2 = 0 V
	5.0 V	5.0 V	2.0 V	AOUT2/BOUT2 = 24 V

10. High-level PHA1/PHB1 input voltage  $V_{PHAH}, V_{PHBH}$

11. Low-level PHA1/PHB1 input voltage  $V_{PHAL}, V_{PHBL}$



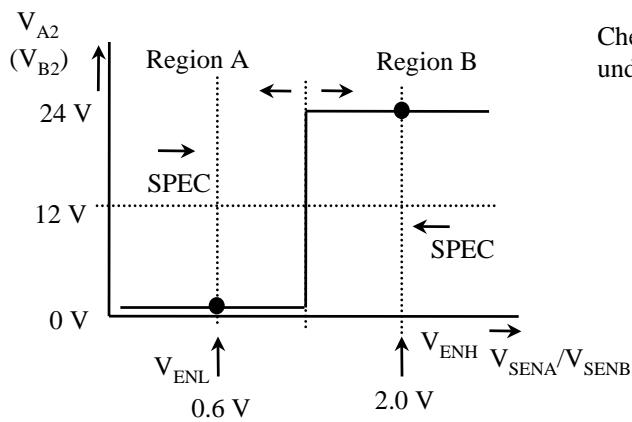
Check the conditions by measuring the AOUT1/BOUT1 voltage and AOUT2/BOUT2 voltage with the input voltage set to high level and low level respectively.

Measuring Pin	Voltage Conditions	
	$V_{SPHA1}/V_{SPHB1}$	Status
$V_{AOUT1}/V_{BOUT1}$	0.6 V	Low-level output
$V_{AOUT2}/V_{BOUT2}$	0.6 V	High-level output
$V_{AOUT1}/V_{BOUT1}$	2.0 V	High-level output
$V_{AOUT2}/V_{BOUT2}$	2.0 V	Low-level output

■ Electrical Characteristics Test Procedures 1

14. High-level ENABLEA/ENABLEB input voltage  $V_{ENABLEAH}, V_{ENABLEBH}$

15. Low-level ENABLEA/ENABLEB input voltage  $V_{ENABLEAL}, V_{ENABLEBL}$



Check that the threshold voltage is in the specification range (SPEC) under the following condition.

$$V_{SPHA1} = V_{SPHB1} = 5 \text{ V}$$

$V_{SENA}/V_{SENB}$	$V_{AOUT2}/V_{BOUT2}$
0.6 V	0 V
2.0 V	24 V

Region A: Power transistor on the flow-in side turned on.

Region B: Power transistor on the flow-in side turned off.

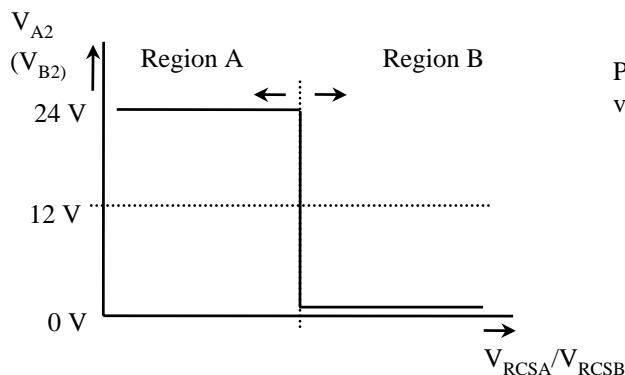
The power transistor on the flow-out side is turned off in the above regions.

## ■ Electrical Characteristics Test Procedures 1

21. Comp threshold H  $V_{TH}$

22. Comp threshold C  $V_{TC}$

23. Comp threshold L  $V_{TL}$



Perform RCS voltage sweeping and measure the threshold voltages on the output pins respectively.

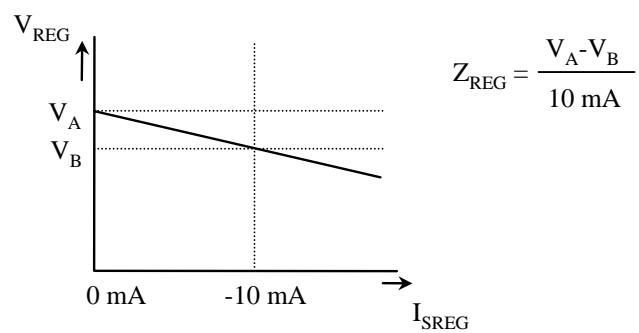
Region A: Always high-level output

Region B: High-level output  
with the duty kept to  
a minimum



Symbol	Measuring Pin	Voltage Conditions			Measurement Conditions
		$V_{SPHA1}/V_{SPHB1}$	$V_{SIN0}/V_{SIN2}$	$V_{SIN1}/V_{SIN3}$	
$V_{TH}$	$V_{AOUT2}/V_{BOUT2}$	5 V	0 V	0 V	Measure the $V_{AOUT2}/V_{BOUT2}$ threshold voltage.
$V_{TC}$	$V_{AOUT2}/V_{BOUT2}$	5 V	5 V	0 V	Measure the $V_{AOUT2}/V_{BOUT2}$ threshold voltage.
$V_{TL}$	$V_{AOUT2}/V_{BOUT2}$	5 V	0 V	5 V	Measure the $V_{AOUT2}/V_{BOUT2}$ threshold voltage.

25. Output impedance  $Z_{REG}$

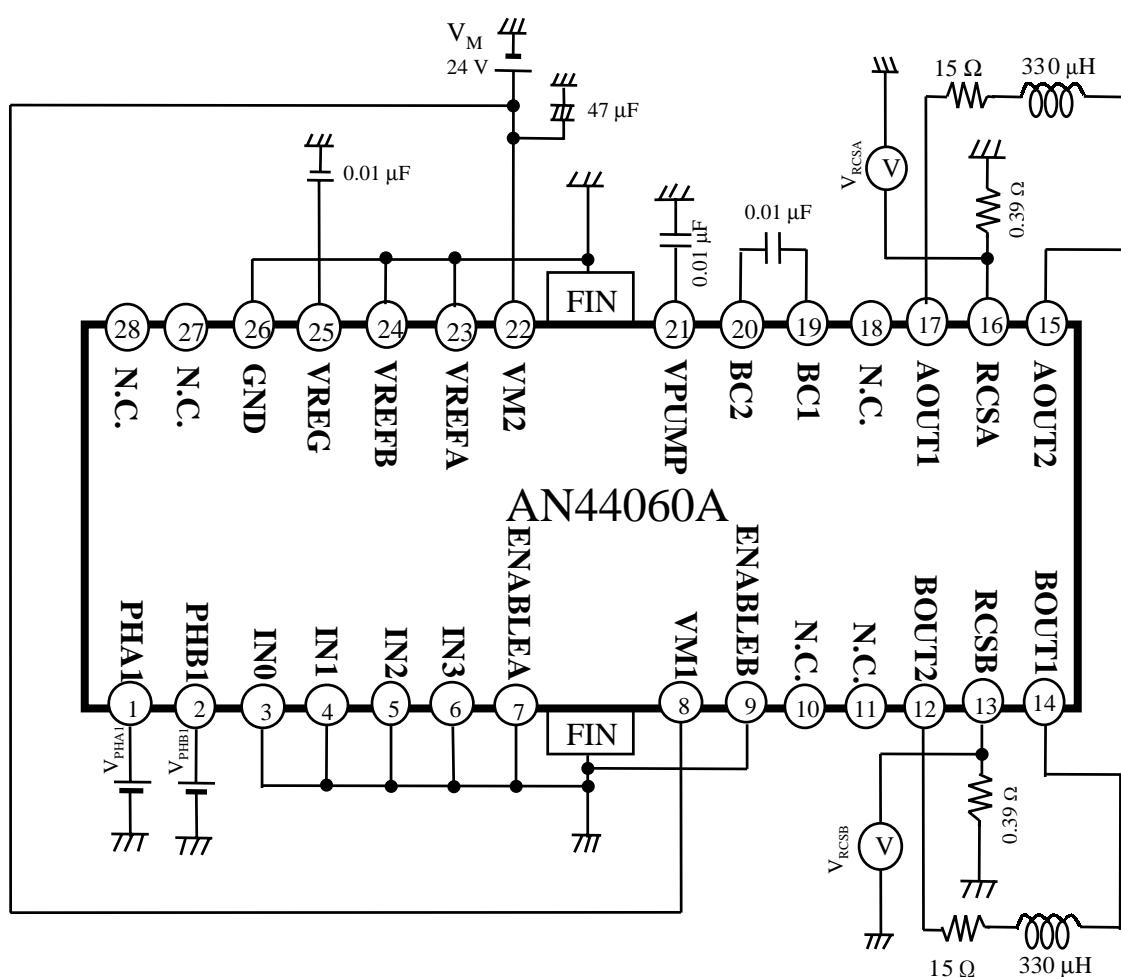


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## ■ Test Circuit Diagram 2

Test Circuit 2



■ Electrical Characteristics Test Procedures 2

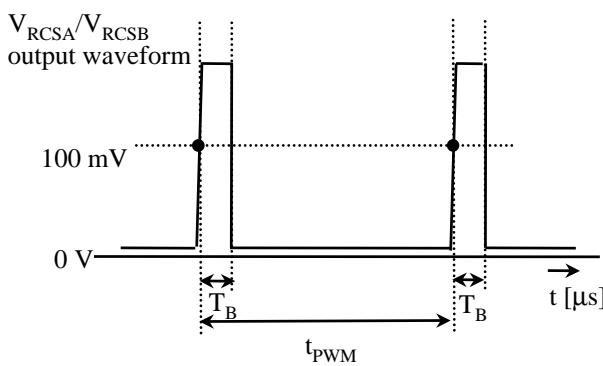
**19. PWM frequency  $t_{\text{PWM}}$**

**20. Pulse blanking time  $T_B$**

These values are obtained from the RCSA and RCSB voltages with both PHA1 and PHB1 set to 0 V and 5 V respectively under the following condition.

$$V_{\text{REFA}} = V_{\text{REFB}} = 0 \text{ V}$$

The  $V_{\text{RCSA}}/V_{\text{RCSB}}$  output waveform is shown below.



**PWM frequency  $t_{\text{PWM}}$**

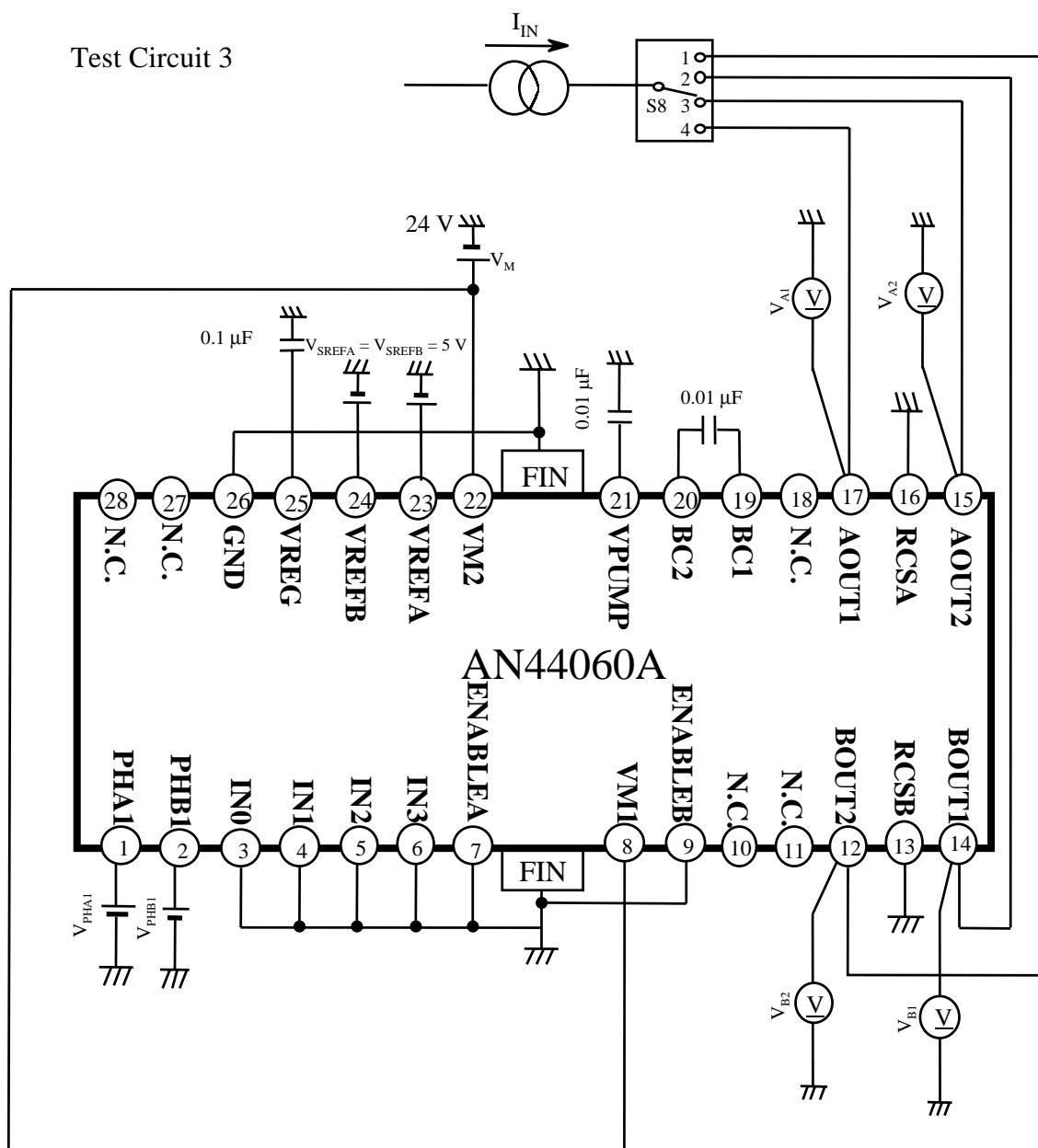
Measure the cycle time of output voltage pulses and obtain the value from the following formula.

$$f_{\text{PWM}} = \frac{1}{t_{\text{PWM}}}$$

**Pulse blanking time  $T_B$**

Measure the high-level time of RCS voltage output.

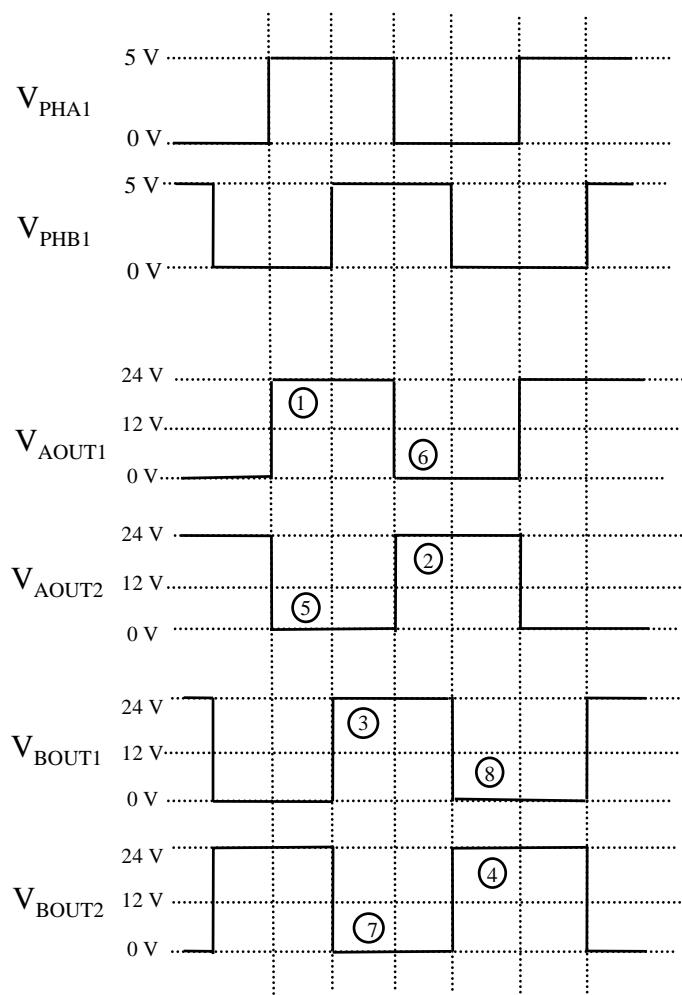
## ■ Test Circuit Diagram 3



■ Electrical Characteristics Test Procedures 3

1. High-level output saturation voltage  $V_{OH}$

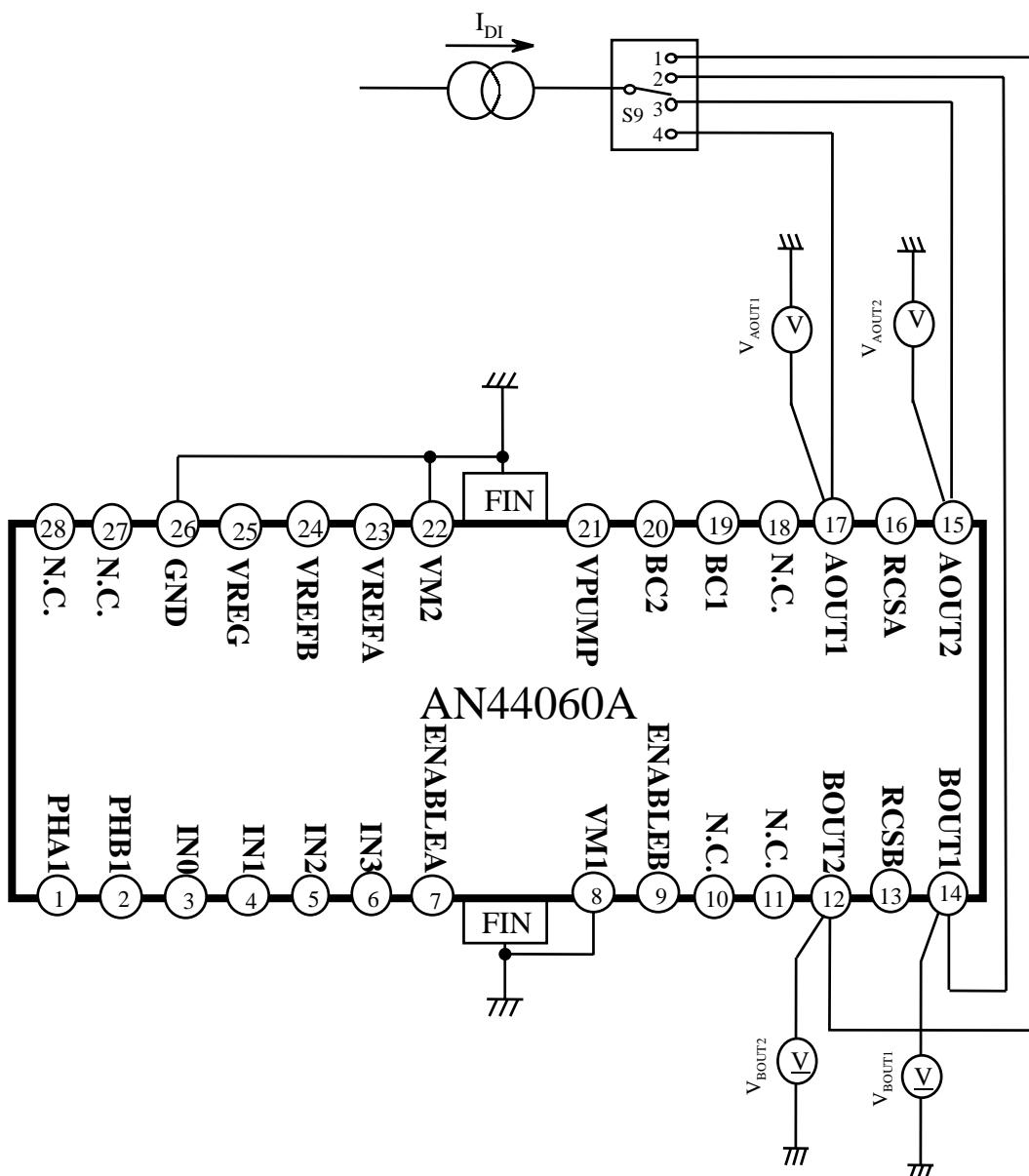
2. Low-level output saturation voltage  $V_{OL}$



No.	Measuring Pin	Voltage Conditions		Remarks
		IN0, IN1, IN2, IN3	$I_{IN}$	
1	AOUT1/AOUT2 BOUT1/BOUT2	0 V	-1.2 A	Judge each logic of the AOUT1, AOUT2, BOUT1, and BOUT2 at ① to ④ above.
2	AOUT1/AOUT2 BOUT1/BOUT2	0 V	1.2 A	Judge each logic of the AOUT1, AOUT2, BOUT1, and BOUT2 at ⑤ to ⑧ above.

## ■ Test Circuit Diagram 4

Test Circuit 4

3. Flywheel diode voltage  $V_{DI}$ 

Relay Conditions		
No.	Measuring Pin	S9
3	$V_{OUT}$	Measure the diode voltage at each level on contacts 1, 2, 3, and 4 of S9.

■ Terminal Equivalent Circuits

Pin	Equivalent Circuit	Pin	Equivalent Circuit
Pin 1 (PHA1) Pin 2 (PHB1)		Pin 15 (AOUT2) Pin 16 (RCSA) Pin 17 (AOUT1)	
Pin 3 (IN0) Pin 4 (IN1) Pin 5 (IN2) Pin 6 (IN3) Pin 7 (ENABLEA) Pin 9 (ENABLEB)		Pin 19 (BC1)	
Pin 12 (BOUT2) Pin 13 (RCSB) Pin 14 (BOUT1)		Pin 20 (BC2) Pin 21 (VPUMP)	

■ Terminal Equivalent Circuits

Pin	Equivalent Circuit	Pin	Equivalent Circuit
Pin 23 (VREFA) Pin 24 (VREFB)			
Symbols	<ul style="list-style-type: none"> <li>↑ VREG (Pin 14)</li> <li>↗ VM (Pin 8, Pin 22)</li> <li>↓ Diode</li> <li>↖ Zener diode</li> <li>↔ Ground (FIN)</li> </ul>		

## ■ Usage Notes

[Precautions for this IC]

- Perform thermal design work with consideration of a sufficient margin to keep the power dissipation based on supply voltage, load, and ambient temperature conditions.
- The protection circuit is incorporated for the purpose of securing safety if the IC malfunctions. Therefore, design the protection circuit so that the protection circuit will not operate under normal operating conditions. The temperature protection circuit, in particular, may be destructed before the temperature protection circuit operates if the area of safety operation of the device or the maximum rating is exceeded instantaneously due to the short-circuiting between the output pin and VM pin or a ground fault caused by the output pin and ground pin.
- Pay utmost attention to the pattern layout in order to prevent the IC from destruction resulting from the short-circuiting of pins. See page 17 *Pin Descriptions* for allocations of the pins of the IC.
- When driving a motor coil or transformer (L) load, the device may be destructed as a result of a negative or excessive voltage generated at the time of turning the load on and off. Unless otherwise provided in the specifications, do not apply any negative or excessive voltage.
- Do not make mistakes in the PCB mounting direction. If power is supplied with the pins mounted in the wrong direction, the IC may be destructed.
- The IC may be destructed by the solder bridge between the pins of semiconductor devices. Fully make a visual check on the PCB before supplying power. Furthermore, the IC may be destructed if conductive foreign matters like solder chips are stuck to the IC during transportation after PCB mounting. Therefore, conduct full technical verification of the mounting quality of the IC.
- The IC is destructed under an abnormal condition, such as the short-circuiting between the output and VM pins, output and ground pins, or output pins (i.e., load short-circuiting), in which case smoke may be generated. Pay utmost attention to the use of the IC.

Pay special attention to the following pins so that they are not short-circuited with the VM pin, ground pin, other output pin, or current detection pin.

- (1) AOUT1 (pin 17), AOUT2 (pin 15), BOUT1 (pin 14), BOUT2 (pin 12)
- (2) BC2 (pin 20), VPUMP (pin 21)
- (3) VM1 (pin 8), VM2 (pin 22), VREG (pin 25)
- (4) RCSA (pin 16), RCSB (pin 13)

The higher the current capacity of power supply is, the higher the possibility of the above destruction or smoke generation. Therefore, it is recommended to take safety countermeasures, such as the use of a fuse.

- When using the IC for model expansion or new sets, be sure to make full safety checks including a long-term reliability check on each set.

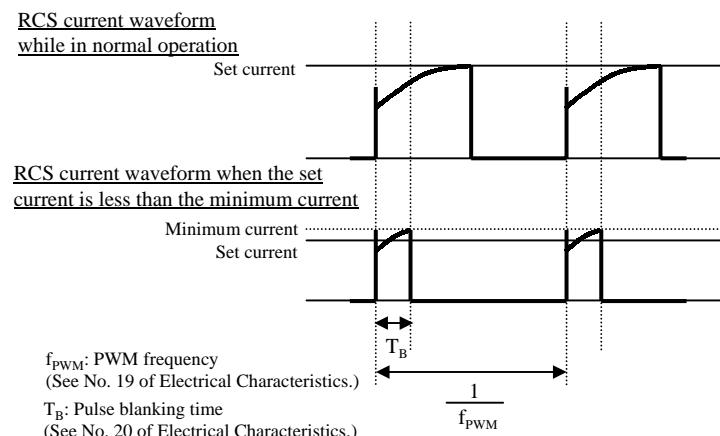
## ■ Usage Notes

(continued)

- Set the value of the capacitor between the VPUMP and GND pins so that the voltage on the VPUMP pin (pin 21) will not exceed 40 V in any case regardless of whether it is a transient phenomenon or not while the motor standing by is started.
- This IC employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the IC is apt to generate noise that may cause the IC to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the VREG and GND pins must be a minimum of 1  $\mu$ F and the one between the VM and GND pins must be a minimum of 47  $\mu$ F and as close as possible to the IC so that PWM noise will not cause the IC to malfunction or have fatal damage.
- The HBM electrostatic breakdown voltage (with a capacitance of 100 pF and a resistance of 1.5 k $\Omega$ ) of BC1 pin (pin 19) is approx. 1500 V.
- On the other hand, the minimum MM electrostatic breakdown voltage (with a capacitance of 200 pF and a resistance of 0  $\Omega$ ) applicable to all pins is 250 V.
- PHA1 pin (pin 1) and PHB1 pin (pin 2) are pulled up with 50 k $\Omega$  to VREG. There will be no problem if the input device connected to this IC is a microcontroller operating at 5 V. If the microcontroller used operates at a voltage less than 5 V (e.g., 3.3 V), however, a problem may result, because 5 V will be applied to the microcontroller output pin when the pin is at high impedance, which may be in excess of the dielectric strength of the microcontroller. If a state of high impedance is likely to occur, pull down PHA1 pin (pin 1) and PHB1 pin (pin 2) with appropriate resistance for the protection of the microcontroller.
- In order to prevent mistakes in current detection resulting noise, this IC is provided with a pulse blanking time of 2.0  $\mu$ s (typ.). The motor current will not be less than the current determined by blanking time. Pay utmost attention at the time of minute current control.

The graph on the right-hand side shows the relationship between the pulse blanking time and minute current value.

The increase or decrease in the motor current is determined by the resistance of the internal winding of the motor.

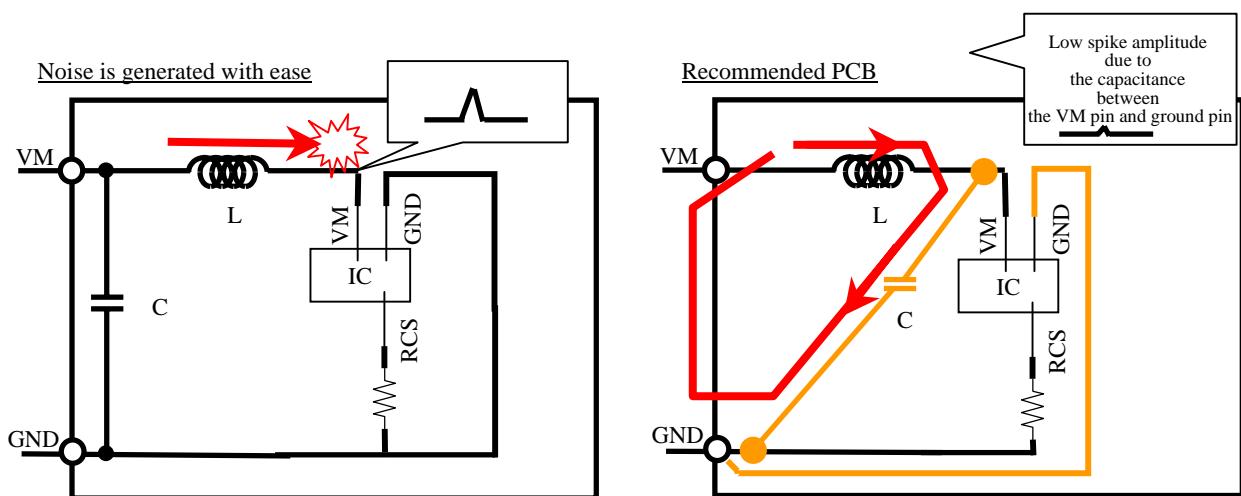


## ■ Usage Notes

(continued)

- A high current flows into the IC. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

A high current flows into the line between the VM1 (pin 8) and VM2 (pin 22) pins. Therefore, noise is generated with ease at the time of switching due to the inductance (L) of the line, which may result in the malfunctioning or destruction of the IC (see the circuit diagram on the left-hand side). As shown in the circuit diagram on the right-hand side, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the IC. This makes it possible to suppress the direct VM pin voltage of the IC. Make the settings as shown in the circuit diagram on the right-hand side as much as possible.



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