### **Driver IC for 3-phase Brushless Motor**

#### **FEATURES**

- Supply voltage range: 4.5 V ~ 26.4 V
- Built-in 5-V regulator
- 3-phase full-wave sine-wave PWM drive by 1-Hall-sensor
- Selectable Input Mode: Either linear voltage input or PWM input through VSP pin
- Selectable the start frequency through SWSF pin
- Conduction angle auto driver phase shift correction
- Rotation direction selectable (Forward/Reverse)
- FG pulse divide selectable
- Sleep mode
- Various protection functions:
   Under Voltage Lock Out (UVLO), Over Voltage Lock Out (OVLO), Thermal protection,
   Over Load Protection, and Over Current Protection

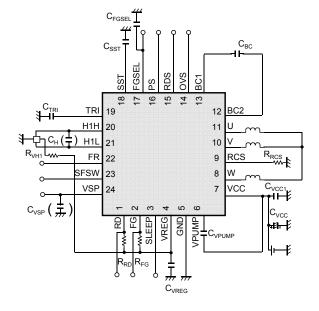
### **DESCRIPTION**

AN44143A is a driver IC for 3-phase brushless motor optimized for fan motors.
 By employing the rotor position detector and sine wave PWM drive by 1-Hall-sensor, this IC achieves component reduction and miniaturization of motor set as well as motor drive at low noise, low vibration and low power consumption.

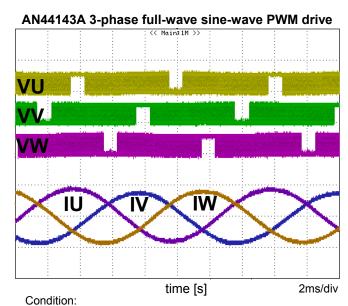
#### **APPLICATIONS**

Driver IC for 3-phase brushless fan motor

### TYPICAL APPLICATION



Notes: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.



 $V_{CC}$  = 12 V,  $V_{FR}$  = 0 V,  $V_{VSP}$  = PWM mode (60kHz,Duty60%)

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**AN44143A** 

### **ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V <sub>CC</sub>	28	V	*1
Operating ambient temperature	T <sub>opr</sub>	− 40 ~ + 95	°C	*2
Storage temperature	T <sub>stg</sub>	− 55 ~ +150	°C	*2
	$V_{VREG}$	-0.3 ~ 6.0	V	*3
Input Voltage Range	$\begin{matrix} V_{\text{SLEEP}}, V_{\text{H1H}}, V_{\text{H1L}}, V_{\text{FGSEL}}, \\ V_{\text{VSP}}, V_{\text{SFSW}}, V_{\text{FR}}, V_{\text{RDS}}, V_{\text{PS}}, V_{\text{OVS}} \end{matrix}$	-0.3 ~ 6.0	٧	_
	V <sub>TRI</sub> ,V <sub>SST</sub>	-0.3 ~ 6.0	V	_
	$V_{FG}, V_{RD}$	-0.3 ~ 6.0	V	_
	$V_{VREG}$	-0.3 ~ 6.0	V	_
Output Voltage Range	$V_{RCS}$	-0.3 ~ 6.0	V	*4
	V <sub>BC1</sub>	28	V	*4
	$V_{BC2}, V_{pump}$	37	V	*4
	I <sub>Upeak</sub> , I <sub>Vpeak</sub> , I <sub>Wpeak</sub>	± 2200	mA	*5, *6
Output Current Range	I <sub>FG</sub> ,I <sub>RD</sub>	5	mA	
	I <sub>VREG</sub>	- 10	mA	_
ESD	HBM	2	kV	

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

- \*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
- \*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 ...
- \*3: Applying external voltage to this pin is possible only when this pin and VCC pin is connected.

  When applying external voltage to this pin, do not exceed the stated ratings even in transient state.
- \*4: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.
- \*5: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.
- \*6: For VCC 5.6 V, output current is ± 2200 mA. For VCC < 5.6 V, output current is ± 1500 mA. Please ensure that there is enough margin and the design does not exceed the allowable value of Power Dissipation(P<sub>D</sub>) and Area of Safe Operation(ASO).

#### POWER DISSIPATION RATING

Package	$\theta_{j-a}$	$\theta_{ extsf{j-c}}$	P <sub>D</sub> (T <sub>a</sub> =25 °C)	P <sub>D</sub> (T <sub>a</sub> =70 °C)
24 pin Plastic Quad Flat Non-leaded Package (QFN type)	56.1 °C/W	4.4 °C/W	2.22 W	1.42 W

Notes: For the actual usage, please refer to the P<sub>D</sub>-T<sub>a</sub> characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

- \*1: Glass-Epoxy Substrate (2 Layers) : 50 x 50 x 0.8t (mm), Heat dissipation fin: Die-pad, Soldered. (Heat dissipation via 2 layer board)
- \*2: For Ta = 70 , output current  $I_{Udc}$ ,  $I_{Vdc}$ ,  $I_{Wdc}$  at Tj = 120 is  $\pm$  600 mA(reference value).



### **CAUTION**

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

### **AN44143A**

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Supply voltage range	V <sub>CC</sub>	4.5	_	26.4	V	
	$V_{SLEEP}$	0	_	$V_{VREG}$	V	*1
	V <sub>H1H</sub>	0	_	$V_{VREG}$	V	*1
	V <sub>H1L</sub>	0	_	$V_{VREG}$	V	*1
	$V_{PS}$	0	_	$V_{VREG}$	V	*1
Input voltage range	$V_{RDS}$	0	_	$V_{VREG}$	V	*1
Input voltage range	V <sub>ovs</sub>	0	_	$V_{VREG}$	V	*1
	$V_{FGSEL}$	0	_	$V_{VREG}$	V	*1
	$V_{VSP}$	0	_	$V_{VREG}$	V	*1
	$V_{SFSW}$	0	_	$V_{VREG}$	V	*1
	$V_{FR}$	0	_	$V_{VREG}$	V	*1
	C <sub>vcc</sub>	4.7μ	_	_	F	*2,*3
	C <sub>VCC1</sub>	_	0.1μ	_	F	*2,*3
	C <sub>VREG</sub>	_	0.1μ	_	F	*2,*4
	C <sub>SST</sub>	22p	1800p	_	F	*2,*5
	C <sub>BC</sub>	_	0.1μ	_	F	*2,*4
External constants	C <sub>VPUMP</sub>	_	0.1μ	_	F	*2,*4
	C <sub>TRI</sub>	220p	390p	1300p	F	*2,*5
	R <sub>RCS</sub>	0.15	0.22	_	Ω	*2,*5,*6
	R <sub>VH</sub>	_	1k	_	Ω	*2,*5
	C <sub>FGSEL</sub>	_	0.01μ	_	F	*2,*7
	C <sub>VSP</sub>		0.1μ	_	F	*2,*8

Note: \*1: For setting range of input control voltage, refer to Electrical Characteristics (page 5 - 8) and Operation (page 11 - 33).

- \*3: Please perform sufficient evaluation and verification to ensure that VCC pin voltage ripple is reduced.
- \*4: It is recommended to use the values indicated.
- \*5: Please choose the setting according to the usage. Please refer to the Electrical Characteristics (page 5 8) and Operation (page 11 33).
- \*6: Do not use resistor of value smaller than this. When using value smaller than the minimum value, latch-up function which is used to prevent thermal damage may operate due to external factors (PCB heat dissipation, metal impedance, etc...) or internal factors (threshold change, etc...).
- \*7: When using with FGSEL pin open, please connect capacitor to the FGSEL pin to prevent noise and carry out sufficient evaluation and verification.
- \*8: When VSP pin is used for DC input, it is recommended to insert a capacitor to the VSP pin.

<sup>\*2:</sup> Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

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### **ELECTRICAL CHARACTERISTICS**

 $V_{\rm CC}$  = 12.0 V,  $V_{\rm VREG}$  = 5.0 V

Note:  $T_a = 25^{\circ}C \pm 2^{\circ}C$  unless otherwise noted.

	Parameter		Symbol	Condition		Limits		Unit	Note
V <sub>CC</sub> current   I <sub>CC1</sub>     3.0   5.6   9.0   mA     V <sub>CC</sub> current at sleep mode   I <sub>CC3</sub>   V <sub>SLEEP</sub> = H       50   μA     Regulator Block     VREG voltage   V <sub>VREG</sub>     4.7   5   5.3   V     Output impedance   Z <sub>VREG</sub>   I <sub>VREG</sub> = -10 mA       10   Ω     FG Block   FG output (low voltage)   V <sub>FGL</sub>   I <sub>FG</sub> = 1.0 mA     0.1   0.3   V     RD Block   RD output (low voltage)   V <sub>ROL</sub>   I <sub>FG</sub> = 1.0 mA     0.1   0.3   V     Power Block   On resistance   R <sub>ONHL</sub>   I = 400 mA     0.1   0.3   V     On resistance   V <sub>CC</sub> = 4.5V   I = 400 mA     1.25   2.05   Ω     Diode forward voltage   V <sub>D1</sub>   I = 400 mA   0.6   0.8   1   V     Motor Lock Protection     Lock detection time_LL   t <sub>LOCK1_LL</sub>   RDS, SFSW = L,L   0.35   0.5   0.65   s     Lock release time_LL   t <sub>LOCK1_LL</sub>   RDS, SFSW = L,L   3.5   5   6.5   s     Lock protection ratio_LL   PP <sub>RATIO_LL</sub>   RDS, SFSW = L,H   0.7   1   1.3   s     Lock detection time_LH   t <sub>LOCK1_LH</sub>   RDS, SFSW = L,H   0.7   1   1.3   s     Lock detection time_LH   t <sub>LOCK1_LH</sub>   RDS, SFSW = L,H   0.7   1   1.3   s     Lock detection time_HH   t <sub>LOCK1_LH</sub>   RDS, SFSW = L,H   9   10   11       Lock detection time_HH   t <sub>LOCK1_LH</sub>   RDS, SFSW = H,H   0.7   1   1.3   s     Lock detection time_HH   t <sub>LOCK1_LH</sub>   RDS, SFSW = H,H   0.35   0.5   0.65   s     Over Current Protection     Over current detection level   V <sub>CL1</sub>     0.225   0.250   0.275   V     SLEEP     Low-level input voltage   V <sub>SLL</sub>       0.5   V     High-level input voltage   V <sub>SLL</sub>       0. 0.3   V     Input impedance   Z <sub>SL</sub>     70   100   130   kΩ		Faranieter	Symbol	Cymber Condition		Тур	Max	Ullit	Note
V <sub>CC</sub> current at sleep mode   I <sub>CCS</sub>   V <sub>SLEEP</sub> = H	Cir	cuit Current		•					
Regulator Block		V <sub>CC</sub> current	I <sub>CC1</sub>	_	3.0	5.6	9.0	mA	_
VREG voltage		V <sub>CC</sub> current at sleep mode	I <sub>CC3</sub>	V <sub>SLEEP</sub> = H	_	_	50	μА	_
Dutput impedance	Re	gulator Block							
FG Block   FG output (low voltage)   V <sub>FSL</sub>   I <sub>FG</sub> = 1.0 mA   — 0.1   0.3   V		VREG voltage	$V_{VREG}$	_	4.7	5	5.3	V	_
FG output (low voltage)		Output impedance	Z <sub>VREG</sub>	$I_{VREG} = -10 \text{ mA}$		_	10	Ω	
RD   Block   RD   output (low voltage)   V <sub>RDL</sub>   I <sub>RD</sub> = 1.0 mA   —   0.1   0.3   V	FG	Block							
RD output (low voltage)		FG output (low voltage)	$V_{FGL}$	I <sub>FG</sub> = 1.0 mA	_	0.1	0.3	V	_
Power Block	RD	Block							
On resistance		RD output (low voltage)	$V_{RDL}$	I <sub>RD</sub> = 1.0 mA	_	0.1	0.3	V	
On resistance (Vcc=4.5V)	Po	wer Block	•						
On resistance (Vcc=4.5V)		On resistance	R <sub>ONHL</sub>	I = 400 mA	0.5	1.0	1.5	Ω	_
		On resistance (Vcc=4.5V)	R <sub>ONHL</sub>		-	1.25	2.05	Ω	-
$ \begin{array}{ c c c c c } \hline Lock \ detection \ time\_LL & t_{LOCK1\_LL} & RDS, \ SFSW = L,L & 0.35 & 0.5 & 0.65 & s \\ \hline Lock \ release \ time\_LL & t_{LOCK2\_LL} & RDS, \ SFSW = L,L & 3.5 & 5 & 6.5 & s \\ \hline Lock \ protection \ ratio\_LL & PR_{RATIO\_LL} & RDS, \ SFSW = L,L & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_LH & t_{LOCK1\_LH} & RDS, \ SFSW = L,H & 0.7 & 1 & 1.3 & s \\ \hline Lock \ release \ time\_LH & t_{LOCK1\_LH} & RDS, \ SFSW = L,H & 7 & 10 & 13 & s \\ \hline Lock \ protection \ ratio\_LH & PR_{RATIO\_LH} & RDS, \ SFSW = L,H & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_HL & t_{LOCK1\_HL} & RDS, \ SFSW = H,L & 1.4 & 2 & 2.6 & s \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HL} & RDS, \ SFSW = H,L & 1.4 & 2 & 2.6 & s \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HH} & RDS, \ SFSW = H,H & 0.35 & 0.5 & 0.65 & s \\ \hline \hline \textbf{Over Current Protection} & \hline \textbf{Over current detection level} & V_{CL1} & & 0.225 & 0.250 & 0.275 & V \\ \hline \textbf{SLEEP} & \hline Low-level \ input \ voltage & V_{SLL} & & & 0.5 & V \\ \hline High-level \ input \ voltage & V_{SLL} & & & 0.5 & V \\ \hline \ Open-circuit \ voltage & V_{SLZ} & & & 0 & 0.3 & V \\ \hline \ Input \ impedance & Z_{SL} & & 70 & 100 & 130 & k\Omega \\ \hline \end{array}$		Diode forward voltage	V <sub>DI</sub>	I = 400 mA	0.6	0.8	1	V	_
$ \begin{array}{ c c c c c } \hline Lock \ release \ time\_LL & t_{LOCK2\_LL} & RDS, \ SFSW = L, L & 3.5 & 5 & 6.5 & s \\ \hline Lock \ protection \ ratio\_LL & PR_{RATIO\_LL} & RDS, \ SFSW = L, L & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_LH & t_{LOCK1\_LH} & RDS, \ SFSW = L, H & 0.7 & 1 & 1.3 & s \\ \hline Lock \ release \ time\_LH & t_{LOCK2\_LH} & RDS, \ SFSW = L, H & 7 & 10 & 13 & s \\ \hline Lock \ protection \ ratio\_LH & PR_{RATIO\_LH} & RDS, \ SFSW = L, H & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_HL & t_{LOCK1\_HL} & RDS, \ SFSW = H, L & 1.4 & 2 & 2.6 & s \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HH} & RDS, \ SFSW = H, H & 0.35 & 0.5 & 0.65 & s \\ \hline \hline \textbf{Over Current Protection} & & & & & & & & \\ \hline \textbf{Over \ Current Protection} & & & & & & & & & \\ \hline \textbf{SLEEP} & & & & & & & & & & & \\ \hline Low-level \ input \ voltage & V_{SLL} & & & 0.5 & V & \\ \hline High-level \ input \ voltage & V_{SLZ} & & & V & \\ \hline Open-circuit \ voltage & V_{SLZ} & & & 0 & 0.3 & V & \\ \hline Input \ impedance & Z_{SL} & & 70 & 100 & 130 & k\Omega \\ \hline \end{array}$	Мо	tor Lock Protection			•				
$ \begin{array}{ c c c c c } \hline Lock \ release \ time\_LL & t_{LOCK2\_LL} & RDS, \ SFSW = L, L & 3.5 & 5 & 6.5 & s \\ \hline Lock \ protection \ ratio\_LL & PR_{RATIO\_LL} & RDS, \ SFSW = L, L & 9 & 10 & 11 & & 1 \\ \hline Lock \ detection \ time\_LH & t_{LOCK1\_LH} & RDS, \ SFSW = L, H & 0.7 & 1 & 1.3 & s & 1 \\ \hline Lock \ release \ time\_LH & t_{LOCK2\_LH} & RDS, \ SFSW = L, H & 7 & 10 & 13 & s & 1 \\ \hline Lock \ protection \ ratio\_LH & PR_{RATIO\_H} & RDS, \ SFSW = L, H & 9 & 10 & 11 & & 1 \\ \hline Lock \ detection \ time\_HL & t_{LOCK1\_HL} & RDS, \ SFSW = H, L & 1.4 & 2 & 2.6 & s & 1 \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HL} & RDS, \ SFSW = H, H & 0.35 & 0.5 & 0.65 & s & 1 \\ \hline \hline \textbf{Over \ Current \ Protection} & V_{CL1} & & 0.225 & 0.250 & 0.275 & V & 1 \\ \hline \textbf{SLEEP} & Low-level \ input \ voltage & V_{SLL} & & & 0.5 & V & 1 \\ \hline High-level \ input \ voltage & V_{SLL} & & & 0.5 & V & 1 \\ \hline Open-circuit \ voltage & V_{SLZ} & & & 0 & 0.3 & V & 1 \\ \hline Input \ impedance & Z_{SL} & & 70 & 100 & 130 & k\Omega & 1 \\ \hline \end{array}$		Lock detection time_LL	t <sub>LOCK1_LL</sub>	RDS, SFSW = L,L	0.35	0.5	0.65	s	_
$ \begin{array}{ c c c c c c } \hline Lock \ detection \ time\_LH & t_{LOCK1\_LH} & RDS, SFSW = L,H & 0.7 & 1 & 1.3 & s \\ \hline Lock \ release \ time\_LH & t_{LOCK2\_LH} & RDS, SFSW = L,H & 7 & 10 & 13 & s \\ \hline Lock \ protection \ ratio\_LH & PR_{RATIO\_LH} & RDS, SFSW = L,H & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_HL & t_{LOCK1\_HL} & RDS, SFSW = H,L & 1.4 & 2 & 2.6 & s \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HH} & RDS, SFSW = H,H & 0.35 & 0.5 & 0.65 & s \\ \hline \hline \textbf{Over Current Protection} \\ \hline \hline Over \ current \ detection \ level & V_{CL1} & & 0.225 & 0.250 & 0.275 & V \\ \hline \textbf{SLEEP} \\ \hline Low-level \ input \ voltage & V_{SLL} & & & 0.5 & V \\ \hline High-level \ input \ voltage & V_{SLH} & & 2.5 & & & V \\ \hline Open-circuit \ voltage & V_{SLZ} & & & 0 & 0.3 & V \\ \hline Input \ impedance & Z_{SL} & & 70 & 100 & 130 & k\Omega \\ \hline \end{array}$		Lock release time_LL		RDS, SFSW = L,L	3.5	5	6.5	s	_
$ \begin{array}{ c c c c c c } \hline Lock \ detection \ time\_LH & t_{LOCK1\_LH} & RDS, SFSW = L,H & 0.7 & 1 & 1.3 & s \\ \hline Lock \ release \ time\_LH & t_{LOCK2\_LH} & RDS, SFSW = L,H & 7 & 10 & 13 & s \\ \hline Lock \ protection \ ratio\_LH & PR_{RATIO\_LH} & RDS, SFSW = L,H & 9 & 10 & 11 & \\ \hline Lock \ detection \ time\_HL & t_{LOCK1\_HL} & RDS, SFSW = H,L & 1.4 & 2 & 2.6 & s \\ \hline Lock \ detection \ time\_HH & t_{LOCK1\_HH} & RDS, SFSW = H,H & 0.35 & 0.5 & 0.65 & s \\ \hline \hline \textbf{Over Current Protection} \\ \hline \hline \textbf{Over current detection level} & \textbf{V}_{CL1} & & 0.225 & 0.250 & 0.275 & \textbf{V} \\ \hline \textbf{SLEEP} \\ \hline Low-level \ input \ voltage & \textbf{V}_{SLL} & & & 0.5 & \textbf{V} \\ \hline High-level \ input \ voltage & \textbf{V}_{SLJ} & & & 0 & 0.3 & \textbf{V} \\ \hline Open-circuit \ voltage & \textbf{V}_{SLZ} & & & 0 & 0.3 & \textbf{V} \\ \hline Input \ impedance & \textbf{Z}_{SL} & & 70 & 100 & 130 & k\Omega \\ \hline \end{array}$		Lock protection ratio_LL	PR <sub>RATIO_LL</sub>	RDS, SFSW = L,L	9	10	11	_	_
		Lock detection time_LH		RDS, SFSW = L,H	0.7	1	1.3	s	_
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		Lock release time_LH		RDS, SFSW = L,H	7	10	13	s	_
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		Lock protection ratio_LH		RDS, SFSW = L,H	9	10	11	_	_
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		Lock detection time_HL		RDS, SFSW = H,L	1.4	2	2.6	s	*1
		Lock detection time_HH		RDS, SFSW = H,H	0.35	0.5	0.65	s	*2
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Ov	er Current Protection	•						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Over current detection level	er current detection level V <sub>CL1</sub> —		0.225	0.250	0.275	V	_
High-level input voltage $V_{SLH}$ —2.5—VOpen-circuit voltage $V_{SLZ}$ ——00.3VInput impedance $Z_{SL}$ —70100130kΩ	SL	EEP		!					
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Low-level input voltage	V <sub>SLL</sub>	_	_	_	0.5	V	—
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		High-level input voltage	V <sub>SLH</sub>	_	2.5	_	_	V	_
	Open-circuit voltage			_		0	0.3	V	
Internal Oscillation Frequency		Input impedance	Z <sub>SL</sub>	_	70	100	130	kΩ	
	Inte	ernal Oscillation Frequency	<u> </u>						
Internal oscillation frequency f <sub>OSC</sub> — 17.5 25 32.5 MHz -		Internal oscillation frequency	f <sub>OSC</sub>	_	17.5	25	32.5	MHz	_

Note: \*1:Motor Lock Protection is released immediately by UVLO signal input and SLEEP signal input. \*2: Motor Lock Protection automatically resets immediately(after 70us elapses).

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### **ELECTRICAL CHARACTERISTICS (Continued)**

 $V_{\rm CC}$  = 12.0 V,  $V_{\rm VREG}$  = 5.0 V

Note:  $T_a = 25^{\circ}C \pm 2^{\circ}C$  unless otherwise noted.

Parameter	Symbol	Condition		Limits		Unit	Note
Parameter	Symbol	Symbol		Тур	Max	Unit	Note
VSP			_				
Pin current	I <sub>VSP</sub>	V <sub>VSP</sub> =5.0V	-	15	45	μΑ	
VSP DC Input Control							
Stop control VSP input	V <sub>VSPDCL</sub>	_	0.9	1.0	1.1	<b>V</b>	_
Max. speed VSP input	V <sub>VSPDCH</sub>	_	3.6	4.0	4.4	>	_
VSP PWM Input Control							
Stop control VSP input	V <sub>VSPPWML</sub>	V <sub>VREG</sub> =V <sub>OSC</sub> =5.0V	2	3	4	%	*1,*2
Max. speed VSP input	V <sub>VSPPWMH</sub>	V <sub>VREG</sub> =V <sub>OSC</sub> =5.0V	-	100	-	%	*1,*4
Low-level input voltage during PWM input	V <sub>VSPLL</sub>	V <sub>VREG</sub> =V <sub>OSC</sub> =5.0V	-	ı	1.0	<b>V</b>	*1
High-level input voltage during PWM input	V <sub>VSPHL</sub>	V <sub>VREG</sub> =V <sub>OSC</sub> =5.0V	2.0	ı	-	>	*1
PWM input frequency range	F <sub>PWM</sub>	-	15	-	100	kHz	*1
Triangle Wave Oscillator for PWM Wav	veform (TRI	pin)					
Amplitude	V <sub>TRI</sub>	_	1.36	1.53	1.70	Vpp	_
External capacitor charging current	I <sub>TRI1</sub>	V <sub>TRI</sub> =0.5V	- 83.5	- 64.5	- 45.5	μΑ	_
External capacitor discharging current	I <sub>TRI2</sub>	V <sub>TRI</sub> =2.0V	45.5	64.5	83.5	μΑ	_
TRI pin input voltage during PWM control	V <sub>TRITH</sub>	_	2.9	ı	-	>	*1
Triangle Wave Oscillator during Soft S	start (SST pi	n)	-				
Amplitude	V <sub>SST</sub>	_	0.75	1.0	1.25	Vpp	_
External capacitor charging current	I <sub>SST1</sub>	V <sub>SST</sub> =0.6V	- 6.0	- 4.0	- 2.0	μА	_
External capacitor discharging current	I <sub>SST2</sub>	V <sub>SST</sub> =1.6V	2.0	4.0	6.0	μΑ	_
SST pin input voltage when Soft Start not used	V <sub>SSTTH</sub>	_	2.9	-	-	٧	*3
Hall Block			•		•		
Input dynamic range	V <sub>HALL</sub>	_	0	_	VREG -2.0V	V	_
Pin current	I <sub>HALL</sub>	_	-2	0	2	μА	
Input offset voltage for H1H - H1L drop	V <sub>HOFS</sub>	_	-6	0	6	mV	_
Min. input amplitude voltage	V <sub>HA</sub>	_	25	_	_	mV	_
Hysteresis width	V <sub>HHYS</sub>	_	7.5	10	13	mV	_

Note: \*1: During PWM control setting, TRI pin must be connected to VREG pin.

<sup>\*2:</sup> It is recommended to input 0% Duty (Low input) when input STOP.

<sup>\*3:</sup> When Soft Start is not in used, SST pin must be connected to VREG pin.

<sup>\*4:</sup> Typical Design Value.

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### **ELECTRICAL CHARACTERISTICS (Continued)**

 $V_{CC}$  = 12.0 V,  $V_{VREG}$  = 5.0 V

Note:  $T_a = 25^{\circ}C \pm 2^{\circ}C$  unless otherwise noted.

Parameter	Symbol	Condition		Limits			
Parameter	Symbol	Condition	Min	Тур	Max	Unit	NOTE
FR (3-State Input circuit)							
Low-level input voltage	$V_{FRL}$	_		_	0.8	V	_
Mid-level input voltage	$V_{FRM}$	_	1.3	_	2.0	V	_
High-level input voltage	$V_{FRH}$	_	2.5	_	_	V	_
Open-circuit voltage	$V_{FRZ}$	_	1.4	1.65	1.9	V	_
Pin current	I <sub>INFR</sub>	V <sub>FR</sub> = 0 V	- 40	- 20	_	μА	_
FGSEL (3-State Input circuit)						-	
Low-level input voltage	$V_{FGSELL}$	_		_	1.0	V	_
High-level input voltage	V <sub>FGSELH</sub>	_	4.0	_	_	V	*1
Open-circuit voltage	V <sub>FGSELZ</sub>	_	1.8	2.4	2.8	V	*2
Pin current	I <sub>INFG</sub>	V <sub>FGSEL</sub> = 0 V	- 40	- 20	_	μА	_
PS (2-State Input circuit)				•			•
Low-level input voltage	V <sub>PSL</sub>	_		_	1.0	V	_
High-level input voltage	V <sub>PSH</sub>	_	4.0	_	_	V	*1
Open-circuit voltage	V <sub>PSZ</sub>	_	_	0.0	0.5	V	_
Pin current	I <sub>INPS</sub>	V <sub>PS</sub> = 5.0 V		5	15	μА	_
RDS (2-State Input circuit)	•		•	•	•		
Low-level input voltage	V <sub>RDSL</sub>	_		_	1.0	V	_
High-level input voltage	V <sub>RDSH</sub>	_	4.0	_	_	V	*1
Open-circuit voltage	$V_{RDSZ}$	_	_	0.0	0.5	V	_
Pin current	I <sub>INRDS</sub>	V <sub>RDS</sub> = 5.0 V	_	5	15	μА	_
OVS (2-State Input circuit)	•	•	•	•	•		•
Low-level input voltage	V <sub>ovsl</sub>	_		_	1.0	V	_
High-level input voltage	V <sub>OVSH</sub>	_	4.0	_	_	V	*1
Open-circuit voltage	V <sub>OVSZ</sub>	_	-	0.0	0.5	V	_
Pin current	I <sub>INOVS</sub>	V <sub>OVS</sub> = 5.0 V	-	5	15	μА	_
SFSW (2-State Input circuit)	'			•	•	•	•
Low-level input voltage	$V_{SFSWL}$	_		_	1.0	V	_
High-level input voltage	V <sub>SFSWH</sub>	_	4.0	_	_	V	*1
Open-circuit voltage	V <sub>SFSWZ</sub>	_	<u> </u>	0.0	0.5	V	_
Pin current	I <sub>INSFSW</sub>	V <sub>SFSW</sub> = 5.0 V	T —	5	15	μА	_

Note: \*1: During High level setting, please ensure to connect to VREG pin.

<sup>\*2:</sup> Please connect a capacitor to FGSEL pin when it is open during use to prevent noise. To ensure the noise prevention, please perform sufficient evaluation and verification.

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### **ELECTRICAL CHARACTERISTICS (Continued)**

 $V_{\rm CC}$  = 12.0 V,  $V_{\rm VREG}$  = 5.0 V

Note:  $T_a = 25^{\circ}C \pm 2^{\circ}C$  unless otherwise noted.

Parameter		Cumbal	Condition	Design value			Unit	Note	
	Parameter	Symbol	Condition	Min	Тур	Max	Unit	Note	
Thern	mal Protection								
Р	rotection operating temperature	TSD <sub>ON</sub>	_	_	160	_	°C	*1	
Н	lysteresis width	TSD <sub>HYS</sub>	_	_	25	_	°C	*1	
Outp	ut Block								
o	Output slew rate at source current	$V_{TRSO}$	_	_	300	_	V/μs	*1	
O	Output slew rate at source current	$V_{TFSO}$	_	_	300	_	V/μs	*1	
0	Output slew rate at sink current	$V_{TRSI}$	_	_	300	_	V/μs	*1	
O	Output slew rate at sink current	$V_{TFSI}$	_	_	300	_	V/μs	*1	
Trian	gle Wave Oscillator for PWM Wav	eform (TRI	pin)		•				
0	Scillation frequency range	f <sub>TRI</sub>	_	15	-	100	kHz	*2	
s	tandard oscillation frequency	F <sub>TRI</sub>	C <sub>TRI</sub> = 390 pF	_	55.4	_	kHz	*1	
Trian	gle Wave Oscillator during Soft S	tart (SST pi	n)		!				
s	tandard oscillation frequency	F <sub>SST</sub>	C <sub>SST</sub> = 1800 pF	_	1.13	_	kHz	*1	
Maxir	num Rotating Speed				•				
N	1inimum hall cycle	T <sub>HMIN</sub>	_	_	173	_	μS	*1	
Unde	r Voltage Lock Out				•		•		
Р	rotection operating voltage	$V_{LVON}$	_	_	3.55	_	V	*1	
Р	rotection release voltage	$V_{LVOFF}$	_	_	3.75		V	*1	
Over Voltage Lock Out									
Р	Protection operating voltage 1		V <sub>OVS</sub> = VREG	15.0	16.0	17.0	V	*1	
Р	rotection operating voltage 2	V <sub>OVON2</sub>	V <sub>OVS</sub> = 0V	26.4	27.2	28.0	V	*1	

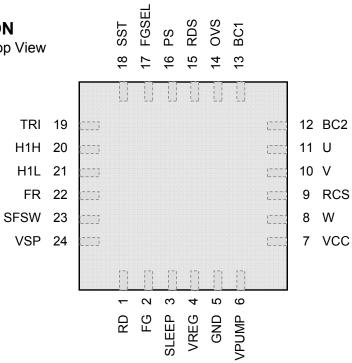
Note: \*1: Typical Design Value.

<sup>\*2:</sup> These are values checked by design but not production tested.

### AN44143A

### PIN CONFIGURATION

Top View



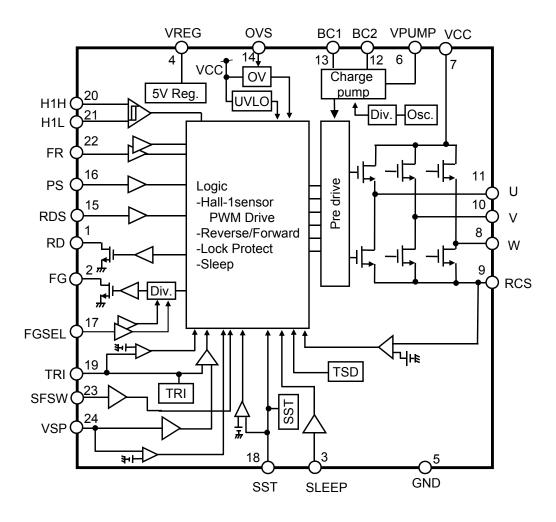
### **PIN FUNCTIONS**

Pin No.	Pin name	Type	Description				
1	RD	Output	Over load protection				
2	FG	Output	FG external output				
3	SLEEP	Input	Sleep setting				
4	VREG	Output	Internal reference voltage				
5	GND	Ground	Ground				
6	VPUMP	Output	Charge pump circuit output				
7	VCC	Power	Supply voltage for motor				
8	W	Output	W-phase output				
9	RCS	Output	Motor current detector				
10	V	Output	V-phase output				
11	U	Output	U-phase output				
12	BC2	Output	Capacitor connection pin 2 for charge pump				
13	BC1	Output	Capacitor connection pin 1 for charge pump				
14	ovs	Input	Over voltage detection selectable threshold. High for 16V detection, Low for 27.2V detection				
15	RDS	Input	Selectable Release of Motor lock protection. High to use the release of lock protection. Low to disable the release of lock protection.				
16	PS	Input	Selectable phase shift mode. High to enable Auto Phase FB shift mode. Low to enable constant phase shift mode.				
17	FGSEL	Input	FG pulse count select				
18	SST	Input / Output	Capacitor connection pin for Soft Start triangle wave oscillator frequency setting				
19	TRI	Input / Output	Capacitor connection pin for PWM triangle wave oscillator frequency setting				
20	H1H	Input	Hall amplifier input (+)				
21	H1L	Input	Hall amplifier input (-)				
22	FR	Input	Rotation direction select (Forward/Reverse)				
23	SFSW	Input	Selectable the start frequency				
24	VSP	Input	Voltage input for setting rotating speed				

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### **FUNCTIONAL BLOCK DIAGRAM**



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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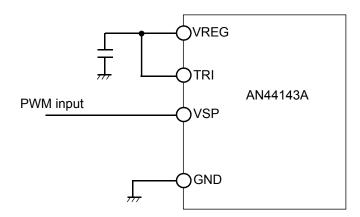
### **OPERATION**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 1. VSP input configuration

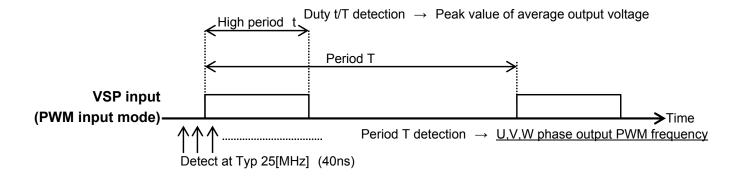
### 1-1. PWM input mode

PWM input control or DC input control are used as the input controls to VSP pin. When using PWM input control, please ensure to connect TRI pin to VREG pin.



#### PWM input control signal detection

The below periodic signal T and Duty signal t/T is detected when PWM is input to VSP pin. Periodic signal T respond to output PWM frequency and Duty signal t/T respond to speed signal.



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### **OPERATION** (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

- 1. VSP input configuration (Continued)
- 1-1. PWM input mode (Continued)

#### Points to note when using PWM input mode

#### Operation when input at VSP=100%duty

During output, when the VSP PWM input duty changes from below 100% to 100% duty, the frequency (period t) that is being input will halt and 100% input will be detected.

Therefore, output frequency will become 1/t. (However, this will be reflected in the output about 7t later, after signal is changed to 100% duty.)

When VSP pin is already input with 100% duty during power or SLEEP start-up, operation is at output frequency of about 58kHz.

After which, when PWM signal is input to the VSP pin and frequency signal is detected, output frequency will follow the frequency that is being input to VSP pin.

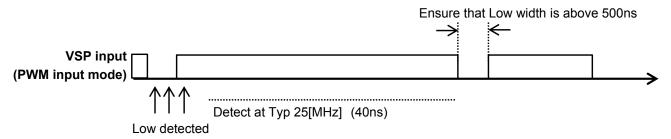
#### Maximum pulse width when VSP below 100% is input

VSP input resolution under PWM input mode is typ 25MHz(40ns period).

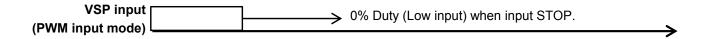
Therefore, input pulse below 40ns may not be detected.

This is especially when input is near to 100% duty, period T signal many not be correctly detected.

Therefore to ensure that normal signal can be detected, please ensure that input to VSP pin at Low is above 500ns and more.



It is recommended to input 0% Duty (Low input) when input STOP.



Under PWM input mode, please ensure that PWM signal is input to the VSP pin.

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### **OPERATION (Continued)**

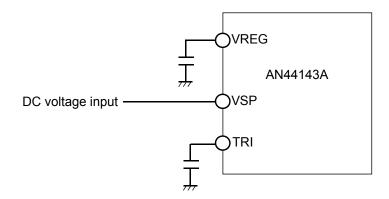
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 1. VSP input configuration (Continued)

#### 1-2. VSP input mode

PWM input control or DC input control are used as the input controls to VSP pin.

When using DC input control, please ensure to connect a capacitor between TRI pin and GND pin.



Signal during DC input mode

During DC input mode, PWM signal is generated by the comparison between the TRI pin triangle waveform and the VSP pin input DC voltage.

Peak value of average output voltage is dependent on VSP pin voltage and output PWM frequency is dependent on TRI pin triangle waveform frequency.

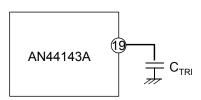
### TRI pin triangle wave oscillator frequency

The triangle wave oscillator frequency input into TRI pin is calculated using the below formula.

Triangle wave oscillator frequency  $f_{TRI} = \frac{A}{2 \times C_{TRI} \times V_{TRI}}$ 

 $V_{TRI}$ : Triangle waveform amplitude (Under typ.1.53 V)

A : 64.5 μA (Under typ.)



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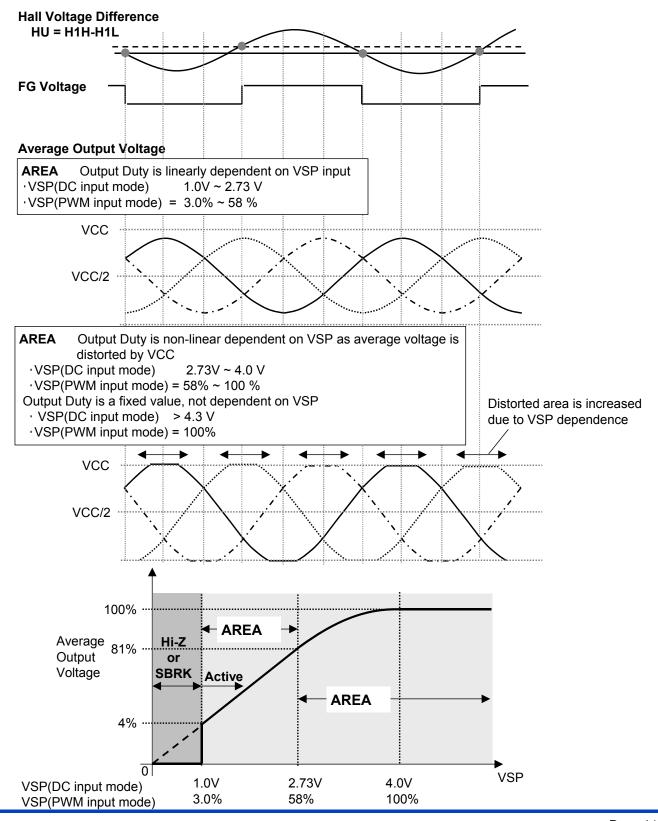
Revised

: ####-##-##

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 2. VSP input voltage and average output voltage

Values in this page are all Typ values. In addition, these are where our recommended TRI value is used, under DC input mode.

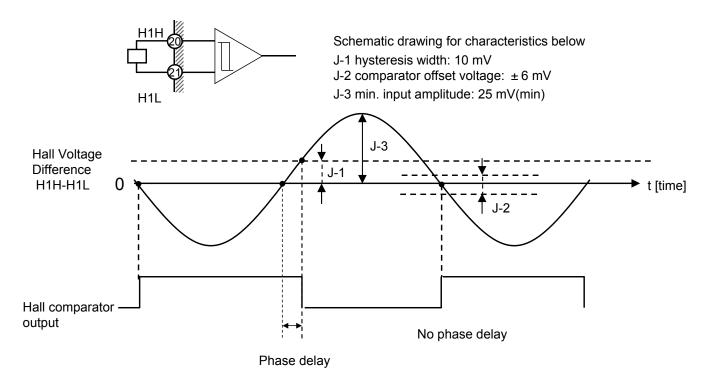


Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

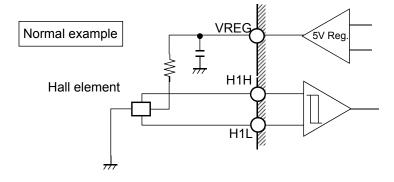
### 3. Hall Input Specification

### 3-1. System to detect hall signal

The motor position is detected by the Hall hysteresis comparator. If the amplitude of sine wave is small, phase delay of comparator output will be very prominent. Therefore, please make the amplitude of the sine wave larger. When chattering occurs to Hall element, insert a capacitor between H1H (pin 20) and H1L (pin 21).



For the biased source of the Hall element, please construct by externally shorting to VREG pin.



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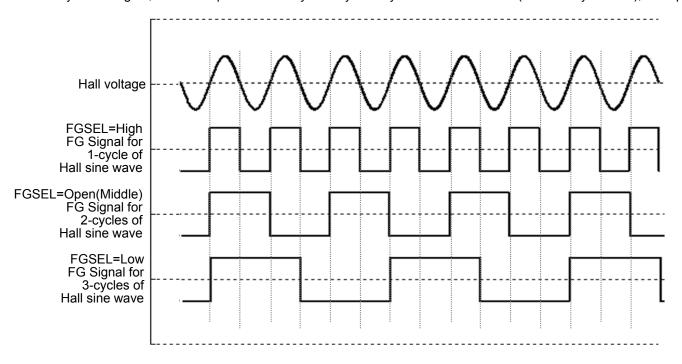
### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 3. Hall Input Specification (Continued)

### 3-2. The Relation between Hall Voltage and FGSEL

1-cycle FG signal, which is equivalent to 1-cycle/2-cycle/3-cycle of Hall sine wave (selected by FGSEL), is output.



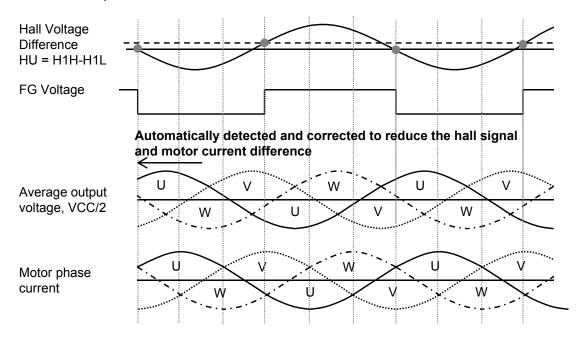
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 3. Hall Input Specification (Continued)

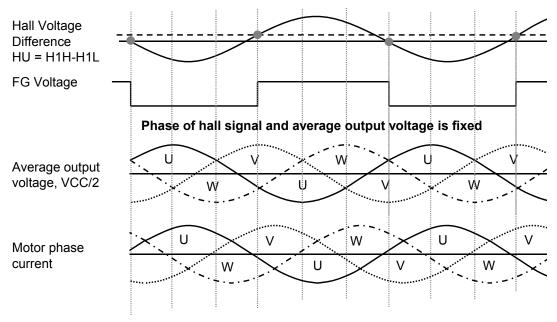
#### 3-3. Drive Phase Shift Control

Automatic drive phase shift control when PS=Low. The hall signal phase with respect to the conduction angle detects the IC's own phase difference and automatically correct it to the most optimum phase. The example for U-phase output voltage is shown below.

### Automatic drive phase shift control when PS=Low



### Fixed to 0 deg when PS=High



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### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

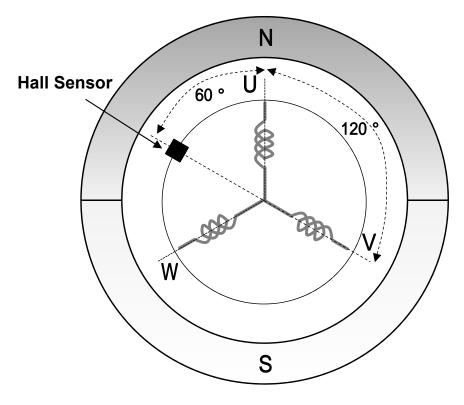
### 3. Hall Input Specification (Continued)

### 3-4. Hall Sensor Placement

This IC uses only 1 hall sensor.

Please use the U-phase hall sensor for 3 phase 3 sensor motor

The diagram below shows the hall placement for a 2 pole 3 slots motor



Example placement for the hall sensor (2 pole 3 slot motor)

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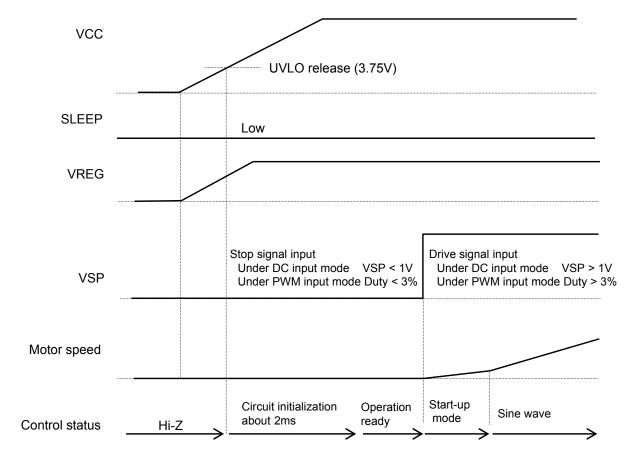
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### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 4. Start / Stop control

Start-up by rising VCC pin voltage



- · After UVLO is released, circuit initialization is required for about 2ms and output signal is stopped. When circuit is under initialization, no signal is output even when VSP drive signal is inputted. Output of signal starts after initialization completes.
- ·Start up mode is within 4 cycles hall signal input. During this period, no FG signal is output.

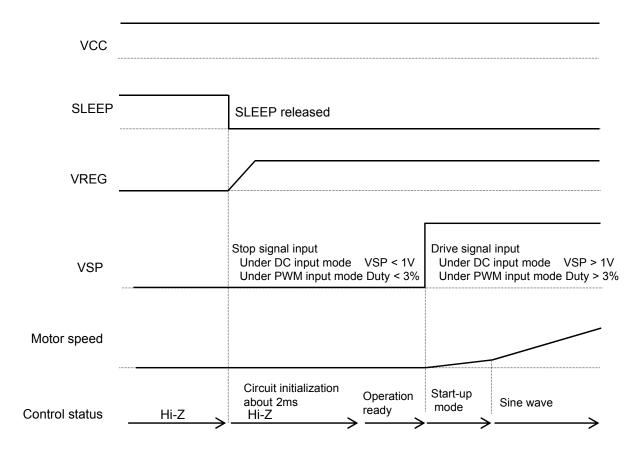
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### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 4. Start / Stop control (Continued)

Start-up by SLEEP signal release



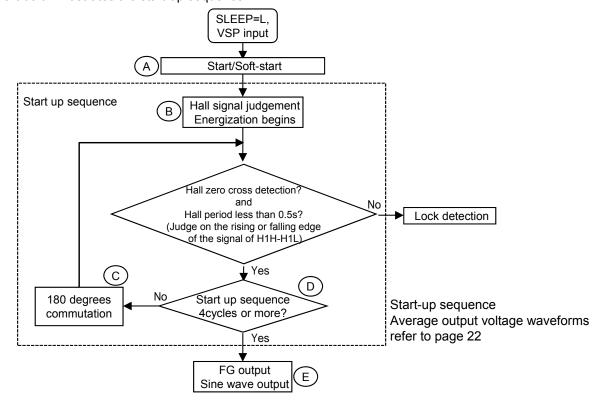
- · After SLEEP mode is released, circuit initialization is required for about 2ms and output signal is stopped. When circuit is under initialization, no signal is output even when VSP drive signal is inputted. Output of signal starts after initialization completes.
- ·Start up mode is within 4 cycles hall signal input. During this period, no FG signal is output.

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

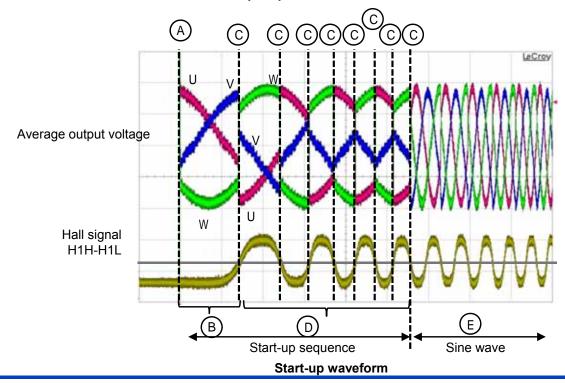
### 4. Start / Stop control (Continued)

#### Start-up sequence

The flow chart below illustrates the start-up sequence.



### Start-up sequence flow chart



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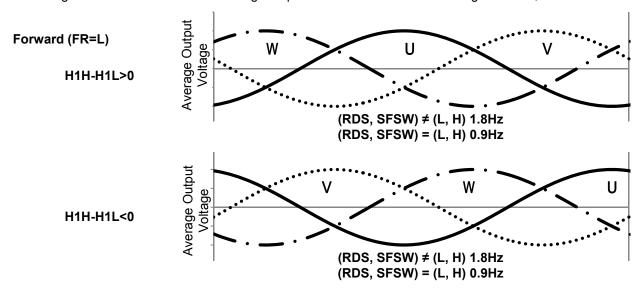
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 4. Start / Stop control (Continued)

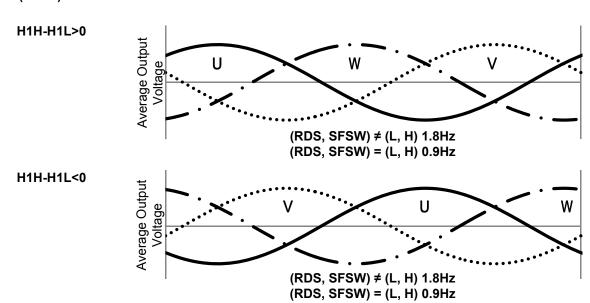
#### Start-up sequence (Continued)

#### Start-up sequence average output voltage.

The following waveforms illustrates the average output for different hall zero crossing detection, H1H-H1L at start-up.



#### Reverse (FR=H)



Due to the initial position of the rotor, the starting torque differs slightly during start-up. For motor type
that requires large inertia force to turn, please ensure that sufficient starting current is available for the
motor. Please perform sufficient testing and evaluations to ensure this.

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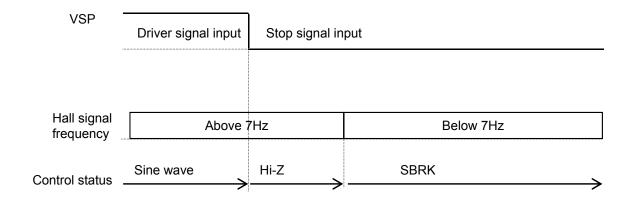
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### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 4. Start / Stop control (Continued)

### Stop

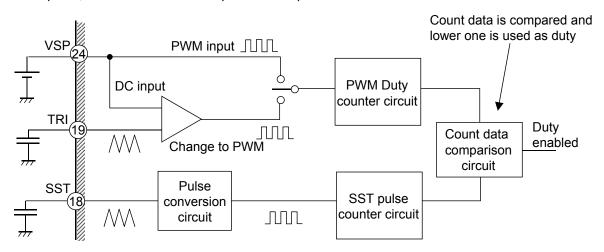


<sup>·</sup>When stop signal is input to VSP, hall signal frequency above 7Hz will result in Hi-Z at output and below 7Hz will result in SBRK at output.

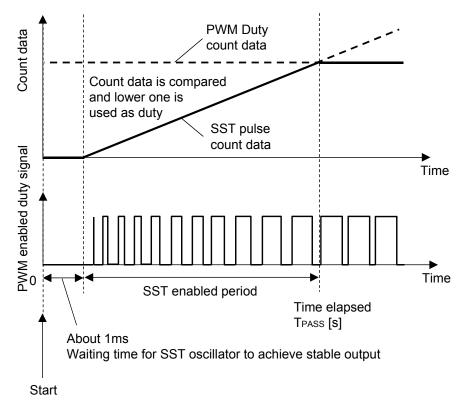
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 5. Soft Start Function and PWM Specification

By connecting a capacitor to the SST pin, soft start control is performed by the start-up mode conditions during the mode transition. The period for soft start control is determined by the formula shown on the next page. When soft start control is not required, ensure to connect SST pin to VREG pin.



Below shows the correlation timing chart of count data and PWM enabled duty for VSP and SST.



<sup>·</sup>Notes on the use of the soft-start function.

With the increase in soft-start time, the motor current will also increase slowly . Therefore if the soft-start timing is too long, it will result in the motor not having enough starting torque and lock protection detection will be triggered if soft start timing is more than 0.5s (typ). This will cause the motor to be unable to start. Please evaluate and check this condition thoroughly when using this function.

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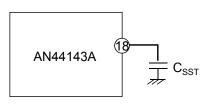
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 5. Soft Start Function and PWM Specification (Continued)

The triangle wave oscillator frequency output by SST pin is determined by the below formula. Soft Start timing is generated by comparing the VSP pin input PWM frequency and this triangle waveform frequency.

Triangle wave oscillator frequency 
$$f_{SST} = \frac{A}{2 \times C_{SST} \times V_{SST}}$$

 $V_{\text{SST}}\,$  : Triangle waveform amplitude (At typ. 1 V) : Current flowing in/out SST pin (At typ. 4 µA)



The PWM enabled duty reflected in the output, at the time elapsed T<sub>PASS</sub> within the SST enabled timing is determined by the below formula:

$$PWM \ duty = \frac{T_{PASS} \times T_{OSC}}{T_{SST} \times T_{PWM}} \qquad \begin{array}{c} T_{PWM} : \text{Input PWM cycle [s]} \\ T_{OSC} : \text{Oscillation cycle of internal oscillator} \\ 40*10^{-9} \ [s] \\ T_{SST} : SST \ triangle \ wave \ oscillation \ cycle[s] \end{array}$$

T<sub>PASS</sub>: Time elapsed [s]

T<sub>PASS</sub> at the end of the SST timing can be determined by the below formula:

$$T_{PASS} = \frac{T_{PWM} \times D \times T_{SST}}{T_{OSC}}$$
 D : Input PWM duty [%]

Input PWM duty during the DC input can be determined by the below formula:

D = 
$$\left(\frac{97}{3} \times V_{VSP} - \frac{88}{3}\right) \times 0.01$$
 Under DC input,  $V_{VSP} = 1V \sim 4V$ 

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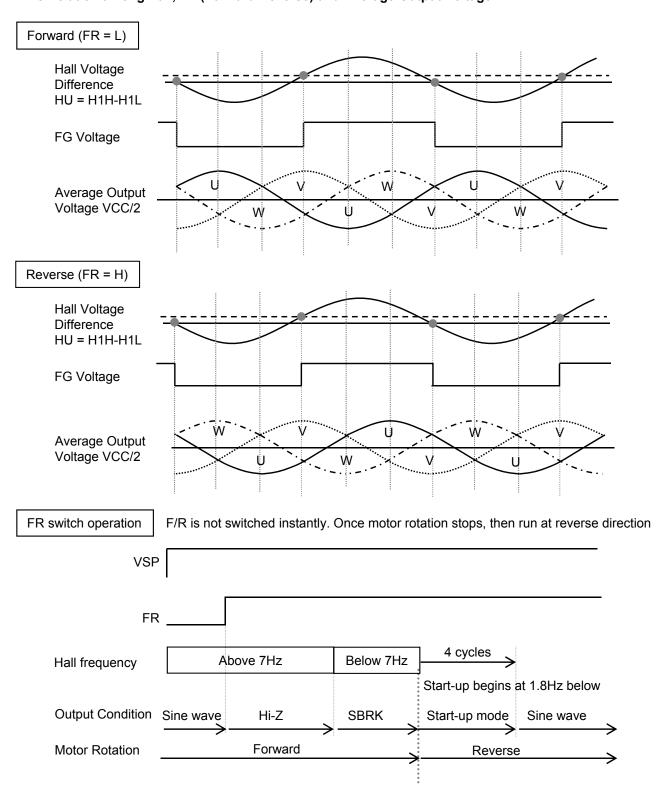
Established: 2015-07-28

### **OPERATION** (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 6. Forward, Reverse and Short-break

The Relation among Hall, FR (Forward/Reverse) and Average Output Voltage



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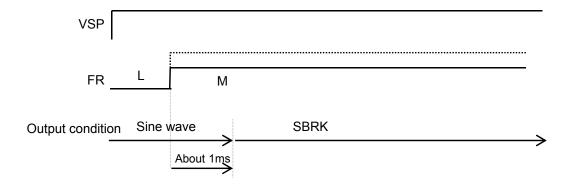
### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 6. Forward, Reverse and Short-break (Continued)

**Short-break mode** 

Changes to short-break mode when FR=M.



Short-break may generate very large motor current. Please perform sufficient evaluation and verification to ensure that it does not exceed the absolute maximum ratings.

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### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 7. SLEEP Mode

Sleep mode is used to reduce power consumption.

	Enter the Mode	Motor Output	VREG Voltage	Exit the Mode
SLEEP SLEEP pin: H	Sleep pin: $L \Rightarrow H$ (Immediate)	All phase OFF	OFF	Sleep pin: H ⇒ L

In SLEEP mode, VREG voltage is OFF and all circuit protections cease to operate.

When SLEEP pin is changed from "L" to "H" while motor is running at high speed, please ensure that motor regenerated current, etc. does not exceed the absolute maximum rating of each pin and perform sufficient evaluation and verification to ensure this.

### Panasonic \_\_\_\_\_

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### **OPERATION** (Continued)

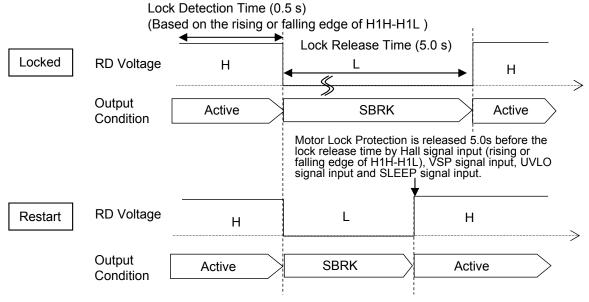
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

#### 8. Protection Functions

### 8-1. Motor Lock Protection

#### When RDS=L, SFSW=L or H (Automatic reset mode)

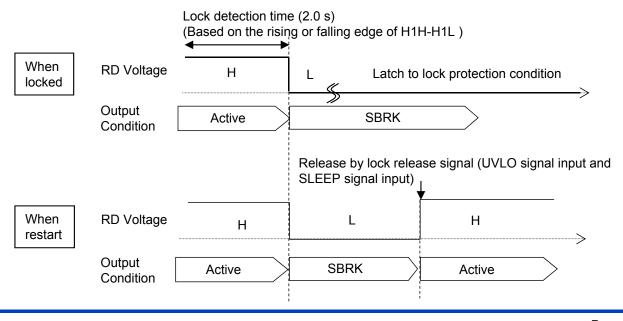
When no signal for Hall signal input (Based on the rising or falling edge of H1H-H1L) is continued for 0.5s(SFSW=L) or 1.0s(SFSW=H) or more, motor output turns OFF (short-brake) and Motor Lock Protection starts working (RD = L), and automatically resets after 5s(SFSW=L) or 10s(SFSW=H) elapses. Motor Lock Protection is released immediately by Hall signal input (rising or falling edge of H1H-H1L), VSP signal input, UVLO signal input and SLEEP signal input.



Note).Lock detection and release time of the upper diagram is in the case of RDS = L, SFSW=L

### When RDS=H, SFSW=L (Latch mode)

When there is no hall signal (Based on the rising or falling edge of H1H-H1L) for more than 2.0s, motor output will be OFF (Short-break), operation will switch and latch to RD=L protection. UVLO signal input and SLEEP signal input will immediately release the protection.



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### **OPERATION** (Continued)

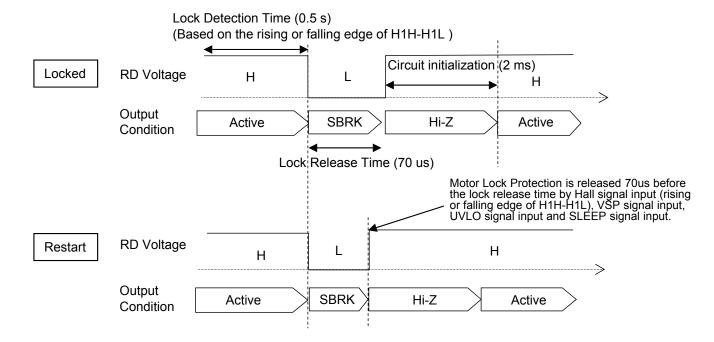
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

#### 8. Protection Functions

#### 8-1. Motor Lock Protection (Continued)

#### When RDS=H, SFSW=H (Immediately reset mode)

When no signal for Hall signal input (Based on the rising or falling edge of H1H-H1L) is continued for 0.5s or more, Motor Lock Protection immediately resets(after 70us elapses). Motor Lock Protection is released immediately by Hall signal input (rising or falling edge of H1H-H1L), VSP signal input, UVLO signal input and SLEEP signal input.



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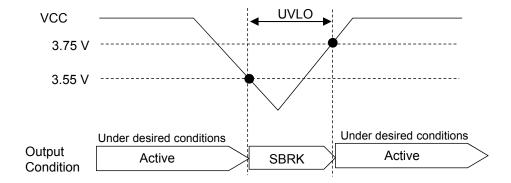
### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 8. Protection Functions

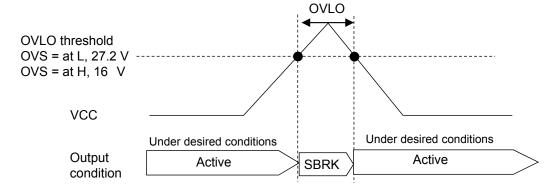
#### 8-2. Under Voltage Lock Out (UVLO)

When VCC voltage drops to 3.55V and below, UVLO activates and motor output enters short-brake mode. When VCC voltage increases to 3.75V and above, UVLO is released.



#### 8-3. Over Voltage Lock Out (OVLO)

When VCC voltage increases above threshold, OVLO activates and motor output enters short-brake mode. When VCC voltage drops below threshold, OVLO is released.

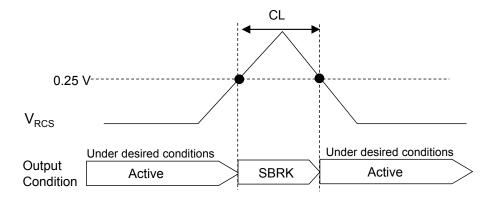


Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 8. Protection Functions

#### 8-4. Over Current Protection (CL)

When RCS voltage increases to 0.25 V and above, OCP starts working and motor output enters short-brake mode. When RCS voltage decreases to 0.25 V and below, OCP is released.



Current value for over current detection can be set by varying the RCS pin detection resistor (RCS).

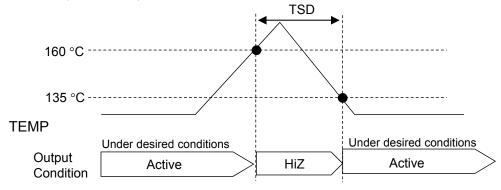
Over current protection current detection value 
$$I_{PEAK} = 0.250V \times \frac{1}{RCS}$$

Eg:  $I_{PEAK}$  = To set to 1.0 A, set RCS to 0.250  $\Omega$  based on the below formula.

$$RCS = 0.250(V) \times \frac{1}{1.00(A)} = 0.250()$$

### 8-5. Thermal Shut Down (TSD)

When IC junction temperature increases to 160 and above, TSD activates and motor output turns OFF. When IC junction temperature drops to 135 and below, TSD is released.



### **AN44143A**

### **OPERATION (Continued)**

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

### 9. Control mode Table

Pin	Pin	Des	- ulus 4! -	_			Voltage			Domining		
No.	Name	Des	criptio	n	Ope	n (Low	)	High		Remarks		
3	SLEEP	Sleep mod	e selec	rt	N	ormal		Sleep		SLEEP = "H" : Sleep mode (Motor output: OFF, VREG output: OFF) SLEEP = "L" : Normal mode  Note) For the setting range of SLEEP control voltage, refer to "SLEEP" under Electrical Characteristics on page 5.		
14	ovs	OVP Thres	hold se	elect	2	7.2V		16V		Note: Please connect to VREG pin when set to High.		
16	PS	Phase Shif	Phase Shift mode select		,	Auto	С	onsta	nt	Note: Please connect to VREG pin when set to High.  Note: Do not switch during motor driving.		
18	SST	for Soft Sta	apacitor connection pin r Soft Start triangle ave oscillator frequency			-		Soft start control not in use		When soft start control is not in used, please connect SST pin to VREG pin. When soft start control is in used, please connect a capacitor to SST pin.		
19	TRI	for PWM tr	pacitor connec PWM triangle cillator frequend ting		-		PWM input control			When PWM input is used in speed control, please connect TRI pin to VREG pin. When DC input is used in speed control, please connect a capacitor to TRI pin.		
Din							Voltage					
Pin No.	Pin Name	Des	criptio	n	Lo	w	Open (Middle)	н	igh	Remarks		
22	FR	Rotation di (Forward/R Short-brake	everse	<del>:</del> )	Forw	/ard	Short- brake	Rev	verse	Arbitrary direction is denoted as "Forward", and reverse direction is denoted as "Reverse".  Note) For the setting range of FR control voltage, refer to "FR" under Electrical Characteristics on page 7.		
17	FGSEL		oulse count select o of hall signal cycle		1/	3	1/2	1/2		FG pulse output which is equivalent to arbitrary magnification of hall signal cycle  Note) For set range of FGSEL control voltage, refer to "FGSEL" of the Electrical Characteristics on page 7		
Pin No 15 Pin Nam RDS	Pin No 23 e Pin Na SFSW	Frequ ime [Hz]	necy	Lock Detection Time [s]	on R	ock elease ime s]	Auto reset		Rema	irks		
Low	Low	1.8		0.5		5	YES		The S	tart frequency, the lock detection and the release		
Low	High	0.9		1.0		10	YES		RDS =	re selectable by RDS and SFSW pin voltage. ="H", SFSW = "L": In this pattern, the lock		
High	Low	1.8		2.0		-	NO	NO protec		rotection isn't released automatically. The protection is eleased by UVLO signal input and SLEEP signal input.		
High	High	1.8		0.5		70µ	YES		Note: Please connect to VREG pin when set to			

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### **AREA OF SAFE OPERATION**

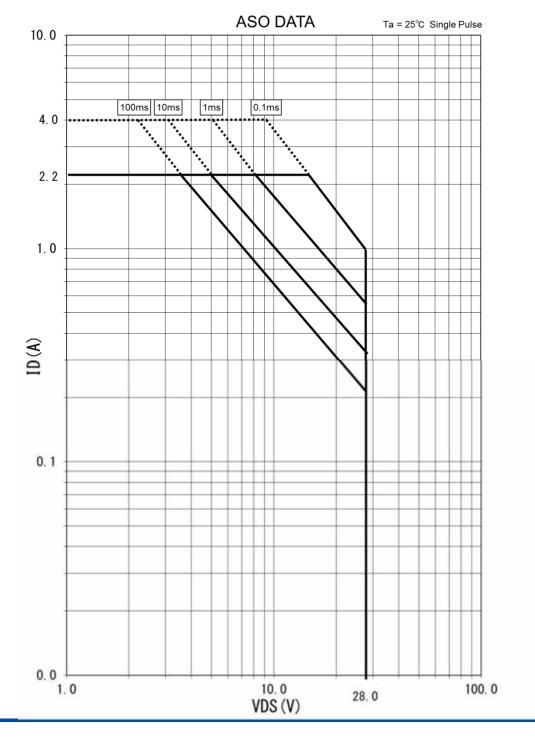
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

This data is a single pulse data under Ta = 25  $^{\circ}$ C.

Under the actual usage, there could be Tj rising and more than one pulse applied.

Therefore, please use this data only as a reference.

Customer shall conduct sufficient reliability evaluation and verification on the set.



### Pin equivalent circuit

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
1, 2	1 VREG	100Ω	Pin1 (RD), Motor lock protection output signal pin. Pin2 (FG), FG output signal pin.
3	$3$ $2k\Omega$ $47k\Omega$ $m$	100kΩ	Pin3(SLEEP), Sleep select input pin.

### Pin equivalent circuit (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
4	4	10Ω (VREG In operation)	Pin4 (VREG) Internal voltage regulator.
6,			Pin6(VPUMP), Charge pump output pin. Pin12(BC2), Pin to connect the boost capacitor.

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## Pin equivalent circuit (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
8, 9, 10, 11	VREG 88 10 11 11		Pin8 (W), 10 (V), 11 (U), Output channel pins to be connected to the motor Pin9 (RCS), Motor current sense resistor pin.

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## Pin equivalent circuit (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
13	VPUMP VCC 13	_	Pin13 (BC1), Pin to connect the boost capacitor.
14	200kΩ 200kΩ 500kΩ	1000kΩ	Pin14(OVS), Over voltage protection threshold selection pin.

## Pin equivalent circuit (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
15, 16	15 16 1000kΩ	1000kΩ	Pin15 (RDS), Motor lock protection input control pin.  Pin16(PS), Auto phase control setting input control pin.  Connect pin to VREG voltage when there is a need to set to high level.
17	VREG   563kΩ   520kΩ	_	Pin17(FGSEL), FG signal input control pin.  Connect pin to VREG voltage when there is a need to set to high level.  When pin is used in open condition, please connect capacitor to pin to prevent noise from affecting operation. Please do verifications and evaluation for this condition.
18	18	_	Pin18 (SST), Soft start triangle waveform using external capacitor to set the frequency.  Connect pin to VREG voltage when SST is not in used.

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## Pin equivalent circuit (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
19	19	_	Pin19 (TRI), Connect a capacitor to TRI pin to set the frequency in DC linear mode.  Connect pin to VREG voltage in PWM mode.
20, 21	20 (21)	Hi-Z	Pin20 (N1H), Hall amplifier + input terminal. Pin21(N1L), Hall amplifier - input terminal.

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## Pin equivalent circuit (continued)

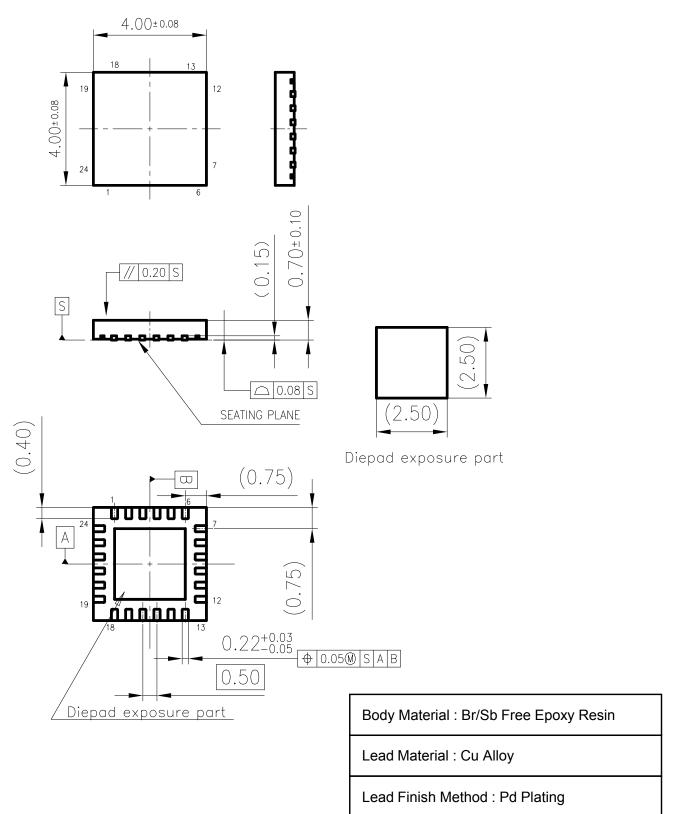
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed values.

Pin No.	Internal Circuit	Impedance	Description
22	22 4kΩ 500kΩ ————————————————————————————————————	504kΩ	Pin22 (FR), Forward / reverse rotation and short brake control input pin.
23	23	1000kΩ	Pin23 (SFSW), Start frequency selection pin.
24	24 165kΩ 165kΩ	330kΩ	Pin24 (VSP), Input pin for speed required  In PWM input mode, please use the high and low level as required in the specifications.

#### PACKAGE INFORMATION

#### **Outline Drawing**

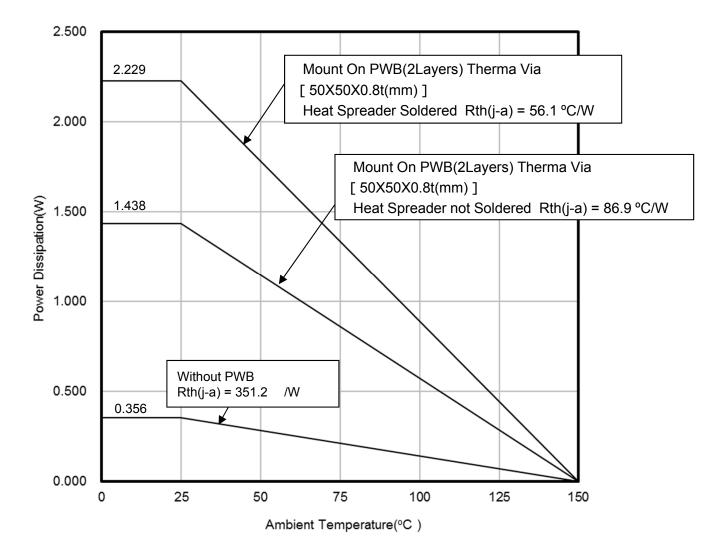
Package code: HQFN024-A-0404AZ Unit: mm



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### PACKAGE INFORMATION (Continued)

Power Dissipation (Technical Report)
Package code: HQFN024-A-0404AZ



### PACKAGE INFORMATION (Continued)

Power Dissipation (Supplementary Explanation)

#### [Experiment environment]

Power Dissipation ( Technical Report ) is a result in the experiment environment of SEMI standard conformity.

( Ambient air temperature (Ta) is 25 degrees C )

#### [Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report ) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
2-layer	2-layer	FR-4
4-layer	4-layer	FR-4

#### [Notes about Power Dissipation (Thermal Resistance) ]

Power Dissipation value (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB, mounting condition and ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the result based on evaluation under specified conditions (Evaluation environment under SEMI International Standards). Power Dissipation value (Thermal resistance) depends and changes with the environmental conditions.

#### [Definition of each temperature and thermal resistance]

Ta : Ambient air temperature

Air temperature is defined as temperature separated from the heating elements and not affected by convection, radiation, etc.

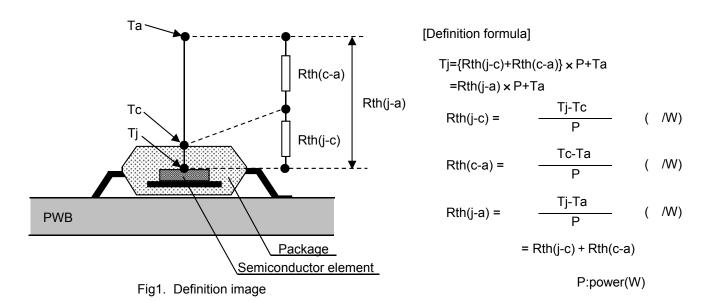
Tc : Temperature near the center of a package surface. Opposite side of the package mounting surface.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c): Thermal resistance (Temperature difference per 1 Watts) between the semiconductor element junction part and the package surface.

Rth(c-a): Thermal resistance (Temperature difference per 1 Watts) between the package surface and ambient air temperature.

Rth(j-a): Thermal resistance (Temperature difference per 1 Watts) between a semiconductor element junction part and ambient air temperature.



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#### IMPORTANT NOTICE

- 1. When using the IC for new models, verify the safety including the long-term reliability for each product.
- When the application system is designed by using this IC, please confirm the notes in this book. Please read the notes to descriptions and the usage notes in the book.
- 3. This IC is intended to be used for general electronic equipment.

Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body. Any applications other than the standard applications intended.

- (1) Space appliance (such as artificial satellite, and rocket)
- (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
- (3) Medical equipment for life support
- (4) Submarine transponder
- (5) Control equipment for power plant
- (6) Disaster prevention and security device
- (7) Weapon
- (8) Others: Applications of which reliability equivalent to (1) to (7) is required

Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.

However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.

- 4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
  - Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
- 5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
- 6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
- 7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
- 8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
- 9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
  - Although the following pins comes with short circuit protection function, the protection may be damaged depending on the VCC voltage. Pins with short circuit protection function: Pin11(U), Pin10(V) and Pin8(W).
- 10. The protection circuit is for maintaining safety against abnormal operation.
  - When sudden voltage or current change is applied to the pin, it may exceed the designated voltage and current level and therefore, customer shall perform sufficient evaluation and verification to ensure these are not exceeded in the usage.
  - Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
- 11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
- 12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
- 13. Verify the risks which might be caused by the malfunctions of external components.

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### **IMPORTANT NOTICE (Continued)**

- 14. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process.
- Dip soldering is not recommended.
- 16. Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.
- 17. Follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
- 18. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment, etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damage, for example, by using the products.

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#### **USAGE PRECAUTIONS**

- Below are the precautions to take note when using this IC.
  - 1. Apply power supply with low impedance to VCC and connect bypass capacitor near to the IC.
- 2. When designing PCB pattern for RCS pin (Pin 9), place a resistor for current detection (R<sub>RCS</sub>) close to the IC. The setting value for over current protection may fluctuate due to the impedance of wiring pattern between RCS pin and the RCS resistor.
- 3. When VCC is input, VCC voltage will start to rise to the designated voltage. However, at the same time, motor driver starts driving and when this results in decreases the VCC voltage, it may disrupt the normal start-up. Therefore, please conduct sufficient evaluation and verification to ensure the power supply current.
- 4. The minimum input amplitude of hall signal comparator should be designed in consideration of tolerances and temperature characteristics of the hall element, so that it will not result in failure to the motor operation.
- 5. In the 1-HALL-sensor system motor driver adopted in this IC, energization pattern of a cycle is generated based on previous 1-cycle of a HALL input signal. Therefore, when the acceleration of a motor is very high, the motor may be unable to accelerate normally because of the big difference in cycle between the generated energization pattern and the motor rotation. When using a motor with very high speed acceleration, ensure to conduct sufficient technical evaluation and examination on the sudden acceleration from low rotation.
  - When the above acceleration problems arises, the problem may be improved by putting the speed to zero first and then input the required speed. Please conduct sufficient evaluation before use.
  - (When HALL input signal of below 10Hz is inputted to this IC, putting the speed to zero and then input the required speed again will restart the rotation.)
- 6. Do not change the control signal of SLEEP pin (pin 3) from Low to High while motor is running at high speed. The IC can be damaged due to the effect of induced voltage and conduction angle. Conduct sufficient technical evaluation to verify.
- 7. Break current during short brake is determined by the motor running speed and motor characteristics. Before the short break, please review and evaluate by reducing the motor current and lower the motor speed. Please refer to the ASO data and perform sufficient evaluation to ensure that the IC is not damaged.
- 8. In case the motor running speed changes from high to low rapidly, supply voltage can be increased due to the flow back of motor current. Conduct sufficient evaluation and examination to ensure there is no issue.
- 9. When designing PCB pattern, place a resistor for current detection (RCS) close to the IC. The setting value for over current protection may fluctuate due to the impedance of wiring pattern between RCS pin and the RCS resistor.
- 10. FG pin (Pin 1) and RD pin (Pin 2) are open-drain outputs. Connect a pull-up resistor to the designated power supplies and use this IC within the allowable voltage and current ranges.
- 11. For the below pins, please ensure to connect to VREG pin under High level condition.

  TRI pin (Under PWM control), SST pin (When Soft Start not used), FGSEL pin, PS pin, RDS pin, OVS pin and SFSW pin.

  In addition, these terminals, changing the applied voltage during the operation of this product, we do not assume.

  When changing the voltage applied to the terminal settings, please temporarily turn off the power.
- 12. When connecting TRI pin to VREG pin using PWM input mode, please make sure to input High level or Low level to the VSP pin. Other voltage levels between High and Low level may result in unexpected operation.
- 13. Due to the initial position of the rotor, the starting torque differs slightly during start-up. For motor type that requires large inertia force to turn, please ensure that sufficient starting current is available for the motor. Please perform sufficient testing and evaluations to ensure this.
- 14. If the soft-start timing is too long, it will result in the motor not having enough starting torque and lock protection detection will be triggered if soft start timing is more than 0.5s (typ). This will cause the motor to be unable to start. Please evaluate and check this condition thoroughly when using this function.
- 15. Sufficiently check the characteristics before use. When there is changes in the external circuits, please check both static and transient characteristics and ensure that there is enough margin

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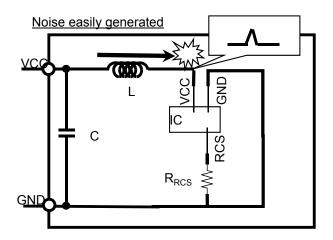
### **USAGE PRECAUTIONS (Continued)**

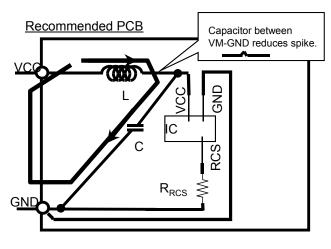
- Below are the precautions to take note when using this IC. (Continued)
  - When input power to VCC(Pin7), it is recommended that VCC voltage rises slower than 1.5V/μs and when turn off, VCC voltage drops slower than -1.5V/μs.
    - When performing power up and shutdown at high-speed, please ensure sufficient evaluation is performed to verify that there is no problem.
  - 17. Capacitor between VCC and GND

This IC employs the PWM driving method and hence, output transistor switches under high current condition and this easily generates noise. Therefore the IC may be damaged or malfunction due to noise.

Hence, it is necessary to ensure that the power supply is stable so as to avoid circuit damaged or malfunction due to noise. Where possible, place a capacitor between VCC and GND near to the IC so that IC will not malfunction due to PWM noise and gets damaged.

- 18. Points to note for Motor PCB pattern
  - As this IC is used under high current, it is necessary to take note of common impedance in the pattern. Please take care of the following in the pattern design of the motor PCB.
- As high current flows from VCC connector to the IC VCC pin (Pin7) and through the metal lines, if the metal line is a 'L' shape pattern, noise may be easily generated resulting in malfunction and damage during switching (Bottom left figure). From the figure on the right, if a capacitor is placed with respect to the connector near VCC, a noise discharge route is created and this reduces the VCC voltage directly to the IC pin. Where possible, please follow the figure on the right. In addition, metal line impedance depends on the pattern length and therefore, please keep the metal line between VCC connector and IC VCC pin as short and as thick as possible in the design.
- The line between current detection resistor (R<sub>RCS</sub>) to RCS pin (Pin9) is very important. Therefore, where possible, it is recommended to use an isolated line to connect from the start of the detection resistor to the RCS pin. Accurate current value may not be detected due to metal impedance if R<sub>RCS</sub> is placed far from the IC. Therefore, if it is not possible to place near to the IC, please ensure that the motor current waveform and R<sub>RCS</sub> current waveform is accurate.
- Please ensure that the line between the GND connector and RCS resistor is isolated from the IC GND pin (Pin5).
   If a common line is used, it may result in malfunction or IC ground connection voltage unstable due to line impedance.
   In addition, to reduce line impedance effect, please ensure that GND line is as short and as thick as possible in the design.





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## **AN44143A**

## **USAGE PRECAUTIONS (Continued)**

• Below are the precautions to take note when using this IC. (Continued)

Function	19. This IC has five protecting functions. Pay attention to the descriptions below.  Function Operate/Release Conditions Remarks			
	•	Conditions	Remarks	
Under	Operate	(Short brake)	Large current may be generated due to a short	
voltage	VCC ≤ 3.55 V	Upper-phase: OFF	brake during motor rotation. Conduct sufficient	
ock out	Release	Lower-phase: ON	verification to prevent damages.	
(UVLO)	VCC ≥ 3.75 V	Lower pridoc. Ort	vermodien to prevent damages.	
Over	Operate/Release	(Short brake)	Large current may be generated due to a short	
voltage	VCC input voltage1: 16.0V (typ.)	Upper-phase: OFF	brake during motor rotation. Conduct sufficient	
lock out	VCC input voltage2: 27.2V (typ.)	Lower-phase: ON	verification to prevent damages.	
(OVLO)	voo input voitagez. 27.2v (typ.)	•		
			R <sub>RCS</sub> is a current detection resistor.	
Over	Operate:	(Ob t b l )	Concerning level of detection, false detection ma	
Current	RCSS voltage ≥ 0.25V (typ.)	(Short brake)	occur due to the effect of PCB layout or noise.	
Protection	• Release:	Upper-phase: OFF	In addition, when specifying the resistance value	
(CL)	RCSS voltage ≤ 0.25V (typ.)	Lower-phase: ON	of R <sub>RCS</sub> , take the followings into consideration:	
` ′	(typ.)		Level of detection, tolerance in resistance value	
			R <sub>RCS</sub> , temperature, ratings, etc.	
	Operate:			
	Hall signal input cycle			
	≥ 0.5 s (RDS=L, SFSW=L)			
	(RDS=H, SFSW=H)			
	≥ 1.0 s (RDS=L, SFSW=H)			
	≥ 2.0 s (RDS=H, SFSW=L)			
	(Based on the rising or falling edge			
	of H1H-H1L )			
	• Release:			
	<ul> <li>With RDS and SFSW is set to following voltage, any of the below 7 conditions will</li> </ul>			
	result in the protection to release.			
	·RDS = L or open and SFSW = L or H			
Ma4a.	•	(Charthralia)	Drake current may be generated due to protecti	
Motor	RDS = H and SFSW = H	(Short brake) Upper-phase: OFF Lower-phase: ON	Brake current may be generated due to protection	
Lock Protection	SLEEP is input with 'H'		circuit operating during the motor rotation.  Conduct sufficient verification to prevent damage	
i iolection	UVLO operates (VCC<3.55V)			
	Automatic reset after the following time;			
	5 s (RDS=L, SFSW=L)			
	10 s (RDS=L, SFSW=H)			
	70 us (RDS=H,SFSW=H)			
	Hall signal being input			
	(Rising or falling edge of H1H-H1L)			
	VSP(PWM)<3.0%(typ), or			
	VSP(DC)<1.0V(typ) is inputted			
	FR signal switch is inputted			
	SBRK signal is inputted			
	Control restrictions to protection functions			
	When RDS is set to 'H' and SFSW is set to			
	'L', the above ~ will be disabled.			
			Since all phases are OFF when protecting	
Th	• Operate:		function operates, reverse current may be	
Thermal	IC junction temperature > 160 • Release:	All phases: OFF	generated due to the repetition ON-OFF switchi	
	• Palagea.			
Protection	IC junction temperature < 135		of the protection function during motor rotation.	

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