AN5394FB

RGB processor IC for the HDTV (Japan) and wide-screen TV

■ Overview

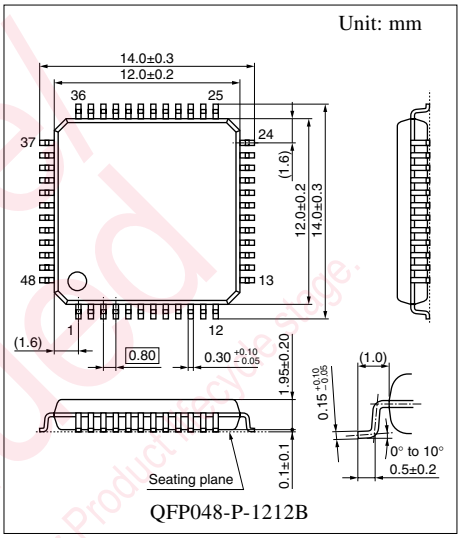
The AN5394FB is an RGB processor IC which converts the brightness and color difference signals to a primary color signal. It can be connected to each input signal of HDTV (Japan), DVD, NTSC, PAL, VGA, etc. and facilitates rationalization and high performance of the end-products.

■ Features

- Wider band for signal processing (Y: 30 MHz/–3 dB, color difference: 15 MHz/–3 dB)
- Direct input of HD, NTSC and DVD standard YUV signal
- High picture quality due to the built-in various correction circuits of Y signal
- Auto-cut off functions
- Having 2 systems of RGB input, OSD plus character broadcasting or external RGB input such as VGA is supported.
- SMD package allows for high density mounting.

■ Applications

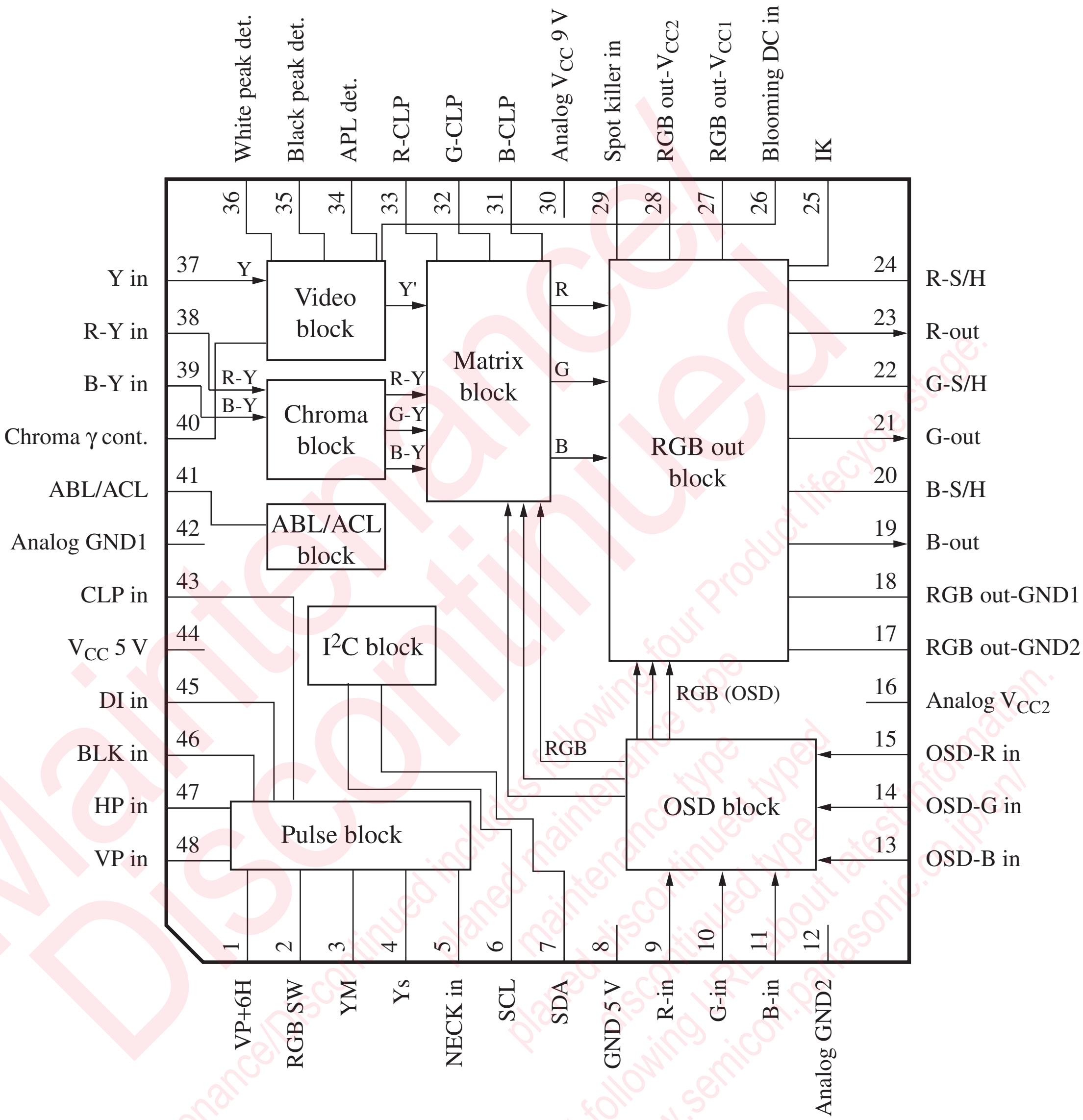
- HDTV (Japan), wide-screen television, projection television, plasma display panel (PDP), LCD projector, video capture board



QFP048-P-1212B

Note) The package of this product will be changed to lead-free type (QFP048-P-1212C). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	VP + 6H	25	IK
2	RGB SW	26	Blooming DC in
3	YM input	27	RGB out-V_{CC1}
4	Ys input	28	RGB out-V_{CC2}
5	Neck in	29	Spot killer in
6	SCL	30	Analog V_{CC1}
7	SDA	31	B-CLP
8	GND 5 V	32	G-CLP
9	R-n	33	R-CLP
10	G-in	34	APL det.
11	B-in	35	Black peak det.
12	Analog GND2	36	White peak det.
13	OSD-B in	37	Yin
14	OSD-G in	38	R−Y in
15	OSD-R in	39	B− Y in
16	Analog V_{CC2}	40	Chroma γ cont.
17	RGB out-GND2	41	ABL/ACL
18	RGB out-GND1	42	Analog GND1
19	B output	43	CLP in
20	B-S/H	44	V_{CC} 5V
21	G output	45	DI in
22	G-S/H	46	BLK in
23	R output	47	HP in
24	R-S/H	48	VP in

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	10.0	V
	V_{CC2}	5.6	
Supply current	I_{CC1}	70.0	mA
	I_{CC2}	39.2	
Power dissipation *2	P_D	681	mW
Operating ambient temperature *1	T_{opr}	−25 to +70	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) ∗1 : Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

∗2 : Power dissipation P_D indicates the value in the free air at T_a = 70°C. For further details, refer to "■ Technical Information".

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	8.1 to 9.9	V
	V_{CC2}	4.5 to 5.5	

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(1) DC characteristics						
Circuit current 1 *1	I_{CC1}	V_{CC1} = 9 V, V_{CC2} = 5 V No signal input	39	51	63	mA
Circuit current 2 *1	I_{CC2}	V_{CC1} = 9 V, V_{CC2} = 5 V No signal input	24	31	35	mA
(2) Y-system						
Video voltage gain	AY_G	Input: Sine wave 0.2 V[p-p] f = 1 MHz; Contrast: max.	4.4	5.4	6.4	Times
Video voltage gain change	ΔAY	Ratio between R,G and B Drive: typ.	−2.5	0	2.5	dB
Frequency characteristics	fY	Input: Sine wave 0.2 V[p-p] f = 30 MHz; Contrast: max.	−6	−3	1	dB
Standard output pedestal	DC_P	Brightness: typ.	2.6	3.0	3.4	V
Brightness variable range	V_{BR}	Brightness: min. → max.	1.8	2.2	2.6	V
Contrast ratio	A(CON)	Contrast: min. → max.	25	—	—	dB
APL detection voltage	V_{APL}	Input: Total white 0.7 V[0-p] Voltage at APL detection pin 34	0.7	0.93	1.3	V
APL detection ratio	Δ_{APL}	Input: Total white 0.7 V[0-p] → 0.35 V[0-p] Voltage at APL detection pin 34	0.44	0.54	0.64	Times
DC regeneration ratio 1	DC1	Input signal APL 10% → 90% APL detection pin 34 = 0 V	95	100	105	%
DC regeneration ratio 2	DC2	Input signal APL 10% → 90% DC regeneration SW/on; Polarity '−' APL det./R = 75 kΩ	70	80	90	%
DC regeneration ratio 3	DC3	Input signal APL 10% → 90% DC regeneration SW/on; Polarity '+' APL det./R = 75 kΩ	110	120	130	%
Output blooming level	V_{BL}	Input: Total white 1.4 V[0-p] Blooming DC = 3.8 V Pin 34: 0 V; Brightness: max.	5.7	6.7	7.7	V
Output blooming level change	ΔV_{BL}	Input: Total white 1.4 V[0-p] Blooming DC = 3.8 V → 4.2 V Pin 34: 0 V; Brightness: max.	−1.2	− 0.9	− 0.7	V

Note) *1: I_{CC1} is a total of the current at pins 16, 27, 28 and 30. I_{CC2} is a total of the current at pin 44.

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(2) Y-system (continued)						
White gradation correction 1 *2	$Y\gamma 1$	Input: Total white 0.7 V[0-p] Gain: max. Level: typ. → max. White gradation SW: On	10	16	22	%
White gradation correction 2 *2	$Y\gamma 2$	Input: Total white 0.7 V[0-p] Gain: max. Level: typ. → min. White gradation SW: On	–26	–20	–14	%
Black extension characteristics 1 *3	Y_{BL1}	Output amplitude 0 V[p-p] Level: typ., gain: min. → max.	– 0.1	0	0.1	V
Black extension characteristics 2 *3	Y_{BL2}	Input: Total white 0.7 V[0-p] Output amplitude1.0 V[0-p], contrast adj level: typ., gain: min. → max.	– 0.86	– 0.66	– 0.46	V
Black extension characteristics 3 *3	Y_{BL3}	Input: Total white 0.7 V[0-p] Output amplitude1.6 V[0-p], contrast adj level: typ., gain: min. → max.	– 0.1	0	0.1	V
Black extension characteristics 4 *4	Y_{BL4}	Black detection open → 3 V Level: typ., gain: typ.	– 0.8	– 0.6	– 0.4	V
Black extension characteristics 5 *4	Y_{BL5}	Black detection open → 3 V Level: typ., gain: max.	–1.5	–1.1	– 0.7	V
Black extension characteristics 6 *4	Y_{BL6}	Black detection open → 3 V Level: min. → max., gain: typ.	–1.20	– 0.75	– 0.30	V
White character correction 1 *2	V_{W1}	Input: Total white 0.7 V[0-p] Blooming DC adjustment Level: max., gain: min. → typ.	10.0	25.0	40.0	%
White character correction 2 *2	V_{W2}	Input: Total white 0.7 V[0-p] Blooming DC adjustment Level: min., gain: min. → max.	–9.3	0	9.3	%
White character correction off *2	W_{OFF}	Y input: Total white 0.7 V[0-p] C-Y input: 0.2 V[0-p] Level: min., gain: min. → max.	– 0.2	0	0.2	V
ABL off *5	V_{ABL1}	ABL/ACL pin 7.5 V Level: min., gain: min. → max.	– 0.1	0	0.1	V
ABL start 1*5	V_{ABL2}	ABL/ACL pin 3 V Level: min. → max., gain: max.	0.28	0.39	0.50	V
ABL start 2*5	V_{ABL3}	ABL/ACL pin 3 V Level: min., gain: min. → max.	– 0.84	– 0.64	– 0.44	V
ABL gain 1*5	A_{ABL}	ABL/ACL pin 5 V → 3 V Level: typ., gain: max.	– 0.48	– 0.37	– 0.26	V

Note) *2: Adjust the blooming DC voltage (pin 26).
*3: Black gradation SW: On
*4: Black gradation SW: On, brightness: max.
*5: ABLSW: On, brightness: max.

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(2) Y-system (continued)						
ACL off *6	A_{ACL1}	Input: Total white 0.7 V[0-p] ABL/ACL pin: 7.5 V Level: min., gain: min. → max.	−5	0	5	%
ACL start 1 *6	A_{ACL2}	Input: Total white 0.7 V[0-p] ABL/ACL pin: 3 V Level: min. → max., gain: typ.	10	20	30	%
ACL start 2 *6	A_{ACL3}	Input: Total white 0.7 V[0-p] ABL/ACL pin: 3 V Level: min., gain: min. → typ.	−45	−35	−25	%
ACL gain 1 *6	A_{ACL4}	Input: Total white 0.7 V[0-p] ABL/ACL pin: 5 V → 3 V Level: typ., gain: typ.	−34	−22	−10	%
(3) Color difference-system						
Color difference voltage gain *7	G_R	Input: Sine wave 0.2 V[p-p] f = 1 MHz, R−Y_{IN} → R_{OUT}	4.64	5.80	6.96	Times
Color difference frequency characteristics *7	fc	Input: Sine wave 0.2 V[p-p] f = 10 MHz	− 6	− 3	+ 2	dB
B−Y axis gain adjustment range NTSC1 *7	G_{B-Y1}	B−Y input: 0.2 V[0-p] B−Y gain: min., brightness: max. Input-SW: NTSC-standard	0.34	0.48	0.62	Times
B−Y axis gain adjustment range NTSC2 *7	G_{B-Y2}	B−Y input: 0.2 V[0-p] B−Y gain: max., brightness: max. Input-SW: NTSC-standard	0.84	1.20	1.56	Times
Tint variable range *8	Tc	R−Y input: 0.228 V[0-p] B−Y input: 0.406 V[0-p] Tint: min. → max.	± 33	± 48	± 68	°
Color control *7	C_{CON}	Color: typ. → max. Contrast: typ.	3	6	9	dB
Color residue *7	C_{MIN}	Color: min., B−Y gain: max. Contrast: max.	− 50	0	50	mV[p-p]
R−Y angle adjustment range *8	θ_R	R−Y input: 0.228 V[0-p] B−Yinput: 0.406 V[0-p] R−Y axis: min. → max.	12	19	26	°

Note) ∗6: ACLSW: On

∗7: Adjust tint, drive R and B.

∗8: Adjust tint, drive R, B and B−Y gains

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color difference-system (continued)						
Input matrix ratio 1 (HD/NTSC) R−Y *7	SW1	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $R-Y_{IN} \rightarrow R_{OUT}$	1.30	1.62	1.94	Times
Input matrix ratio 2 (DVD/NTSC) R−Y *7	SW2	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $R-Y_{IN} \rightarrow R_{OUT}$	1.14	1.42	1.70	Times
Input matrix ratio 3 (HD/NTSC) B−Y *7	SW3	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $B-Y_{IN} \rightarrow B_{OUT}$	1.53	1.91	2.29	Times
Input matrix ratio 4 (DVD/NTSC) B−Y *7	SW4	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $B-Y_{IN} \rightarrow B_{OUT}$	1.45	1.81	2.17	Times
Output matrix ratio 1 (matrix 1/standard) R−Y *7	SW5	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $R-Y_{IN} \rightarrow R_{OUT}$	1.28	1.60	1.92	Times
Output matrix ratio 2 (matrix 2/standard) R−Y *7	SW6	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $R-Y_{IN} \rightarrow R_{OUT}$	1.10	1.38	1.65	Times
Output matrix ratio 3 (matrix 1/standard) B−Y *7	SW7	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $B-Y_{IN} \rightarrow B_{OUT}$	1.28	1.60	1.92	Times
Output matrix ratio 4 (matrix 2/standard) B−Y *7	SW8	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $B-Y_{IN} \rightarrow B_{OUT}$	1.10	1.38	1.65	Times
G−Y matrix ratio (G−Y/R−Y) HD *7	M1	G−Y matrix: HD	0.23	0.30	0.35	Times
G−Y matrix ratio (G−Y/R−Y) standard *7	M2	G−Y matrix: Standard	0.38	0.51	0.58	Times
G−Y matrix ratio (G−Y/R−Y) matrix 1 *7	M3	G−Y matrix: matrix 1	0.26	0.34	0.40	Times
G−Y matrix ratio (G−Y/R−Y) matrix 2 *7	M4	G−Y matrix: matrix 2	0.26	0.34	0.40	Times
G−Y matrix ratio (G−Y/B−Y) HD *7	M5	G−Y matrix: HD	0.07	0.10	0.13	Times
G−Y matrix ratio (G−Y/B−Y) standard *7	M6	G−Y matrix: Standard	0.15	0.19	0.23	Times
G−Y matrix ratio (G−Y/B−Y) matrix 1 *7	M7	G−Y matrix: matrix 1	0.22	0.28	0.34	Times
G−Y matrix ratio (G−Y/B−Y) matrix 2 *7	M8	G−Y matrix: matrix 2	0.13	0.17	0.21	Times

Note) *7: Adjust tint, drive R and B.

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(4) OSD, RGB input						
Ys input threshold voltage *9	Ys_{TH}	Pin 4 > 2.1 V: OSD Pin 4 < 0.9 V: Main or RGB	0.9	1.4	2.1	V
RGB input threshold voltage *9	RGB_{TH}	Pin 2 > 2.1 V: RGB Pin 2 < 0.9 V: Main	0.9	1.4	2.1	V
Ym input threshold voltage *9	Ym_{TH}	Pin 3 > 2.1 V: Half tone Pin 3 < 0.9 V: Normal	0.9	1.4	2.1	V
CLP input threshold voltage	CLP_{TH}	Pin 43 (main, OSD, RGB)	0.9	1.4	2.1	V
Clamp-possible pulse width	W_M	Pin 43 (main, OSD, RGB)	0.8	—	—	µs
OSD gain	G_{OSD}	Input: Sine wave 0.2 V[p-p] f = 1 MHz, Ys pin: 2.1 V	4.6	5.8	7.0	Times
OSD frequency characteristics	f_{OSD}	Input: Sine wave 0.2 V[p-p] f = 30 MHz, Ys pin: 2.1 V	−7	−3	1	dB
OSD contrast ratio 1	OSD_{C1}	Contrast: max. → typ. Ys pin: 2.1 V	−3	−1	1	dB
OSD contrast ratio 2	OSD_{C2}	Contrast: typ. → 01 Ys pin: 2.1 V	−16	−11	−7	dB
RGB gain	G_{RGB}	Input: Sine wave 0.2 V[p-p] f = 1 MHz, RGB pin: 2.1 V	4.6	5.8	7.0	Times
RGB frequency characteristics	f_{RGB}	Input: Sine wave 0.2 V[p-p] f = 30 MHz, RGB pin: 2.1 V	−7	−3	1	dB
RGB contrast ratio	RGB_C	Contrast: max. → min. RGB pin: 2.1 V	25	—	—	dB
(5) Cutoff drive						
BLK input threshold voltage *10	BLK_{TH}	BLK SW: On	0.9	1.4	2.1	V
Neck mute input threshold voltage *10	N_{TH}		0.9	1.4	2.1	V
DI input threshold voltage	D_{TH}		0.9	1.4	2.1	V
Vp input threshold voltage	V_{TH}		0.9	1.4	2.1	V
Hp input threshold voltage	H_{TH}		0.9	1.4	2.1	V
Cutoff variable range (R, G, B) *11	ΔL_{RGB}	Cutoff R, G, B: min. → max. Cutoff SW: min. → max.	1.6	2.0	2.4	V
Drive variable range (R, G, B)	ΔG_D	Drive R, G, B: min. → max.	9.0	11.5	14.0	dB
R, G, B pedestal potential difference	ΔV_P	Cutoff: typ. Bright: typ.	− 0.3	0	0.3	V

Note) ∗9: SW priority: Ys > Ym, RGB

∗10: Priority: Neck > single color adjustment (I^2C) > auto cutoff > BLK SW(I^2C) > BLK pulse

∗11: Drive R, B adjustment

■ Electrical Characteristics at V_{CC1} = 9 V, V_{CC2} = 5 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(5) Cutoff drive (continued)						
Output blanking level	BLK	BLK SW: On BLK (pin 46): 2.1 V	1.0	1.4	1.8	V
IK pulse peak voltage (max.)*12	IK_{max}	IK input (pin 25) BLK SW: On Auto cutoff mode	2.7	3.5	4.3	V
IK pulse peak voltage varying width*12	ΔIK	IK input (pin 25) BLK SW: On Auto cutoff mode	2.5	3.1	3.7	V
Potential difference for IK pulse vs. pedestal *12	IK-PED	IK input (pin 25) BLK SW: On Auto cutoff mode	– 0.01	0.23	0.31	V
(6) I^2C · DAC						
SCL · SDA Input threshold voltage	V_{TH}	V_{CC2} = 5 V	1.5	—	3.0	V
Sink ability at ACK	V_{ACK}	I = 3 mA at pull-up 1.6 kΩ	—	—	0.4	V
Maximum clock frequency		V_{CC2} = 5 V	100	—	—	kHz

Note) *12: Priority ··· NECK > single color adjustment (I^2C) > auto cutoff > BLKSW

• Design refernce data

V_{CC} = 9 V, V_{CC} = 5 V, T_a = 25°C

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(1) Y-system						
Y (main) Input dynamic range	D_{YIN1}	V_{CC1} = 9 V V_{26} = 1.5 V Contrast; typ.	—	1.4	—	V[p-p]
R, G, B output dynamic range	D_{OUT}	V_{CC1} = 9 V For pedestal 3 V	—	4.4	—	V[p-p]
APL detection stop	APL_S	BLK, DI = 2.1 V	—	0	—	V
Black extension inhibition delay	TH_{BLACK}	Delay from BLK, DI	—	60	—	ns
S/N	S/N	Band width 20 MHz	—	–56	—	dB
Y output amplitude Ambient temp. dependency	Y/ΔT	– 20°C to +70°C	—	±2	—	%
Y signal delay time	TD_Y	f = 5 MHz	—	19	—	ns
(2) Color difference-system						
R–Y, B–Y input dynamic range (HD)	D_{CIN1}	Input–SW: HD	–	±0.7	–	V[p-p]
R–Y, B–Y input dynamic range (NTSC)	D_{CIN2}	Input–SW: NTSC standard	–	±1.1	–	V[p-p]

■ Electrical Characteristics at V_{CC} = 9 V, V_{CC} = 5 V, T_a = 25°C (continued)

The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

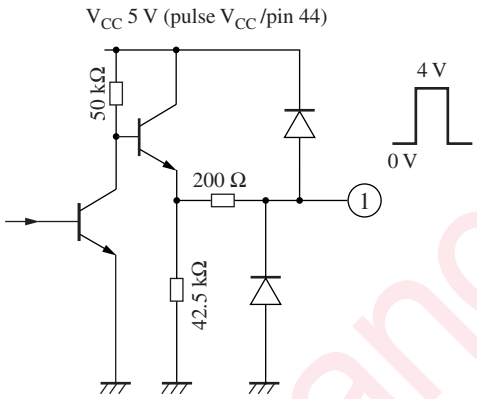
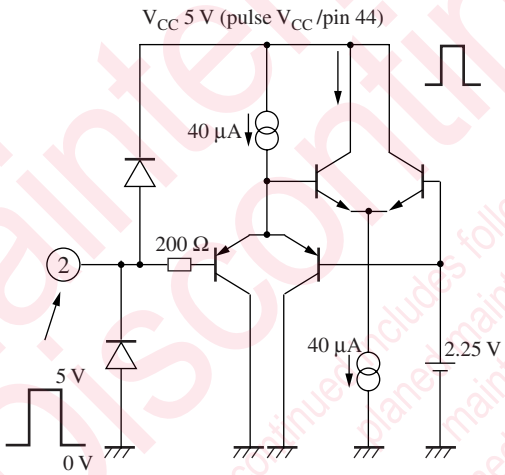
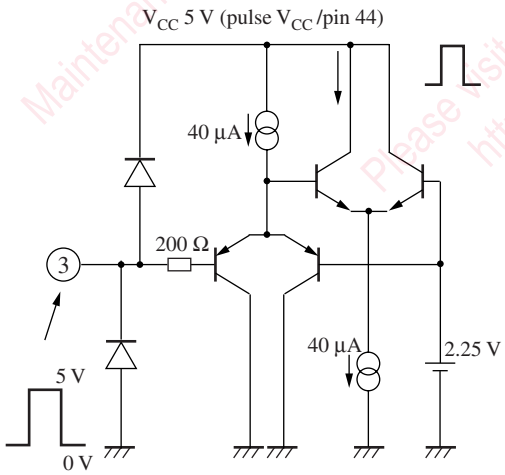
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(2) Color difference-system (continued)						
R−Y, B−Y input dynamic range (DVD)	D_{CIN3}	Input−SW: DVD standard	–	±0.7	–	V[p-p]
R−Y angle adjustment range (2)	θ_{R2}	R−Y input: 0.228 V[0-p] B−Y input: 0.406 V[0-p] R−Y axis: min.	–	0	–	°
Color difference contrast ratio	C_{CONT}	Contrast: min. → max.	26	–	–	dB
Tint ambient temp. dependency	TC/T	−20°C to +70°C	—	±2	—	°C
Color difference signal delay time	TD_C	f = 5 MHz	—	40	—	ns
Color difference output amplitude Ambient temp. dependency	C/ΔT	−20°C to +70°C	—	±4	—	%
Chroma γ control (1)	$\gamma_{CHROMA(1)}$	Pin 40: Open → 3 V White gradation SW: On Gain: max, Level: typ.	—	2.0	—	Times
Chroma γ control (2)	$\gamma_{CHROMA(2)}$	Pin 40: Open → 6 V White gradation SW: On Gain: max, Level: typ.	—	0	—	Times
(3) Cross-talk						
Y cross-talk Y(main → OSD)	CT_1	f = 10 MHz	—	−75	—	dB
Y cross-talk Y(main ↔ RGB)	CT_2	f = 10 MHz	—	−78	—	dB
Color difference cross-talk R−Y(main → OSD)	CT_3	f = 10 MHz	—	−67	—	dB
Color difference cross-talk B−Y(main → OSD)	CT_4	f = 10 MHz	—	−80	—	dB
Color difference cross-talk R−Y(main → RGB)	CT_5	f = 10 MHz	—	−66	—	dB
Color difference cross-talk B−Y(main → RGB)	CT_6	f = 10 MHz	—	−85	—	dB
Cross-talk (OSD → main)	CT_7	f = 10 MHz	—	−54	—	dB
Cross-talk (OSD → RGB)	CT_8	f = 10 MHz	—	−52	—	dB
Cross-talk between OSD	CT_9	f = 10 MHz	—	−47	—	dB
Cross-talk (RGB → main)	CT_{10}	f = 10 MHz	—	−44	—	dB
Cross-talk (RGB → OSD)	CT_{11}	f = 10 MHz	—	−44	—	dB
Cross-talk between RGB	CT_{12}	f = 10 MHz	—	−48	—	dB
(4) OSD, RGB						
OSD signal delay	t_{dOSD}	f = 5 MHz	—	12	—	ns
RGB signal delay	t_{dRGB}	f = 5 MHz	—	15	—	ns
Ys rise-up delay	t_{rYs}		—	31	—	ns
Ys fall delay	t_{fYs}		—	40	—	ns

■ Electrical Characteristics at V_{CC} = 9 V, V_{CC} = 5 V, T_a = 25°C (continued)

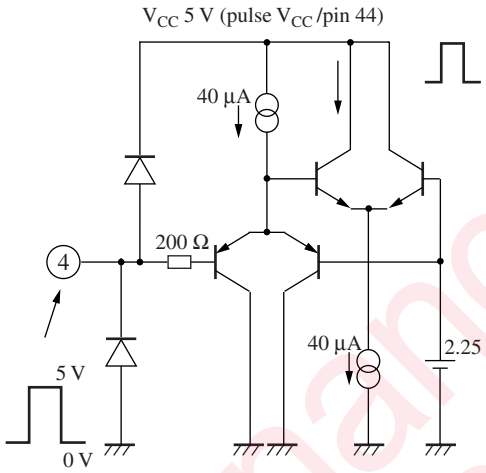
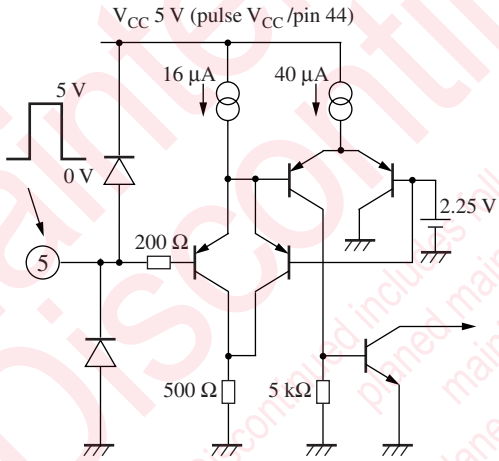
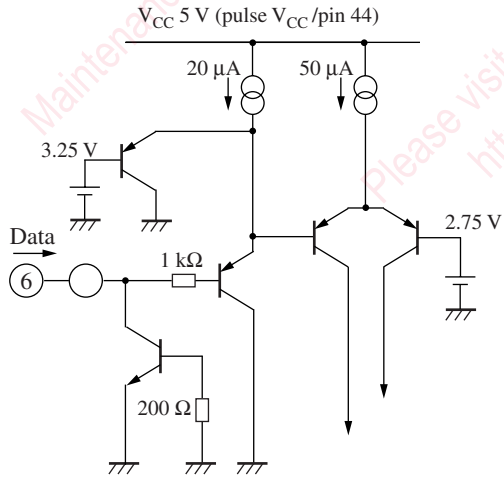
The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(4) OSD, RGB (continued)						
Ym rising delay	t_{rYm}		—	22	—	ns
Ym falling delay	t_{fYm}		—	20	—	ns
RGB rising delay	t_{rRGB}		—	28	—	ns
RGB falling delay	t_{fRGB}		—	43	—	ns
Pedestal change at Ys changeover	$\Delta V_{P(Ys)}$	Ys: Low → varying amount of high	—	–40	—	mV
Pedestal change at Ym changeover	$\Delta V_{P(Ym)}$	Ym: Low → varying amount of high	—	–40	—	mV
Pedestal change at RGB changeover	$\Delta V_{P(RGB)}$	RGB: Low → varying amount of high	—	–40	—	mV
Pedestal change at RGB+Ym changeover	$\Delta V_{P\ (RGB+Ym)}$	RGB, Ym: Low → varying amount of high	—	–50	—	mV
OSD input dynamic range	D_{OSD}		—	1.5	—	V[p-p]
OSD output amplitude ambient temp. dependency	$\frac{OSD}{\Delta T}$	–20°C to +70°C	—	±2	—	%
RGB input dynamic range	D_{RGB}		—	1.5	—	V[p-p]
RGB output amplitude ambient temp. dependency	$\frac{RGB}{\Delta T}$	–20°C to +70°C	—	±2	—	%
R, B-in clamp voltage variable range	ΔV_{CLP}	R-in, B-in–DC adj min. → max.	—	200	—	mV
(5) Cutoff drive						
Blanking delay	$t_{dBLK(1)}$	From BLK to BLK output	—	45	—	ns
Pedestal fluctuation at contrast variation	$\Delta V_{P(CONT)}$	Contrast: min. → max.	—	0	—	mV
Pedestal fluctuation at color variation	$\Delta V_{P(COLOR)}$	Contrast: min. → max.	—	0	—	mV
Pedestal fluctuation at tint variation	$\Delta V_{P(TNIT)}$		—	0	—	mV
Output pedestal potential ambient temp. dependency	$\frac{\Delta VP}{\Delta T}$	–20°C to +70°C	—	–1.5	—	mV/°C
Spot killer operation	V_{SP}	Lowering 9V system V_{CC} Pin 29: C = 10 µF	—	7.8	—	V
(6) I²C DAC						
4 · 5 · 6DAC DNLE	L1	1LSB = {DAT (max.) – data(min.)}/(2^N–1)	0.1	1.0	1.9	$\frac{LSB}{STep}$
8-bit DAC DNLE (excluding 40, 80, CO)	L2	1LSB = {DAT (max.) – data(min.)}/(2^N–1)	0.1	1.0	1.9	$\frac{LSB}{STep}$
8-bit DAC DNLE (for 40, 80, CO only)	L3	1LSB = {DAT (max.) – data(min.)}/(2^N–1)	–1.0	1.0	2.0	$\frac{LSB}{STep}$
7-bit DAC DNLE (excluding 40)	L4	1LSB = {DAT (max.) – data(min.)}/(2^N–1)	0.1	1.0	1.9	$\frac{LSB}{STep}$
7-bit DAC DNLE (for 40 only)	L5	1LSB = {DAT (max.) – data(min.)}/(2^N–1)	–1.0	1.0	2.0	$\frac{LSB}{STep}$

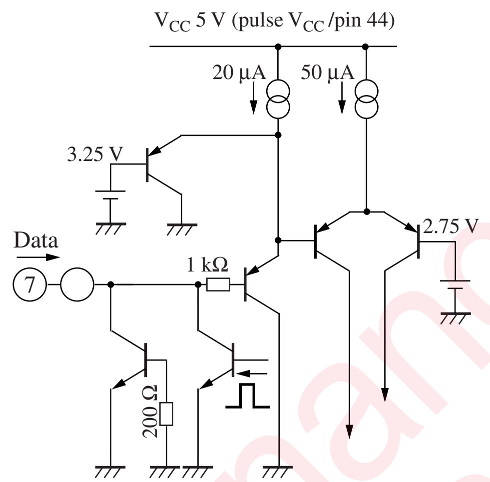
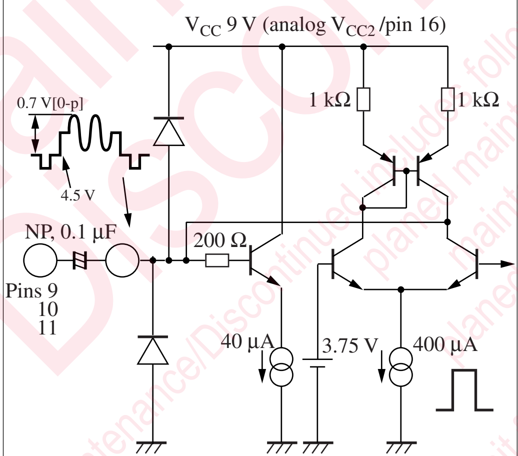
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description
1		VP+6H: VP+6H pin • Outputs the pulse whose width is pin 48 input pulse plus 6H. • Recommended use range: 200 µA to 0 µA
2		RGB-in: RGB switch signal input pin • Input threshold voltage: 1.4 V 1) 2.1 V < V_2 Outputs the signal inputted from Pins 9, 10 and 11. 2) V_2 < 0.9 V Outputs the signal inputted from pins 13, 14, 15 or pins 37, 38, 39. Note) If you switch main input to RGB input in a high speed within 1H period, WB will be changed. In this case, adjust R-in DC adj. and B in DC adj. of the sub-address 16,17. • Priority of signal switch Ys > Ym > RGB • Recommended use range: 0 V to 5 V
3		Ym in: Half tone switch signal input pin • Input threshold voltage: 1.4 V 1) 2.1 V < V_3 Lowers the amplitude of the signal inputted from pins 9, 10, 11 or pins 37, 38, 39. 2) V_3 < 0.9 V Normal • Priority of signal switch Ys > Ym > RGB • Recommended use range: 0 V to 5 V

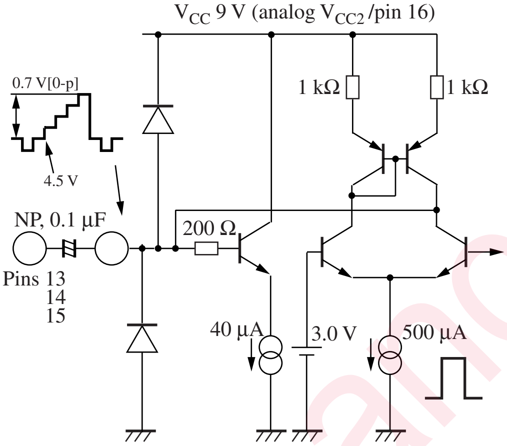
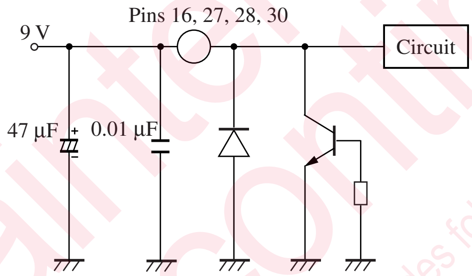
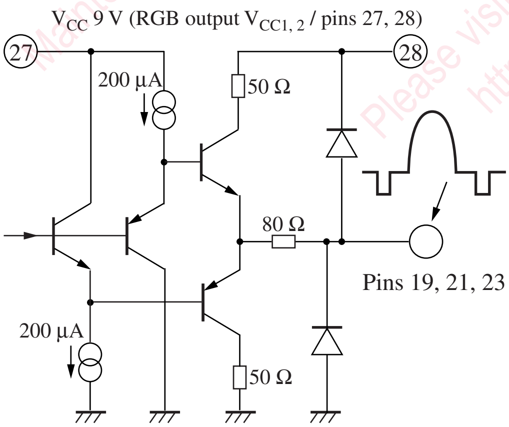
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
4		Ys in: OSD switch signal input pin • Input threshold voltage: 1.4 V 1) 2.1 V < V_4 Outputs the OSD signal inputted from pins 13, 14 and 15. 2) V_4 < 0.9 V Outputs the OSD signal either from pins 9, 10, 11 or Pins 37, 38, 39. • Priority of signal switching Ys > Ym > RGB • Recommended use range: 0 V to 5 V
5		Neck in: Neck input pin • Input threshold voltage: 1.4V Hingh: $V_{19, 20} \geq 2.1$ V Low: $V_{19, 20} \leq 0.9$ V • Force the RGB output down to BLK level when the input = high. At this time, BLKSW (I^2C) and the single color adjustment SW (I^2C) become invalid and the IK clamp pulse is not outputted. • Recommended use range: 0 V to 5 V
6		SCL: I^2C clock input pin • Input threshold voltage: 2 V • Recommended use range: 0 V to 5 V

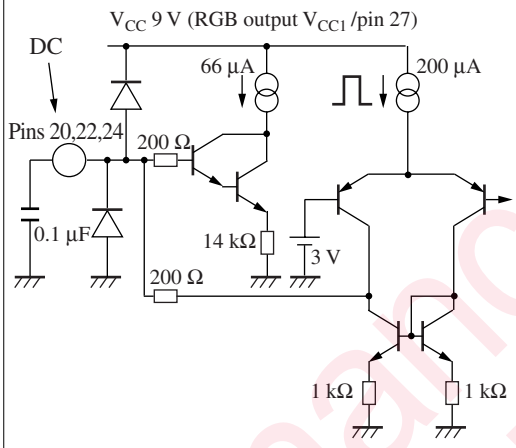
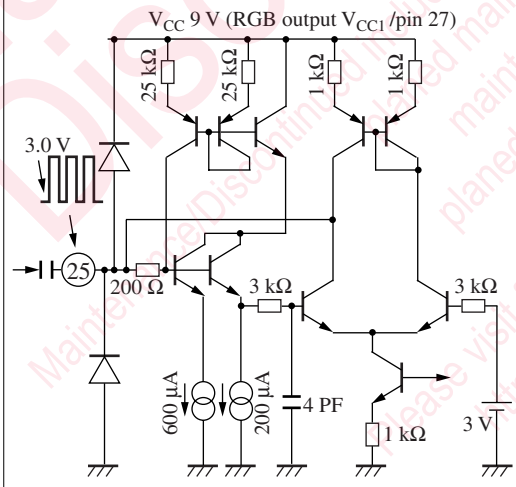
■ Terminal Equivalent Circuits (continued)

<table>
<tr><th>Pin No.</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>7</td><td> 
</td><td>SDA:
I²C bus input pin
• Input threshold voltage: 2 V
• Recommended use range: 0 V to 5 V</td></tr>
<tr><td>8</td><td>—</td><td>GND:
GND pin
• Pin 8 : Pulse-system GND pin</td></tr>
<tr><td>9
10
11</td><td> 
</td><td>RGB in:
RGB signal input pin for analog signal
• A standard input signal is 0.7 V[0-p] from a black level to a white level.
Pin 9: R signal input pin
Pin 10: G signal input pin
Pin 11: B signal input pin
Drive them at a low impedance.
• Clamp an input signal with pin 43 clamp pulse.
• Recommended use range: Do not apply the DC voltage from outside.</td></tr>
<tr><td>12</td><td>—</td><td>GND:
GND pin
• Pin 12: GND pin for OSD, RGB input circuit</td></tr>
</table>

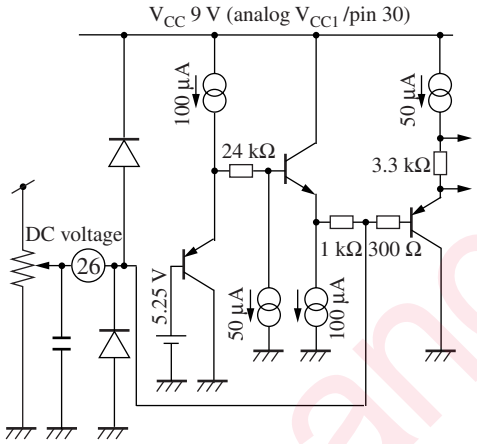
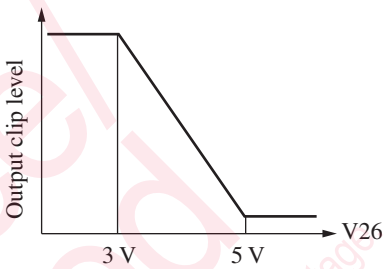
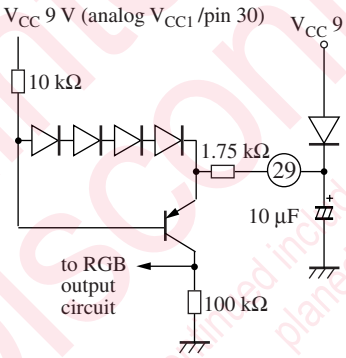
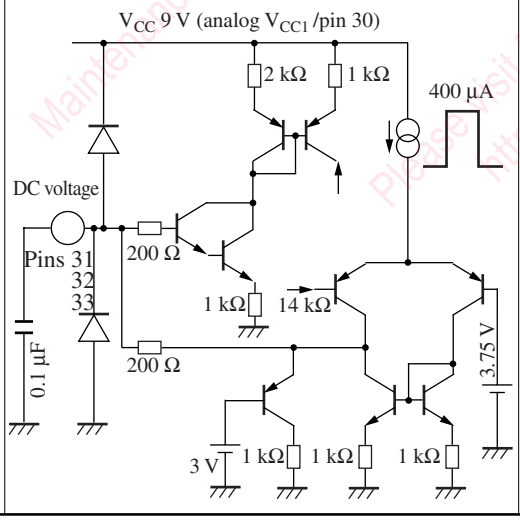
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
13 14 15		OSD in: OSD signal input pin for analog signal • A standard input signal is 0.7 V[0-p] from black to white level Pin 13: B signal input pin Pin 14: C signal input pin Pin 15: R signal input pin Drive them at a low impedance. • Clamp the input signal with pin 43 clamp pulse. • Recommended use range: Do not apply the DC voltage from outside.
16		V_{CC} 9 V: Signal-system power supply pin • Apply 9 V for use. • Pin 16: OSD, RGB input circuit power supply pin (pair with pin 12 GND) Pin 27: RGB output circuit power supply pin (pair with pin 18 GND) Pin 28: RGB output circuit power supply pin (pair with pin 17 GND) Pin 30: Analog power supply pin (pair with pin 42 GND) • Recommended use range: 8.1 V to 9.9 V
17	—	GND: GND pin • Pin 17: GND pin for RGB output circuit
18	—	GND: GND pin • Pin 18: GND pin for RGB output circuit
19		R, G, B-out: RGB output pin • Output dynamic range 1.5 V to 7.5 V • Use the standard output pedestal at approx. 3 V. • Pin 23: R output pin Pin 21: G output pin Pin 19: B output pin • Recommended use range: −4 mA to +4 mA

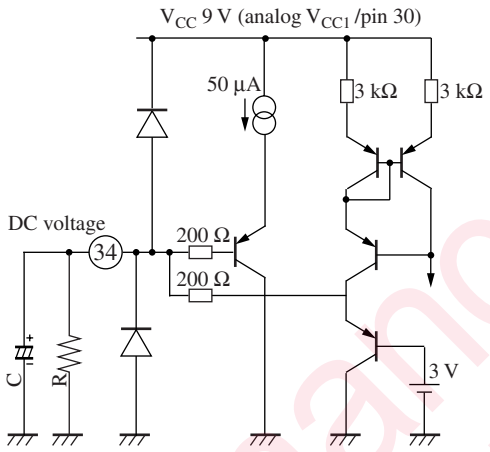
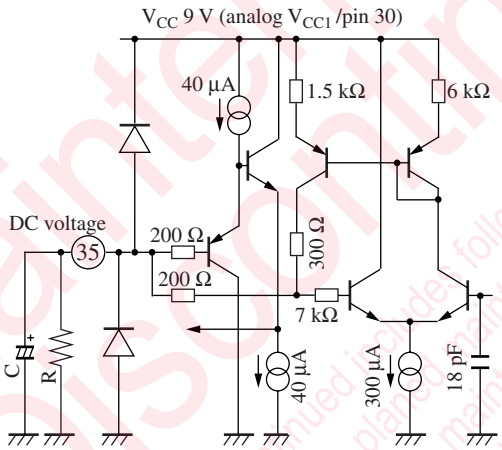
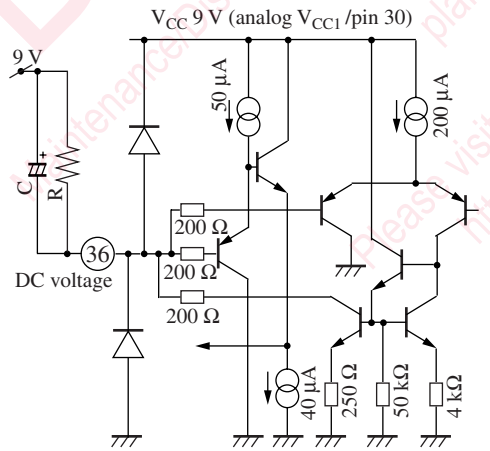
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
20		RGB-S/H: Pin to sample-hold the auto cutoff signal • Use a less-leak capacitor to hold during V period. Also be careful of the leak between pins. • Ground on use if you do not use an auto-cutoff. Pin 20: for B signal Pin 22: for G signal Pin 24: for R signal • Recommended use range: 0 V to 5 V
21	Refer to pin 19	Refer to pin 19
22	Refer to pin 20	Refer to pin 20
23	Refer to pin 19	Refer to pin 19
24	Refer to pin 20	Refer to pin 20
25		IK: IK input pin • Clamps a feed-back input signal of auto cutoff-pulse. • Recommended use range: Do not apply DC voltage from outside.

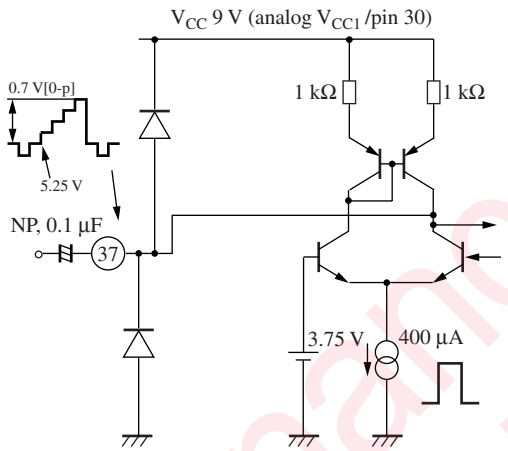
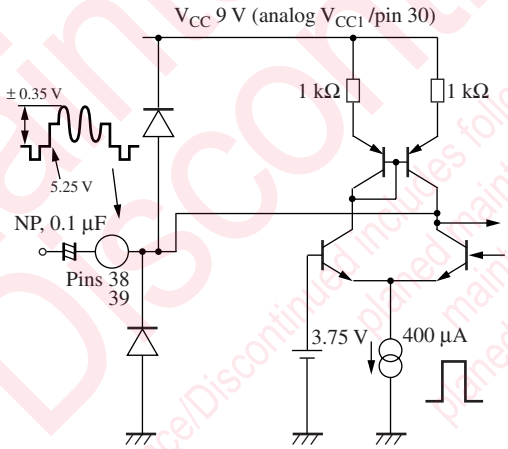
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
26		Blooming level in: • Input pin to determine a blooming level  • Recommended use range: 1.5 V to 5 V
27	Refer to pin 16	Refer to pin 16
28	Refer to pin 16	Refer to pin 16
29		Spot killer in: Spot killer pin • Used to quickly discharge the electricity of the CRT when the set is turned-off. • Raises DC voltage of RGB output pins (pins 19, 21 and 23) when RGB output V_{CC} 9 V (pin 27) becomes low.
30	Refer to pin 16	Refer to pin 16
31 32 33		RGB CLP: Clamps the main signal to the voltage proportioned to brightness data. • Shorten the distance between the pin and the external capacitor. Pin 33: R signal clamp pin Pin 32: G signal clamp pin Pin 31: B signal clamp pin • Recommended use range: 0 V to 5 V (Do not apply DC voltage from outside.)

■ Terminal Equivalent Circuits (continued)

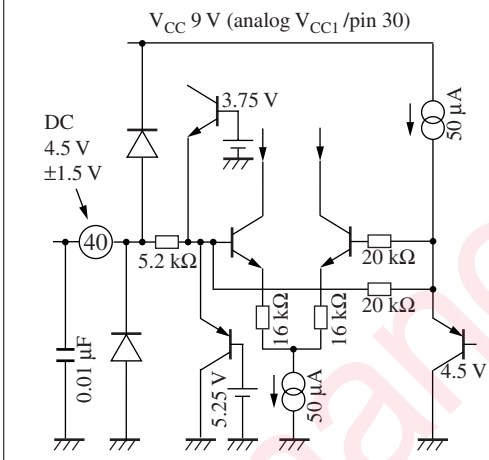
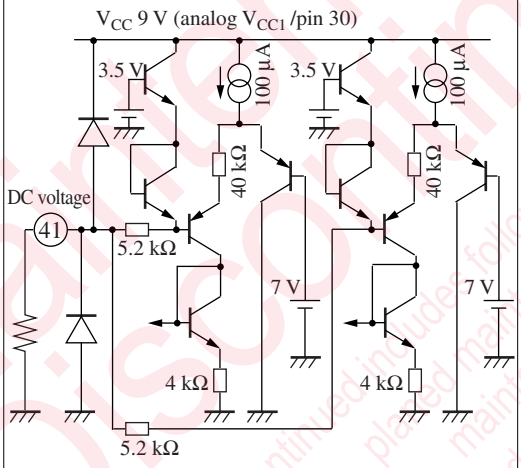
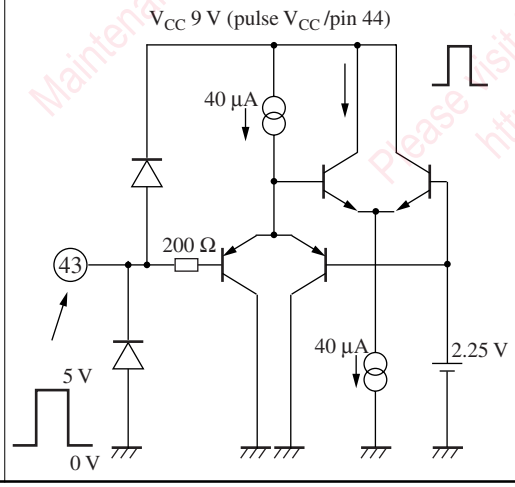
Pin No.	Equivalent circuit	Description
34		APL det.: APL detection pin for main signal • Outputs the voltage proportioned to main signal • Fit an RC filter at this pin. R: For adjusting detection sensitivity C: For adjusting tracking characteristics • Recommended use range: 0 V to 3 V
35		Black peak det.: Detecting the blackest level of main signal • Externally fit an RC filter at this pin. • Corrects a black gradation with this detection voltage R: For adjusting the detection sensitivity C: For adjusting the tracking characteristics • Recommended use range: 0 V to 9 V
36		White peak det.: Detecting the darkest level of main signal • Externally fit an RC filter between this pin and V_{CC}. • Makes a white gradation correction and a blooming control with this detection voltage. R: For adjusting detection sensitivity C: For adjusting tracking characteristics • Recommended use range: 0 V to 9 V

■ Terminal Equivalent Circuits (continued)

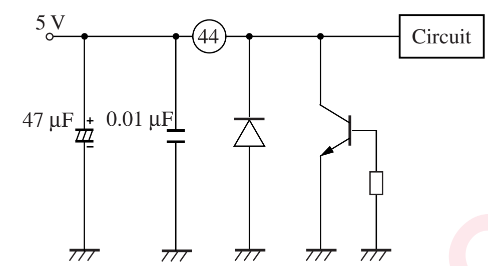
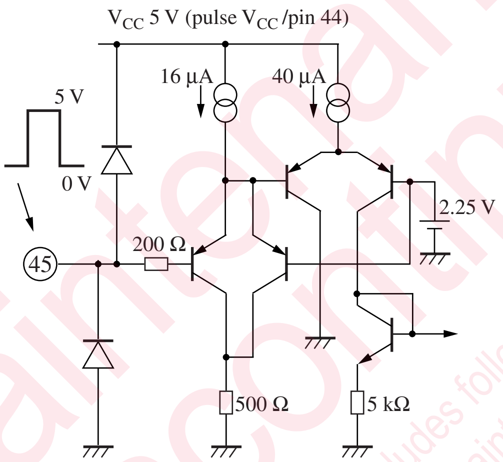
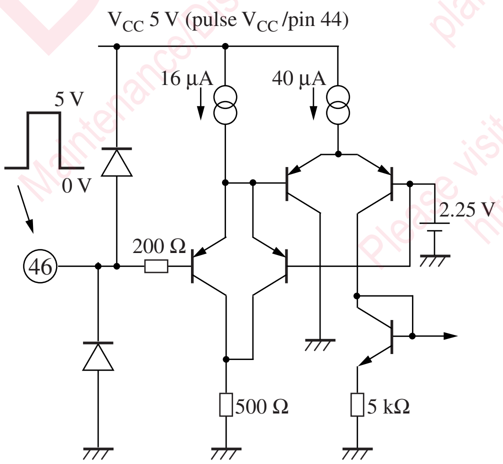
Pin No.	Equivalent circuit	Description
37		Y-in: Y input pin for main signal • Input 0.7 V_{B-W} • Drive this pin with a low impedance. A high impedance is likely to change a white balance for the volume on the user side. • Clamps the input signal with a clamp pulse of pin 43. • Recommended use range: Do not apply DC voltage from outside.
38 39		R−Y in, B−Y in: R−Y, B−Yinput pin for main signal • Pin 38: R−Y signal input pin Pin 39: B−Y signal input pin • Color bar input amplitude at switching the G−Y matrix • Drive this pin with a low impedance. A high impedance is likely to change a white balance for the volume on the user side. • Clamps the input signal with a clamp pulse of pin 43. • Recommended use range: Do not apply DC voltage from outside.

	HD	NTSC	DVD
Pin38	± 0.35 V	± 0.245 V	± 0.35 V
Pin39	± 0.35 V	± 0.312 V	± 0.35 V

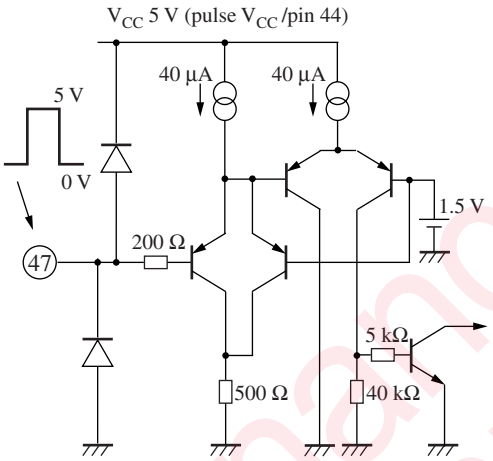
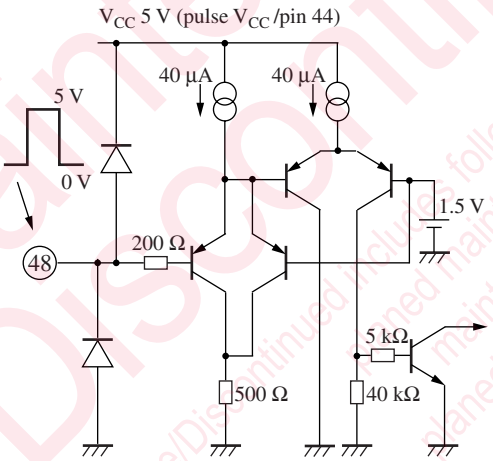
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
40		Chroma γ cont.: External pin for chroma signal γ correction control • Correcting the color level inside the IC in order to adjust Y/C-Y ratio depending on white gradation correction of Y signal. This pin is for external control on this correction value. • Controls the correction value of color level for 2 to 0 times the open mode by means of applied voltage. • Recommended use range: 3.0 V to 6.0 V
41		ABL/ACL in: Control voltage input pin for ABL/ACL • Apply the signal inversely proportional to the screen brightness of CRT. • Operating range is 7 V to 2 V. • Possible to control contrast and brightness in inverse proportion to the applied voltage (Controls the main signal and the OSD signal) • Recommended use range: 0 V to 9 V
42	—	GND: GND pin • Pin 42: Analog GND pin
43		CLP in: Clamp pulse input pin • Input threshold voltage: 1.4 V (to clamp at high) • Clamps the signal inputted from the pins below. Pins 9, 10, 11, 13, 14, 15, 37, 38, 39 • Recommended clamp pulse width: NTSC: 2.5 µs HD: 1.0 µs • Recommended use range: 0 V to 5 V

■ Terminal Equivalent Circuits (continued)

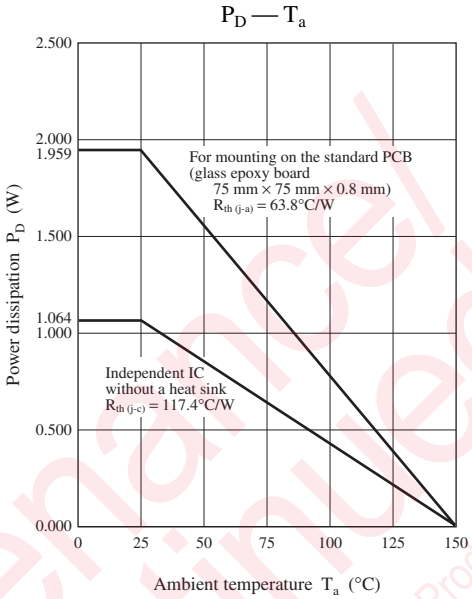
Pin No.	Equivalent circuit	Description
44		V_{CC} 5 V: Pulse-system supply voltage pin • Apply 5 V on use. • Pin 44: Pulse-system supply voltage pin (pair with pin 8 GND) • Recommended use range: 4.5 V to 5.5 V
45		DI in: Input pin for correction inhibition pulse • Input threshold voltage: 1.4 V High: $V_{45} \geq 2.1$ V Low: $V_{45} \leq 0.9$ V • At the input high, the following Y-signal corrections are inhibited. Black gradation correction: Det. and corr. inhibited White gradation correction: Det. and corr. inhibited DC transfer amount correction: Det. and corr. inhibited • In the DI pin input, only detection is inhibited, but correction is left uninhibited. • Recommended use range: 0 V to 5 V
46		BLK in: Blanking pulse input pin • Input threshold voltage: 1.4 V High: $V_{46} \geq 2.1$ V Low: $V_{46} \leq 0.9$ V • Blanking RGB output at input = high • At input = high, the following Y-signal corrections are inhibited: Black gradation correction: Detection and correction inhibited White gradation correction: Detection and correction inhibited DC transfer amount correction: Detection and correction inhibited • At BLK-SW/off, the BLK is released, but the above-mentioned correction is not released. • Recommended use range: 0 V to 5 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
47		HP in: HP pulse input pin • Input threshold voltage: 1.4 V • Does BLK on the RGB output at input = high High input: $V_{47} \geq 2.1$ V Low input: $V_{47} \leq 0.9$ V • The auto cutoff timing pulse is generated by HP pulse. • Recommended use range: 0 V to 5 V
48		VP in: VP pulse input pin • Input threshold voltage: 1.4 V High input: $V_{48} \geq 2.1$ V Low input: $V_{48} \leq 0.9$ V • The data for color, tint, brightness and contrast will be re-written at the time when VP pulse goes high to low. But at DAC SW (V-latch Mode): In the through mode, the data will be rewritten according to the timing sent, regardless of VP pulse. • Auto cutoff timing pulse will be generated according to VP pulse. • Be sure to keep the VP pulse width more than 6H. • Recommended use range: 0 V to 5 V

■ Application Note

1. P_D — T_a curves of QFP048-P-1212B



■ Application Note (continued)

2. I2C bus

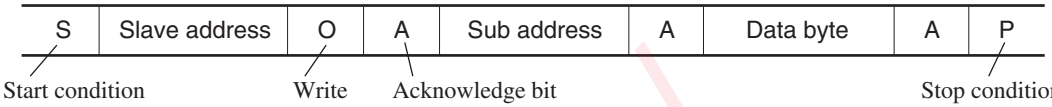
1) Sub address byte and data byte format: ( ) is for initial state.

Sub address	Data byte D7	D6	D5	D4	D3	D2	D1	D0
00 (41H)		Color(V latch)						
01 (41H)		Tint(V latch)						
02 (81H)	Brightness(V latch)							
03 (41H)		Contrast(V latch)						
04 (81H)	Drive R							
05 (81H)	Drive G							
06 (81H)	Drive B							
07 (01H)	Cutoff R							
08 (01H)	Cutoff G							
09 (01H)	Cutoff B							
0A (01H)	Cutoff SW R		Cutoff SW G		Cutoff SW B			
0B (81H)	Color temperature correction R							
0C (81H)	Color temperature correction G							
0D (81H)	Color temperature correction B							
0E (89H)	ACL gain level				ACL start level			
0F (89H)	ABL gain level				ABL start level			
10 (89H)	Black gradation correction gain				Black gradation correction level			
11 (89H)	White gradation correction gain				White gradation correction level			
12 (89H)	White character correction gain				White character correction level			
13 (21H)	G-Y SW		B-Y axis gain					
14 (09H)	Input SW				R-Y axis angle			
15 (09H)					RGB limit			
16 (41H)		R in DC adj.						
17 (41H)	1H/2H changeover	B in DC adj.						
18 (01H)	Single color adjustment R	Single color adjustment G	Single color adjustment B	Blanking off	DC reproduction ratio polarity	White gradation /contrast interlocking	Black gradation /contrast interlocking	Cutoff auto/manual
19 (01H)	Test mode	V-latch through	ACL off	ABL off	White gradation correction off	Black gradation correction off	DC transfer amount correction off	Auto cutoff current changeover

■ Application Note (continued)

2. I²C bus control contents

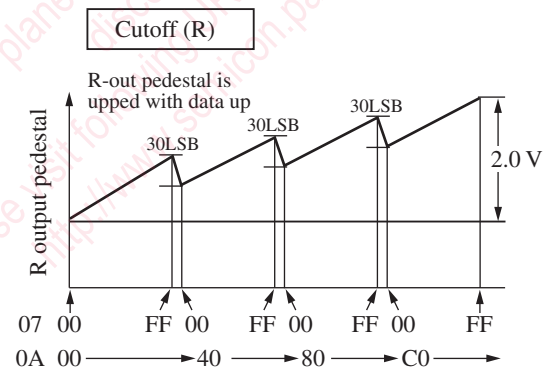
1) I²C bus protocol



2) Slave address
The slave address of this IC is 84H.

3) Since the data status at power on is not guaranteed, be sure to send data to all addresses before using.

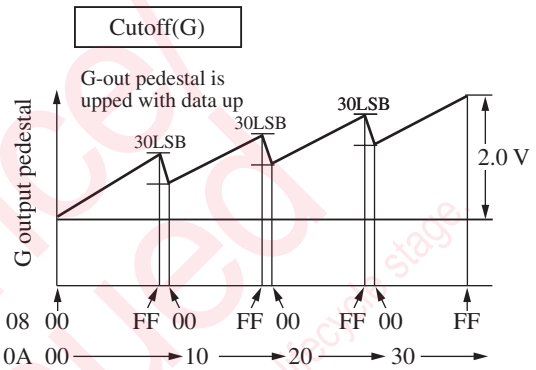
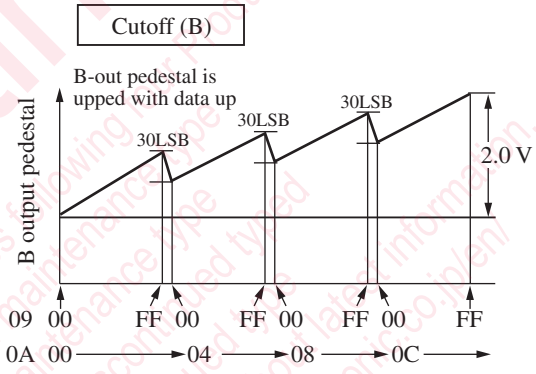
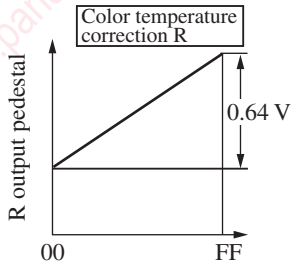
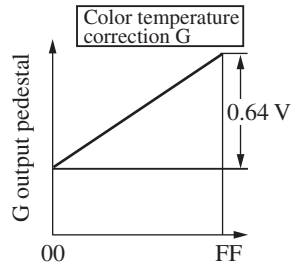
4) Sub-address data

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
Color control	7	00	00 to (40) to 7F	Chroma amplitude upped with data upped Complete iris of data(00) color with	With V latch → Refer to "(5) V latch operation" in ■ Application Note for details.
Tint control	7	01	00 to (40) to 7F	Direction to make the flesh tone red with data(00) Direction to make the flesh tone green with data(7F)	With V-latch
Brightness control	8	02	00 to (80) to FF	Pedestal upped with data upped	With V-latch
Contrast control	7	03	00 to (40) to (7F)	Signal amplitude upped with data upped complete iris of color with data(00)	With V-latch
Drive (R)	8	04	00 to (40) to 7F	R gain upped with data upped	
Drive (G)	8	05	00 to (40) to 7F	G gain upped with data upped	
Drive (B)	8	06	00 to (40) to 7F	B gain upped with data upped	
Cufoff (R)	8 + 2SW	07 + 0A	(00) to 80 to FF 00 to (80) to C0		

■ Application Note (continued)

2. I²C bus control contents (continued)

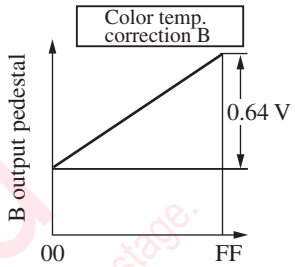
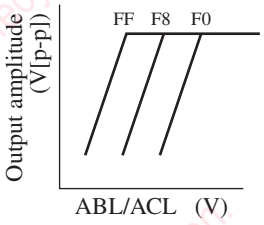
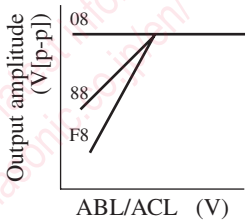
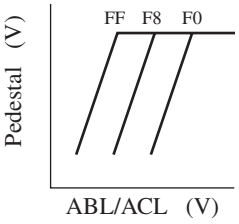
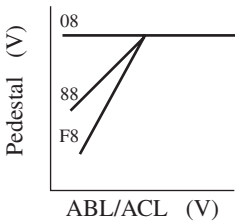
4) Sub-address data (continued)

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
Cutoff (G)	8 + 2SW	08 + 0A	(00) to 80 to FF 00 to (20) to 30	
Cutoff (B)	8 + 2SW	09 + 0A	(00) to 80 to FF 00 to (08) to 0C	
Color temperature correction (R)	8	0B	00 to 80 to (FF) at manual cutoff 00 to (80) to FF at auto cutoff	Used for color temperature correction at manual cutoff. At auto-cutoff, R-out pedestal is upped with data up	
Color temperature correction (G)	8	0C	00 to 80 to (FF) at manual cutoff 00 to (80) to FF at auto cutoff	Used for color temperature correction at manual cutoff. At auto-cutoff, G-out pedestal is upped with data up	

■ Application Note (continued)

2. I²C bus control contents (continued)

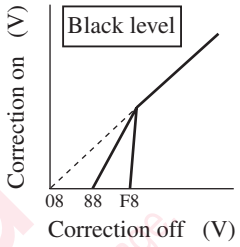
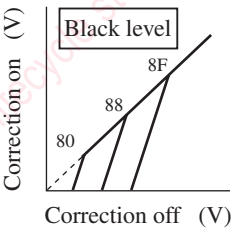
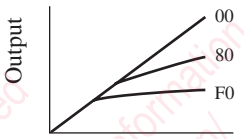
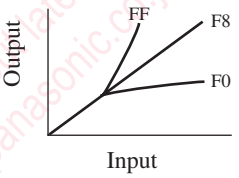
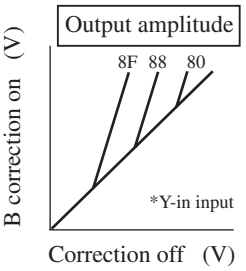
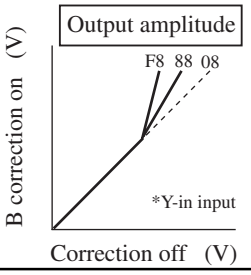
4) Sub-address data (continued)

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
Color temperature correction (B)	8	0D	00 to 80 to (FF) at manual cutoff 00 to (80) to FF at auto cutoff	Used for color temp. correction at manual cutoff. B-out pedestal is upped with data up	
ACL start level	4	0E(L) lower 4-bits	00 to (08) to 0F	Pin 41: Adjusts the start level of output amplitude change against the voltage of ABL/ACL pin	
ACL gain	4	0E(H) upper 4-bits	00 to (80) to F0	Pin 41: Adjusts the start level of output amplitude change against the voltage of ABL/ACL pin	
ABL start level	4	0F(L) lower 4-bits	00 to (08) to 0F	Pin 41: Adjusts the start level of output amplitude change against the voltage of ABL/ACL pin	
ABL gain	4	0F(H) upper 4-bits	00 to (80) to F0	Pin 41: Adjusts the start level of output amplitude change against the voltage of ABL/ACL pin	

■ Application Note (continued)

2. I²C bus control contents (continued)

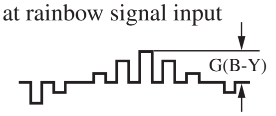
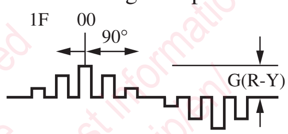
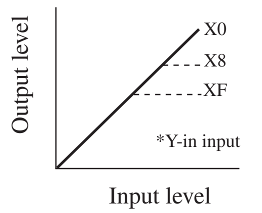
4) Sub-address data (continued)

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
Black gradation correction gain	4	10(H) Upper 4-bit	00 to (80) to F0	Adjusts the gain to be corrected at correcting the black extension	
Black gradation correction start level	4	10(H) Lower 4-bit	00 to (08) to 0F	Adjusts signal level where black extension correction starts	
White gradation correction gain	4	11(H) Upper 4-bit	00 to (80) to F0	Adjusts correction amount at correcting the gamma	
White gradation correction level	4	11(H) Lower 4-bit	00 to (80) to 0F	Adjusts a converging point at correcting the gamma	
White character correction gain	4	12(H) Upper 4-bit	(00) to 80 to F0	Adjusts a detecting(or slicing) level for white characters	
White character correction start level	4	12(H) Lower 4-bit	(00) to 08 to 0F	Adjusts the amount to add the sliced white signal to (B)	

■ Application Note (continued)

2. I²C bus control contents (continued)

4) Sub-address data (continued)

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
B−Y axis gain	6	13	00 to (20) to 3F	Adjusts B−Y gain in accordance with 3 modes of HD/NTSC Data up → $\frac{B-Y}{R-Y}$ Gain ratio up	B-Y output at rainbow signal input  B-Y axis gain = $\frac{G(B\text{-}Y)}{G(R\text{-}Y)}$ G(B-Y) is variable.
G−Y matrix SW	2		11XXXXXX 00XXXXXX	G-Y matrix changeover (Standard/matrix/matrix2) Note) Normally use it at either HD or standard.	Standard (HD): 00 Standard (NTSC, DVD): 11 Matrix 1 (NTSC, DVD): 10 Matrix 2 (NTSC, DVD): 01
R−Y angle adjustment	4	14	(X0) to XF	Carries out R−Y angle adjustment in accordance with matrix changeover data up → 90° (+ 0° to +19°) Note) Normally use it at the angle of 90°	R-Y output at rainbow signal input  R-Y angle adjustment R-Y output peak moves.
Input SW	4		00XXXXXX 11XXXXXX	Output matrix changeover (Standard/matrix/matrix2) Note) Normally use it at standard.	Standard (HD, NTSC, DVD): 00 Matrix 1 (NTSC, DVD): 10 Matrix 2 (NTSC, DVD): X1
			XX00XXXX XX11XXXX	Input signal changeover (HD/NTSC/DVD)	HD: 00 NTSC: 10 DVD: X1
RGB limit	4	15	(X0) to XF	The RGB output limited level is lowered when data is upped.	

■ Application Note (continued)

2. I²C bus control contents (continued)

4) Sub-address data (continued)

DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
R-in DC. adj.	7	16	00 to (40) to 7F	The input clamp voltage of R-in (pin 9) rises with data up.	WB is likely to vary in switching the main and RGB screen within 1H period with a high speed. It is possible to adjust the position error of WB by controlling an input clamp voltage.
B-in DC. adj.	7	17	00 to (40) to 7F	The input clamp voltage of B-in (pin 11) rises with data up.	
1H/2H SW	1		1XXXXXXX 0XXXXXXX	Timing pulse width changeover for auto cutoff. Note) Use it at standard except for progressive scan	1H (normal): 0 2H (progressive scan): 1
Single color adjustment R-off SW12-7	1	18	0XXXXXXX 1XXXXXXX	Blanking R output only.	Normal: 0 R-BLK: 1
Single color adjustment G-off SW12-6	1		X0XXXXXX X1XXXXXX	Blanking G output only.	Normal: 0 G-BLK: 1
Single color adjustment B-off SW12-5	1		XX0XXXXX XX1XXXXX	Blanking B output only.	Normal: 0 B-BLK: 1
Blanking off SW12-4	1		XXX0XXXX XXX1XXXX	Output blanking on/off changeover	With BLK: 0 Without BLK: 1
DC regeneration ratio polarity SW12-3	1		XXXX0XXX XXXX1XXX	(+side)Pedestal down with APL up (−side)Pedestal up with APL up	−: 0 +: 1
White gradation correction/contract interlocking SW12-2	1		XXXXX0XX XXXXX1XX	(On side) White gradation correction level is upped in sequence with contrast up.	Interlocking: 0 Non-interlocking: 1
Black gradation correction/contrast interlocking SW12-1	1		XXXXXX0X XXXXXX1X	(On side) Black gradation correction level is upped in sequence with contrast up.	Interlocking: 0 Non-interlocking: 1
Cutoff manual/ auto SW12-0	1		XXXXXXX0 XXXXXXX1		Auto: 0 Manual: 1

■ Application Note (continued)

2. I²C bus control contents (continued)

4) Sub-address data (continued)

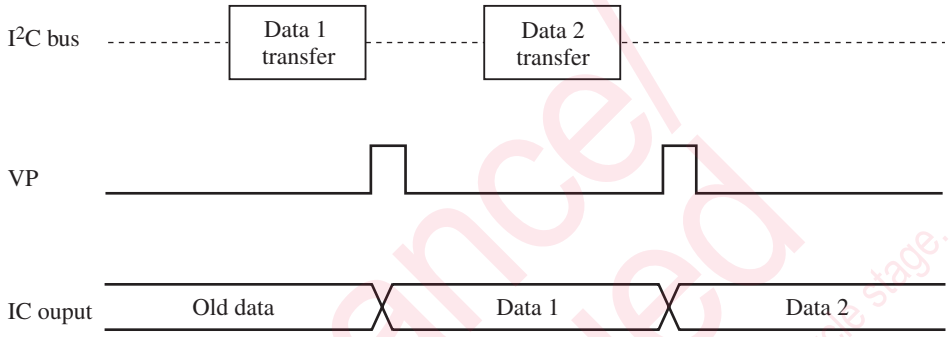
DAC name	bit	Sub address(H)	Data address(H) ( )Standard status	Operation	Remarks
DAC mode SW19-7	1	19	0XXXXXXX 1XXXXXXX	Bits for inspection Be sure to use it with 0	
V-Latch mode SW19-6	1		X0XXXXXX X1XXXXXX	Through mode changeover for V-latch DAC	Normal: 0 Through: 1
ACL SW19-5	1		XX0XXXXX XX1XXXXX	ACL on/off changeover	On: 0 Off: 1
ABL SW19-4	1		XXX0XXXX XXX1XXXX	ABL on/off changeover	On: 0 Off: 1
White gradation correction SW19-3	1		XXXX0XXX XXXX1XXX	White gradation correction on/off changeover	On: 0 Off: 1
Black gradation correction SW19-2	1		XXXXX0XX XXXXX1XX	Black gradation correction on/off changeover	On: 0 Off: 1
DC transmission amount correction SW19-1	1		XXXXXX0X XXXXXX1X	DC transfer amount on/off changeover	On: 0 Off: 1
Auto cuttoff current changeover SW19-0	1		XXXXXX0X XXXXXX1X	Auto cutoff current changeover to large/small	Small current: 0 Large current: 1

■ Application Note (continued)

2. I²C bus control contents (continued)

5) V-latch operation

(Function) The data for sub-address 00 to 03 remains unchanged until VP pulse comes.



6) Auto increment: This IC performs the designation of sub address by using the lower 5 bits. The uppermost bit is used for designation of auto increment.

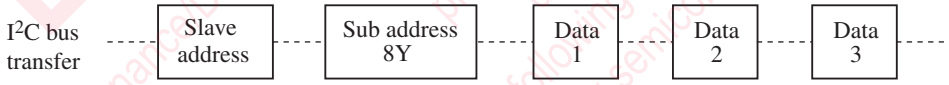
- When the sub address uppermost bit is defined as 0 (sub address: 00 to 19 HEX)

The sequential data transfer leads to the sequential change of sub address, then the data is inputted.

Sub address	Input data
X	Data 1
X + 1	Data 2
X + 2	Data 3

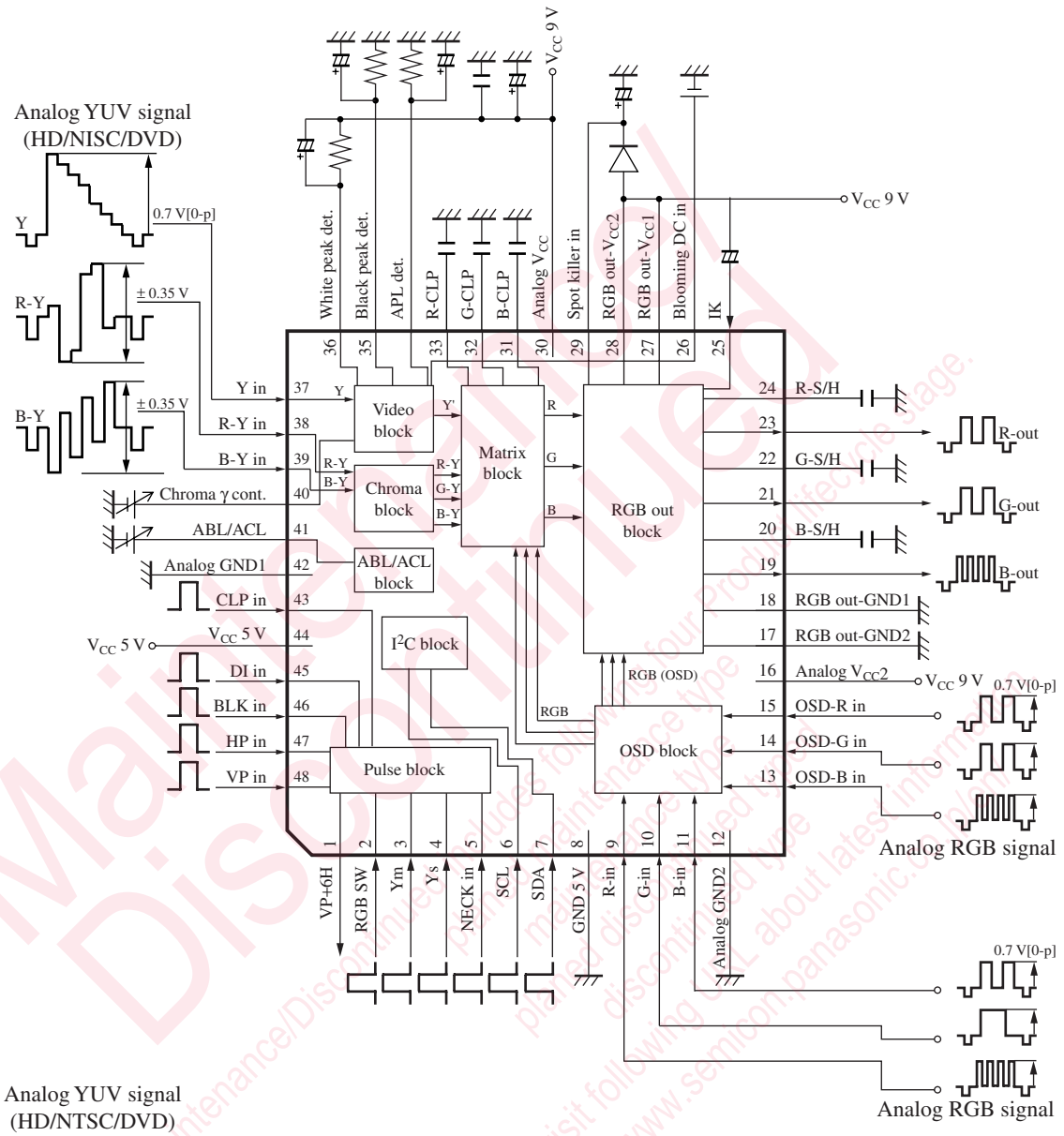
The data is inputted as above. But the data will be invalid after sub address 1A.

- When the sub address uppermost bit is defined as 1 or sub address is 80 to 99 HEX, the sequential data transfer leads to data input on the same address.



Sub address	Input data
8Y	Data 1
8Y	Data 2
8Y	Data 3

■ Application Circuit Example

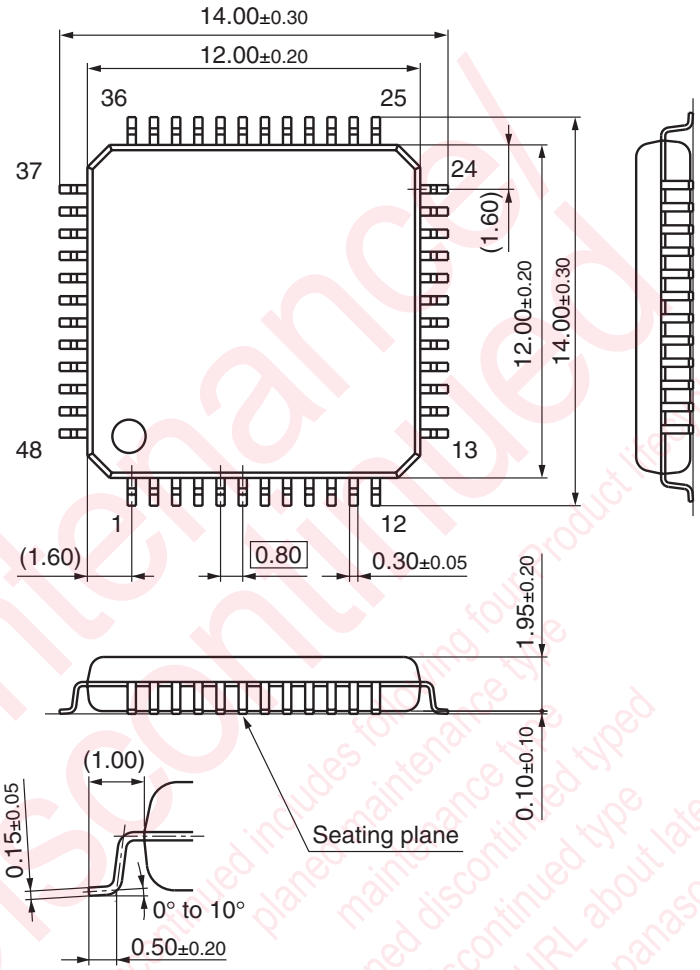


Video signal	
HD	NTSC/DVD
Y: 700, 650, 551, 501, 199, 149, 50	Y: 700, 623, 490, 413, 287, 210, 77

Chrominance signal		
HD	NTSC	DVD
Pr: 350, 318, 32, 0, −32, −318, −350	R-Y: 490, 413, 77, 0, −77, −413, −490, 623	Cr: 350, 295, 55, 0, −55, −295, −350
Pb: 350, 270, 80, 0, −80, −270, −350	B-Y: 413, 210, 0, −210, −413, −623	Cb: 350, 232, 118, 0, −118, −232, −350
Y = 0.2125R + 0.7154G + 0.0721B Pr = 0.6349(R-Y) Pb = 0.5389(B-Y)	Y= 0.3R + 0.59G + 0.11B	Y = 0.3R + 0.59G + 0.11B Cr = R-Y/1.4 Cb= B-Y/1.78

■ New Package Dimensions (Unit: mm)

• QFP048-P-1212C (Lead-free package)



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