Power MOSFET Basics: Understanding MOSFET Characteristics Associated With The Figure of Merit

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INTRODUCTION

Power MOSFETs have become the standard choice as the main switching device for low-voltage (<200 V) switchmode power-supply (SMPS) converter applications. However using manufacturers' datasheets to choose or size the correct device for a specific circuit topology is becoming increasingly difficult. The main criteria for MOSFET selection are the power loss associated with the MOSFET (related to the overall efficiency of the SMPS) and the power-dissipation capability of the MOSFET (related to the maximum junction temperature and thermal performance of the package). This application note focuses on the basic characteristics and understanding of the MOSFET.

There are several factors which affect the gate of the MOSFET, and it is necessary to understand the fundamental basis of the device structure before the MOSFET behavior can be explained. This application note details the basic structure of the Trench MOSFET structure, identifying the parasitic components and defining related terminology. It also describes how and why the parasitic parameters occur.

With a large variety of topologies, switching speeds, load currents, and output voltages available, it has become impossible to identify a generic MOSFET that offers the best performance across the wide range of circuit conditions. In some circumstances the on-resistance ($r_{DS(on)}$) losses dominate, and in others it is the switching losses of the transient current and voltage waveforms, or the losses associated with driving the gate of the device. It also has been shown[1,2] that the input and output capacitances can be the dominant loss.

INTRODUCING THE FIGURE OF MERIT FOR MOSFET SELECTION

To add to this confusion, device manufacturers specify MOSFET parameters at different static and dynamic conditions, diminishing designers' ability to compare like for like. Therefore, the only true method of making the correct MOSFET choice is to compare a selection of devices within the circuit in which the MOSFET will be used.

There are methods available that, though sometimes difficult to implement, enable the designer to compare MOSFETs that appear suited for a given application. One method for evaluating MOSFETs is according to "figure of merit." In its simplest form, the figure of merit compares gate charge (Q_g) against $r_{DS(on)}$. The result of this multiplication relates to a certain device technology, which is effectively scalable to achieve the required $r_{DS(on)}$ or Q_g. However, the lower the $r_{DS(on)}$ the higher the gate charge will be. A similar method for comparing devices is the "Baliga high-frequency figure of merit," BHFFOM[1], which assumes that the dominant switching loss will be associated with the charging and discharging of the input capacitance (C_{iss}). A third method uses the "new high-frequency figure of merit," NHFFOM[2], which assumes that the dominant switching loss is due to the charging and discharging of the output capacitance (C_{oss}). The latter two methods are geared towards the applications in which the MOSFETs will be implemented. However, these methods only allow like-for-like comparisons; they do not enable the user to determine that a device with one figure of merit is necessarily better than a different device with another.

Figure 1 shows the Q_g x $r_{DS(on)}$ figure of merit for a sample of Vishay Siliconix's range of 30-V SO-8 n-channel MOSFETs. The Si4888DY, for example, may be better in certain switching applications than the Si4842DY, but it is not possible to use this graph—or other graphs using more complex figures of merit—to determine objectively the best device for a specific application.

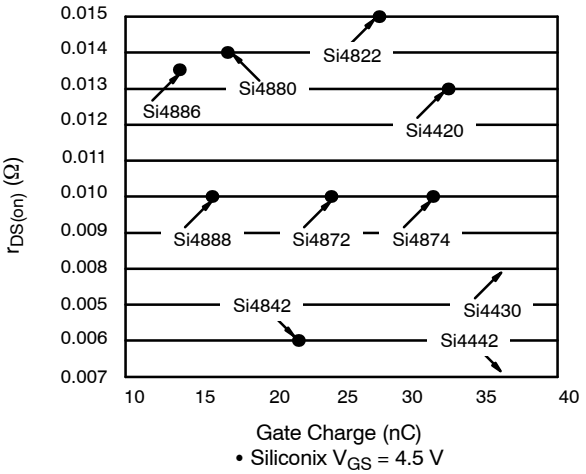

FIGURE 1. Typical figure of merit for Vishay Siliconix n-channel, 30-V SO-8 MOSFETs

1. IEEE Electron Device Letters, Vol. 10, No. 10, October 1989, "Power Semiconductor Device Figure of Merit for High Frequency applications," B. Jayant Baliga.
2. Proc. of 1995 Int. Sym. on Power Semiconductor Devices and ICs, Hokohama, "New Power Device Figure of Merit for High-Frequency Applications," IL-Jung Kim, Satoshi Mastumoto, Tatsuo Sakai, and Toshiaka Yachi.

MOSFET STRUCTURE

Table 1 identifies the common definitions of the majority of the MOSFET parameters and parasitics found in a Trench MOSFET.

TABLE 1
Definitions of MOSFET Parameters

Symbol	Description
R_B	Base resistance
R_g	Gate resistance internal to the MOSFET
C_{gs}	Capacitance due to the overlap of the source and channel regions by the polysilicon gate. Independent of applied voltage.
C_{gd}	Consists of two parts: 1.. Associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. Independent of applied voltage. 2.. The capacitance associated with the depletion region immediately under the gate. Non-linear function of voltage. This provides a feedback loop between the output and input circuit. It is called the Miller Capacitor because it causes the total dynamic input capacitance to become greater than the sum of the static capacitors.
C_{ds}	Capacitance associated with the body drift diode. Varies inversely with the square root of the drain source bias.
BV_{DSS}	Voltage at which the reverse-biased body drift diode breaks down and a significant current starts to flow between source and drain by the avalanche multipication process, while the gate and source are shorted together. This is normally measured at 250-µA drain current.
$r_{DS(on)}$	On-state resistance for Trench. Equals $R_{SOURCE} + R_{CH} + R_A + R_D + R_{sub} + R_{wcl}$
R_{SOURCE}	Source diffusion resistance
R_{CH}	Channel resistance
R_A	Accumulation resistance
R_J	JFET component resistance
R_D	Drift-region resistance
R_{sub}	Susbtrate resistance
R_{wcl}	Bond wire, contact and leadframe resistance (significant in low-voltage devices)
g_{fs}	Transconductance, a measure of the sensitivity of drain voltage to changes in gate-source bias. Normally quoted for a V_{GS} that gives a drain current equal to $^1/_2$ of maximum current and for V_{DS} that ensures operation in the constant-current region. Note: g_{fs} is influenced by gate width, which increases in proportion as cell density increases. Reduced channel length is beneficial to both g_{fs} and $r_{DS(on)}$.
C_{iss}	Input capacitance. Equals $C_{gs} + C_{gd}$ with C_{ds} shorted.
C_{rss}	Reverse transfer capacitance, C_{gd}
C_{oss}	Output capacitance. Equals $C_{ds} + C_{gd}$
Q_g	Total gate charge. The amount of charge consumed by the capacitance of gate
Q_{gs}	Gate source charge. The charge consumed by the gate source capacitance.
Q_{gd}	Gate drain charge. The charge consumed by the gate drain capacitance.

The foundations of any power MOSFET device can be derived from the vertical planar DMOS technology. Currents emanating from the source flow laterally along the surface, then turn and flow in a perpendicular direction away from the surface between adjacent body diffusions, through the epitaxial drain, into the substrate, and out of the wafer backside. The channel is formed under the polysilicon gate layer along the planar surface. However, the planar structure has an effective finite level of cell density because the JFET pinch-off effect[3] leads to an increased device on-resistance, compared with the Trench structure, at very high cell densities.

With such electrical and geometric restrictions, further increases to planar DMOS cell density above 30 million cells/inch^2 are not only unwarranted, but also likely to be detrimental to performance. Only by eliminating the pinching effect can cell reductions significantly benefit MOSFET on-resistance.

To overcome the planar pinch-off problem, device designers at Vishay Siliconix implemented the trench-gate vertical power MOSFET, or TrenchFET®. Rather than conduct current along the surface, the TrenchFET conducts via a channel formed vertically along the sidewall of a trench etched into the silicon.

A Trench DMOS cross-section is shown in Figure 2. Using a closed cell pattern similar to that of planar DMOS, the trench forms a grid surrounding islands of silicon. Each silicon island is the location of a double diffused channel region and its associated source diffusion.

The trench is oxided, then filled with a conductor and planarized to form the device gate.

With this trench technology, it is feasable to increase the cell density without any JFET pinch-off effects, and as such, high cell densities (>200 million cells/inch^2) are achievable. It is beneficial to have incremental steps up to this level of cell density, thereby creating a family of devices balancing ultra-low on-resistance, gate characteristics, and cost. However, the increase in die per wafer, which improves cost benefits, and reduction in $r_{DS(on)}$, which improves performance, remain the two most compelling advantages.

Figure 3 shows a cross-section of the MOSFET Trench die at a density of 178 million cells/inch^2. This is a slice through the actual ultra-high-density cell wafer in an area that demonstrates the high-density cell scaling. To achieve such a cell figure, the focus has been placed on both the lateral and vertical cell scaling, optimizing not only the $r_{DS(on)}$ but also the gate characteristics.

Along with advances in lateral scaling designed to increase the cell density, there also have been improvements in the associated capacitance, Figure 3b, to enhance fast switching, which is essential for high-frequency operation (>400 kHz). Also at light current loads, the gate drive losses become a significant contributing factor to the overall system efficiency, so the gate capacitances must be taken into consideration.

The vertical scaling improvements have achieved lower capacitance, resulting in lower merit values of $r_{DS(on)} \times Q_g$ of <100 (mΩ x nC).

3. "A Fivefold Increase in Cell Density Sets the New Milestone in TrenchFET® Device Performance," G. Moxey and M. Speed. PCIM, 2001.

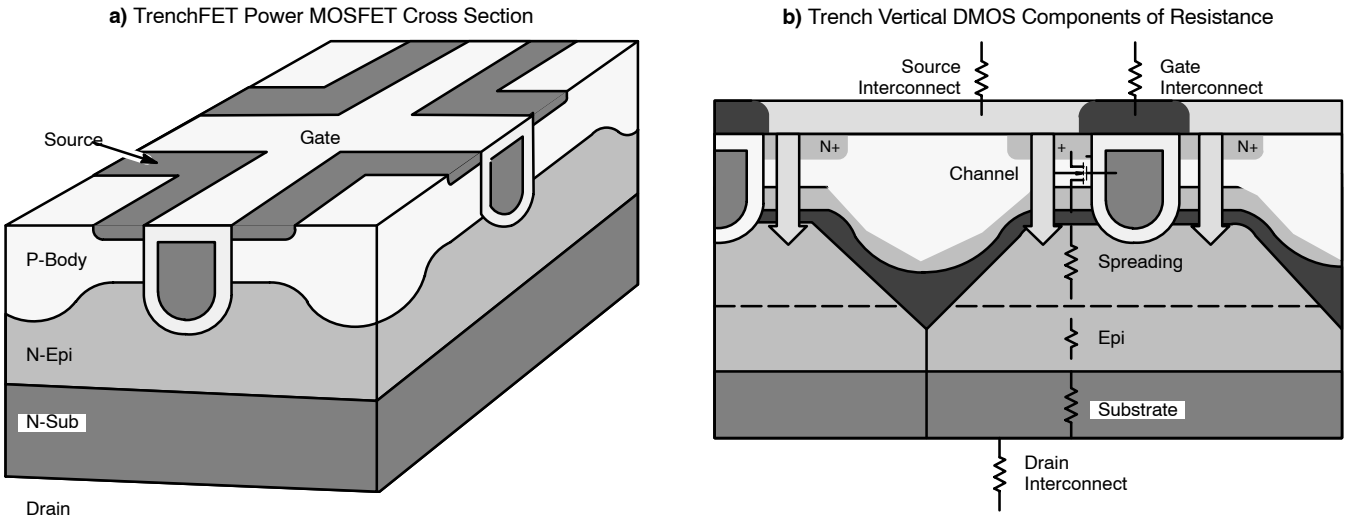

FIGURE 2. Trench DMOS 3D cross-section, with associated resistive elements.

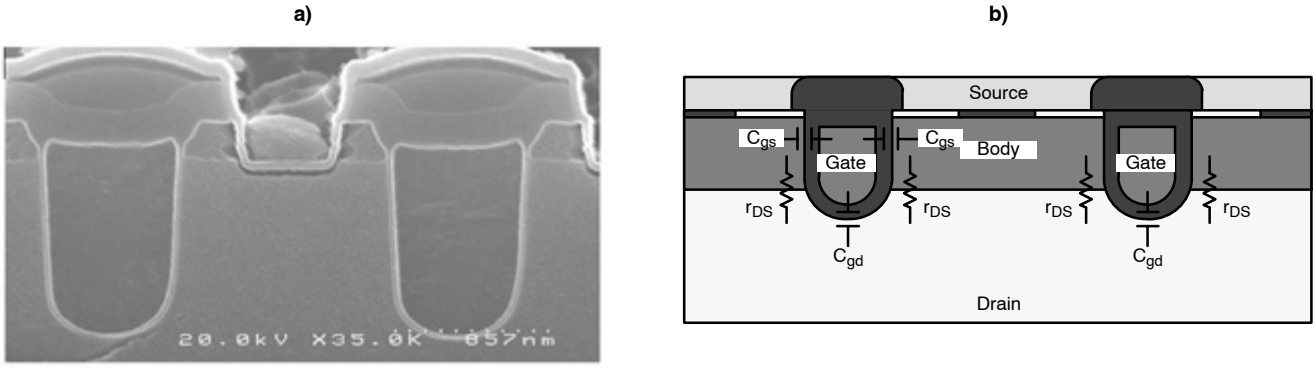

FIGURE 3. Ultra-high-density die cross-section with equivalent parasitic parameters

The on-resistance of the DMOS Trench MOSFET is the sum of all the individual regions through which the mobile carriers must flow (as shown in Figure 2).

$$r_{DS(on)} = R_{SOURCE} + R_{CH} + R_A + R_D + R_{sub} + R_{wcl} \quad (1)$$

It should be noted that for a Planar MOSFET, the $r_{DS(on)}$ figure also includes the JFET component resistance.

PARASITIC CAPACITANCE IN A MOSFET

The simplest view of an n-channel MOSFET is shown in Figure 4, where the three capacitors, C_{gd}, C_{ds}, and C_{gs} represent the parasitic capacitances. These values can be manipulated to form the input capacitance, output capacitance, and transfer capacitance, as described in Table 1.

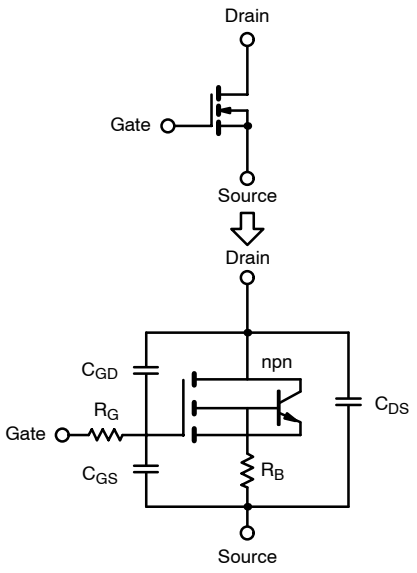

FIGURE 4. Simple equivalent circuit for a n-channel MOSFET, showing the parasitic capacitance, npn transistor and R_b resistor.

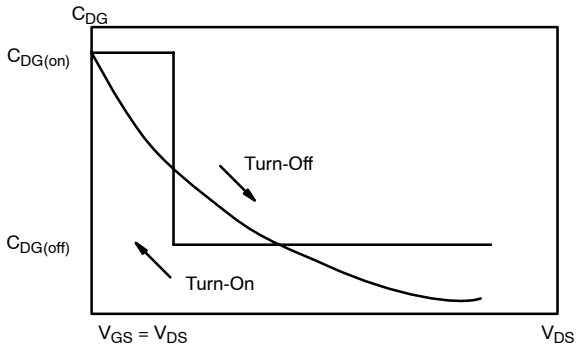

FIGURE 5. Gate-drain capacitance over the drain-source voltage range

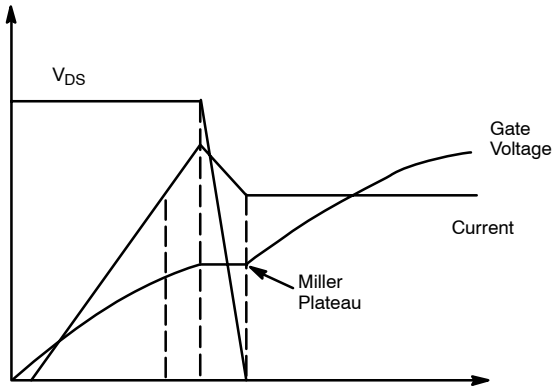

FIGURE 6. Gate voltage and respective voltage and current during turn-on

However, it should be noted that because the equivalent circuit is much more complex than a resistor and three capacitors, these capacitances may only be used for understanding the behavior of the switching transients.

The gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} are voltage-dependent capacitances, and therefore the capacitance value changes depending on the voltage that appears across the drain source and also across the gate source of the device. The change in C_{gd} is more significant than C_{gs}, simply because the voltage that appears across it is much larger than that seen across C_{gs}. The change in C_{gd}[4], shown in Figure 5, can be as large as a factor of 100 and usually is approximated to two static values. These changes in capacitance have an influence on the voltage that appears at the gate of the device, called the Miller Plateau[4]. This causes the turn-off and turn-on rise and fall times on the switching transients and causes the gate voltage to “flatten out” as shown in Figure 6.

CONCLUSIONS

This application note is the first in a series of technical documents describing the basic characteristics and operating performance of the power MOSFET when implemented in a switched-mode power supply. It is intended to give the reader a thorough background on the device technology behind Vishay Siliconix MOSFETs.

The FOM does not in itself enable the power supply designer to choose the ideal device, but does give an overview of the device technology and possible performance. To give a definitive and subjective analysis, every FOM would have to be modified to include information on the application in which the MOSFET was to be used. Therefore the application note defines the principle characteristics (Table 1), which need to be taken into account when choosing the correct device for a specific application.

4. “Power Electronics, converters, Applications and Design,” Mohan, Underland and Robbins. ISBN 0-471-58404-8.