

## A SIMPLE ALTERNATIVE TO ANALOG ISOLATION AMPLIFIERS

### 1. Introduction

Analog circuits sometimes require linear (analog) signal isolation for safety, signal level shifting, and/or ground loop elimination. Linear signal isolation is typically difficult to implement, costly, and often exhibits mediocre performance. While the design community thirsts for a flexible and inexpensive linear isolator solution, it is the analog isolation amplifier (ISOamp) that most often captures the socket.

ISOamps are hybridized devices that contain linear input and output circuits separated by an internal isolation barrier. ISOamps typically modulate the linear input signal and transmit the resulting digital information across the isolation barrier to a demodulator where it is converted back to analog (Figure 1). ISOamps typically employ transformers and high-voltage capacitors or optocouplers in the isolation barrier design. While ISOamps are a convenient single-package linear isolation solution, the industry's limited device offerings often force the designer to make difficult trade-offs or add external circuitry for a complete solution. In addition, transformer-based ISOamps are susceptible to signal corruption from external field interference and errors due to poor common-mode transient immunity (CMTI). Optocoupler-based ISOamp versions also often suffer from poor linearity and even worse CMTI. This application note provides insight into a robust linear isolator reference design based on the Silicon Labs Si86xx family of CMOS digital isolators.

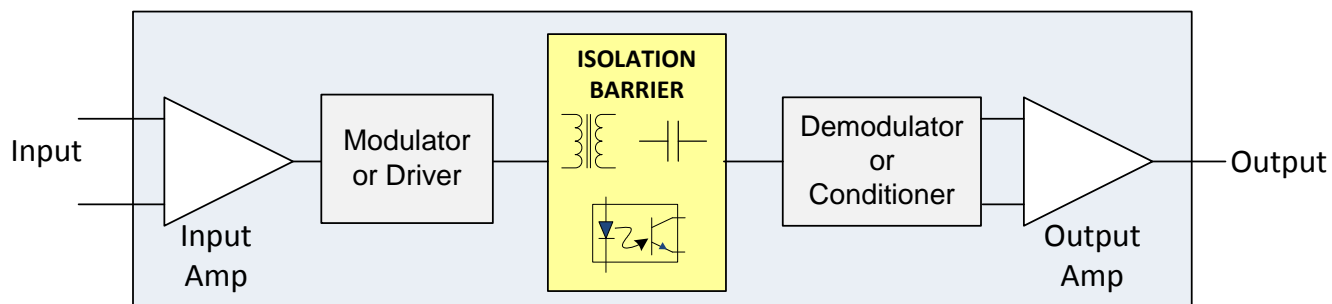


Figure 1. ISOamp Block Diagram

## 2. Silicon Labs' ISOLinear Reference Design Overview

Silicon Labs offers the ISOLinear reference design (Si86IsoLin), a simple linear isolation circuit that is enabled by the Si86xx isolator family, offering industry-leading integration, operating performance, and reliability. The Si86xx isolators are available in UL/VDE/CSA certified isolation ratings of 2.5 or 5 kV. The ISOLinear reference design architecture is shown in Figure 2. A self-oscillating pulse width modulator (PWM) converts the linear input voltage into a series of fixed-frequency, variable duty, cycle pulses in which the width of each pulse is proportional to the sampled input signal amplitude as shown in the waveform diagrams at the bottom of Figure 2. This modulated (digital) signal is passed through the CMOS digital isolator and then restored to analog format by a fourth-order analog filter.

Unlike ISOamps, the ISOLinear reference design gives the designer flexibility to craft low-cost, linear isolators that meet the needs of the end application. For example, the user may elect to relax output ripple requirements to use a lower order (lower cost) output filter; or modulator performance can be enhanced if higher slew rate op-amps and/or low-delay comparators are used, and so on.

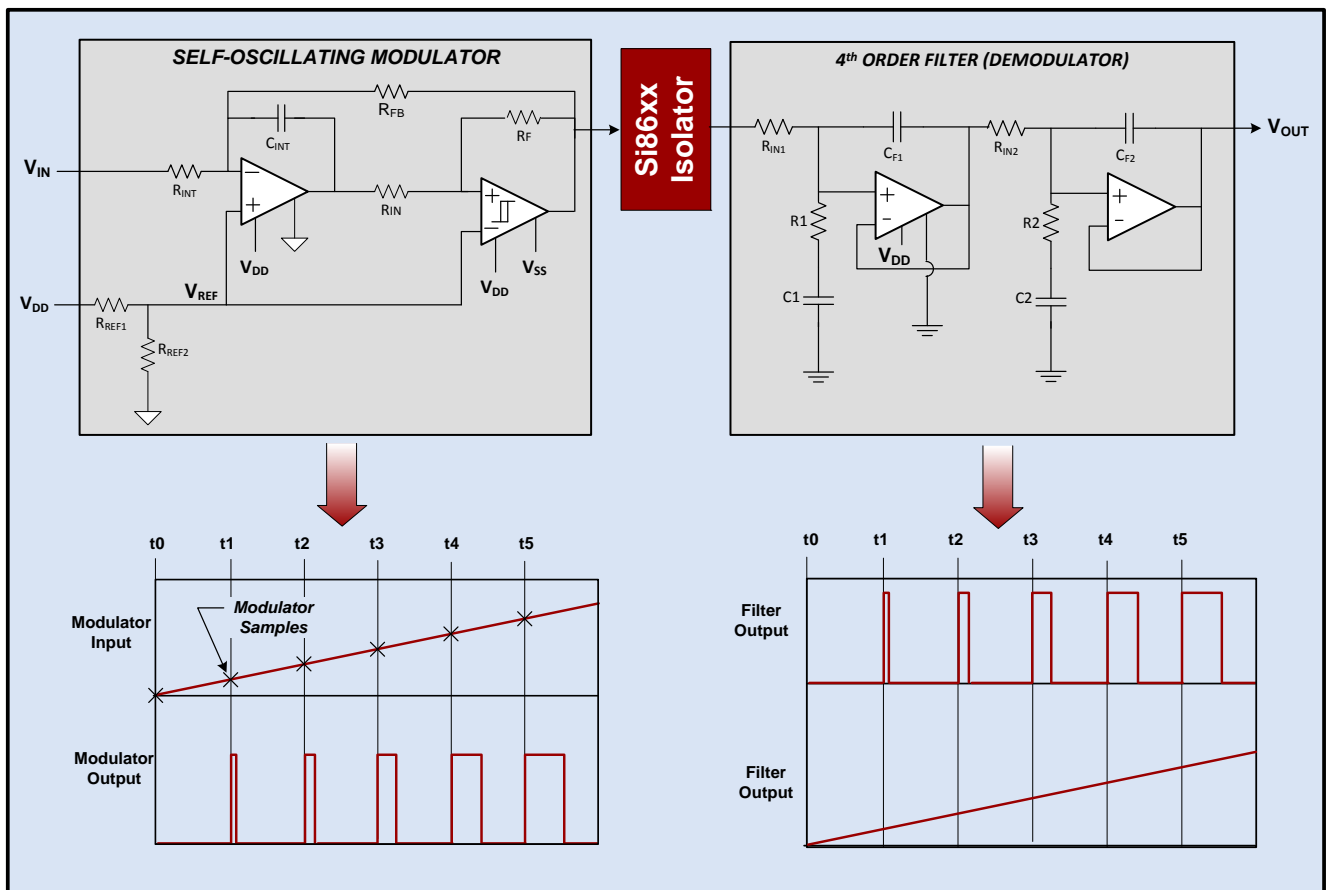
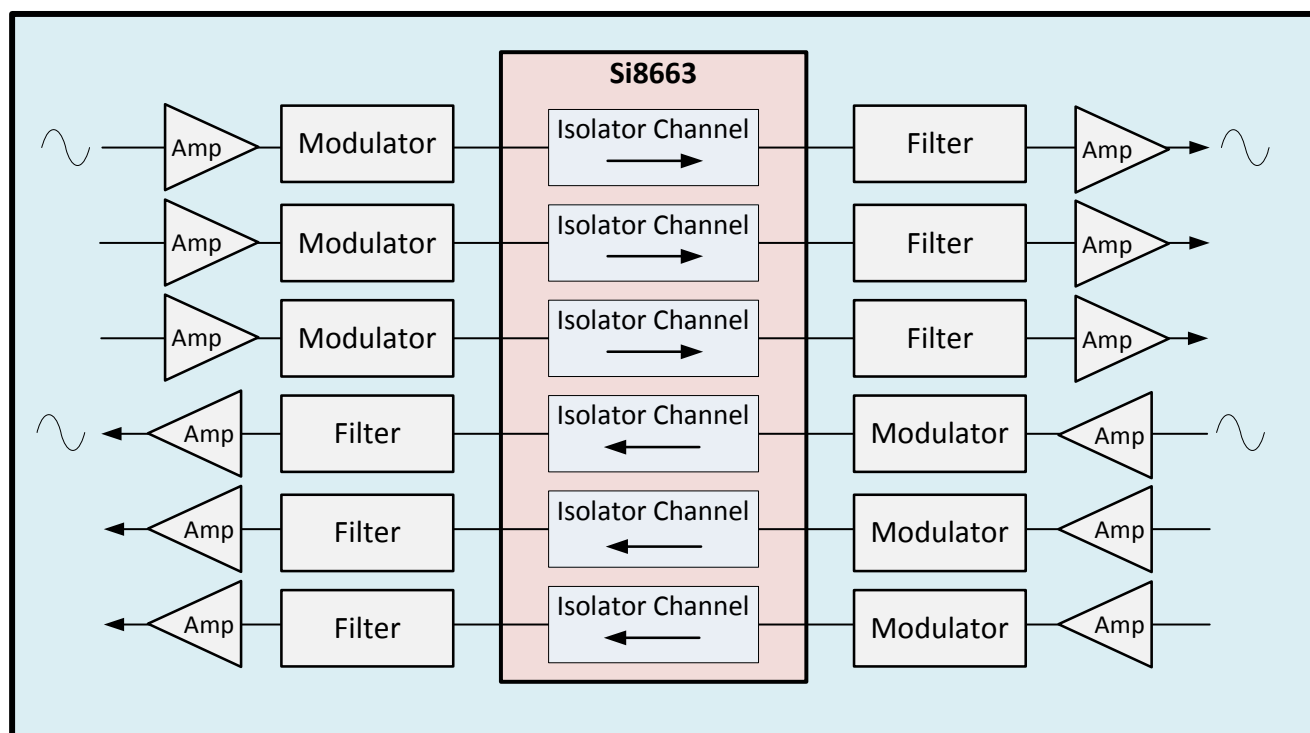
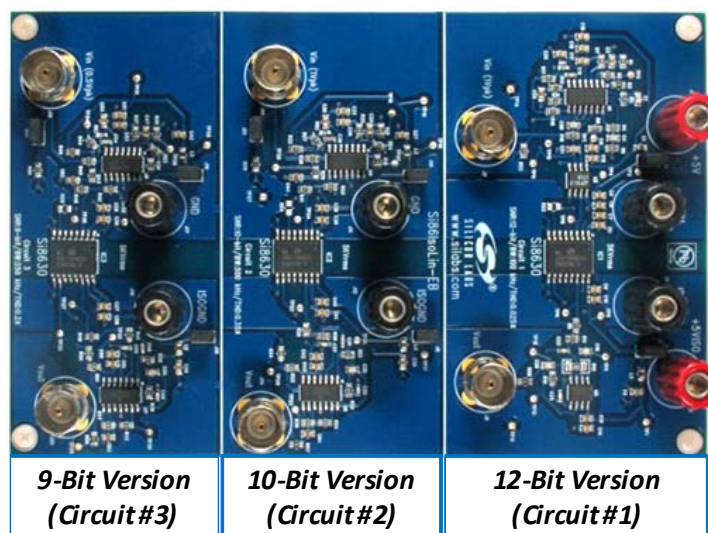


Figure 2. ISOLinear Reference Design Schematic and Operation



**Figure 3. Six-Channel Linear Isolator Block Diagram**

In addition, a single Si86xx isolator can host multiple linear isolators by adding additional modulator/filter circuits to a multi-channel Si86xx digital isolator, as shown in Figure 3. In this example, an Si8663 six-channel digital isolator provides three forward and three reverse linear isolator channels, amortizing the isolator across all six channels.

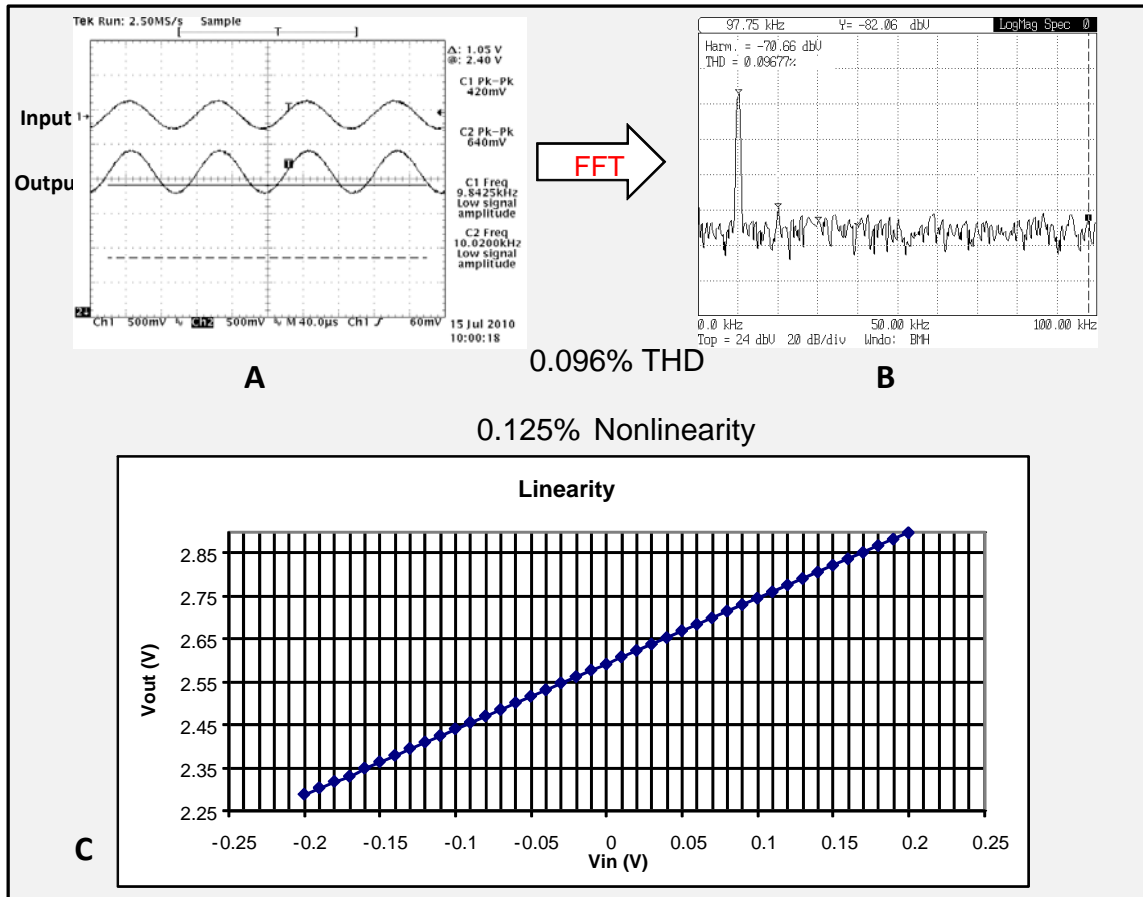


**Figure 4. ISOLinear Reference Design Evaluation Board**

Figure 4 shows the board included in the ISOLinear reference design kit. This board contains reference design configurations for 9-bit, 10-bit, and 12-bit linear isolator performance, enabling the user to optimize isolator cost/performance trade-offs. (For detailed circuit ISOLinear reference design schematics, see the “ISOLinear Reference Design Users Guide” available for download at [www.silabs.com/isolation](http://www.silabs.com/isolation).)

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Figure 5 shows total harmonic distortion and nonlinearity measurements from the evaluation board of Figure 4. Waveform A shows the ISOLinear input and output oscilloscope waveforms. The FFT of waveform A reveals a total harmonic distortion (THD) of 0.096% (waveform B). The performance of this design rounds to 12-bit performance with 0.125% nonlinearity. (Note: for more information about the ISOLinear Reference Design, please see application note “AN559: Isolating Analog Signals Using the Si86xx CMOS Isolator Family”. This application note provides detailed technical information for modifying the stock ISOLinear reference design, including modulator and filter design equations, design guidelines and more. The ISOLinear Reference Design Kit (Si86IsoLin) is available for purchase at [www.silabs.com/isolation](http://www.silabs.com/isolation).)



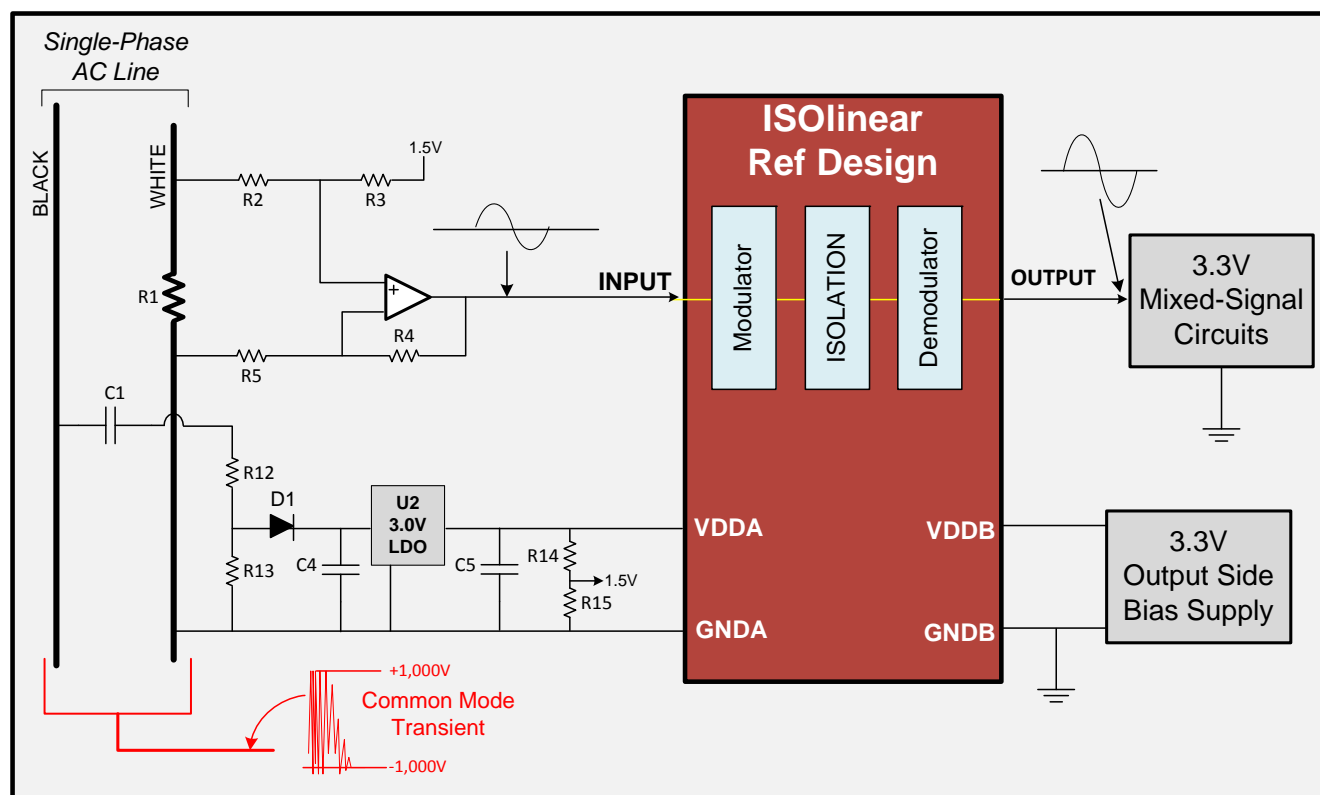
**Figure 5. ISOLinear Reference Design Performance Example**

Table 1 compares the ISOLinear reference design performance against several commercially-available ISOamps. The ISOLinear reference designs offer higher signal-to-noise (sans the 9-bit version); higher CMTI, greater isolation rating flexibility and lower cost compared to competing ISOamps. (Note: a higher cost, faster comparator can be used to reduce nonlinearity to less than 0.1%.)

Table 1. ISOlinear vs. Analog Isolation Amplifiers

| Device   | SNR (dB)      | BW (kHz) | Linearity | Isolation Rating (kV) | CMTI (kV/ $\mu$ s)    | Price at 1 kU (\$) |
|--|---------------|----------|-----------|-----------------------|-----------------------|--------------------|
| Silicon Labs <i>ISOlinear</i><br>(12-Bit Reference Design) | 71.8          | 100      | 0.125     | 2.5 or 5.0            | 35 (min),<br>50 (typ) | 2.50 to 3.50       |
| Silicon Labs <i>ISOlinear</i><br>(10-Bit Reference Design) | 62            | 250      | 0.125     | 2.5 or 5.0            | 35 (min),<br>50 (typ) | 2.00 to 2.50       |
| Silicon Labs <i>ISOlinear</i><br>(9-Bit Reference Design)  | 50.8          | 500      | 0.125     | 2.5 or 5.0            | 35 (min),<br>50 (typ) | 1.75 to 2.25       |
| Avago HCPL-7840  | Not Specified | 100      | 0.1       | 2.5                   | 15                    | 3.05               |
| Avago ACPL-790   | 60            | 200      | 0.05      | 5.0                   | 15                    | 6.63               |
| Avago ACPL-780   | Not Specified | 100      | 0.004     | 5.0                   | 15                    | 7.30               |
| Avago ACPL-C79A  | 60            | 200      | 0.05      | 5.0                   | 15                    | 10.00              |
| Avago ACPL-C790 ( $\Delta \Sigma$ )                        | 60            | 200      | 0.05      | 5.0                   | 15                    | 4.65               |
| TI ISO-124   | Not Specified | 50       | 0.01      | 1.5                   | Not Specified         | 8.30               |
| ADIAD202   | Not Specified | 5        | 0.05      | 1.0                   | Not Specified         | 29.82              |





**Figure 7. AC Line Current Monitor (Safety Isolation and Level Shift) Application**

Figure 7 shows an ac line current monitor that demonstrates both safety isolation and level shifting. Safety isolation galvanically isolates the 110 VAC line from the low-voltage, ground-based circuits. This circuit uses resistive shunt R1 to sense ac current. The high-voltage interface circuit is referenced to the ac neutral (white) wire in a two-wire (non-earth grounded) single-phase ac service.

ISOLinear input-side bias voltage is line-derived and uses a 3 V linear regulator. The low-voltage output-side circuits are biased by a ground-referenced supply. Because there is no earth ground in this system, an ac line perturbation can potentially cause high voltage to appear on the neutral (white) wire. This elevated neutral line common-mode voltage is rejected by the Si86xx isolator's high CMTI of 35 kV/ $\mu$ s minimum, 50 kV/ $\mu$ s typical. For more isolated level shifting application examples, see Silicon Labs Application Note "AN598: High-Speed Level Shifting Using Si8xxx Isolators".

Figure 8 shows a common ground loop in the transmission path of two linear circuits (a common scenario in test and measurement, audio and other applications that use cable interconnects). The ground loop in the top diagram circulates between the connector grounds while parasitic inductance ( $Z$ ) causes ringing that generates output noise. The bottom circuit of Figure 8 inserts the ISOLinear circuit between the signal source and receiver, breaking the ground loop and dramatically reducing the local ground path lengths and associated parasitic inductance.

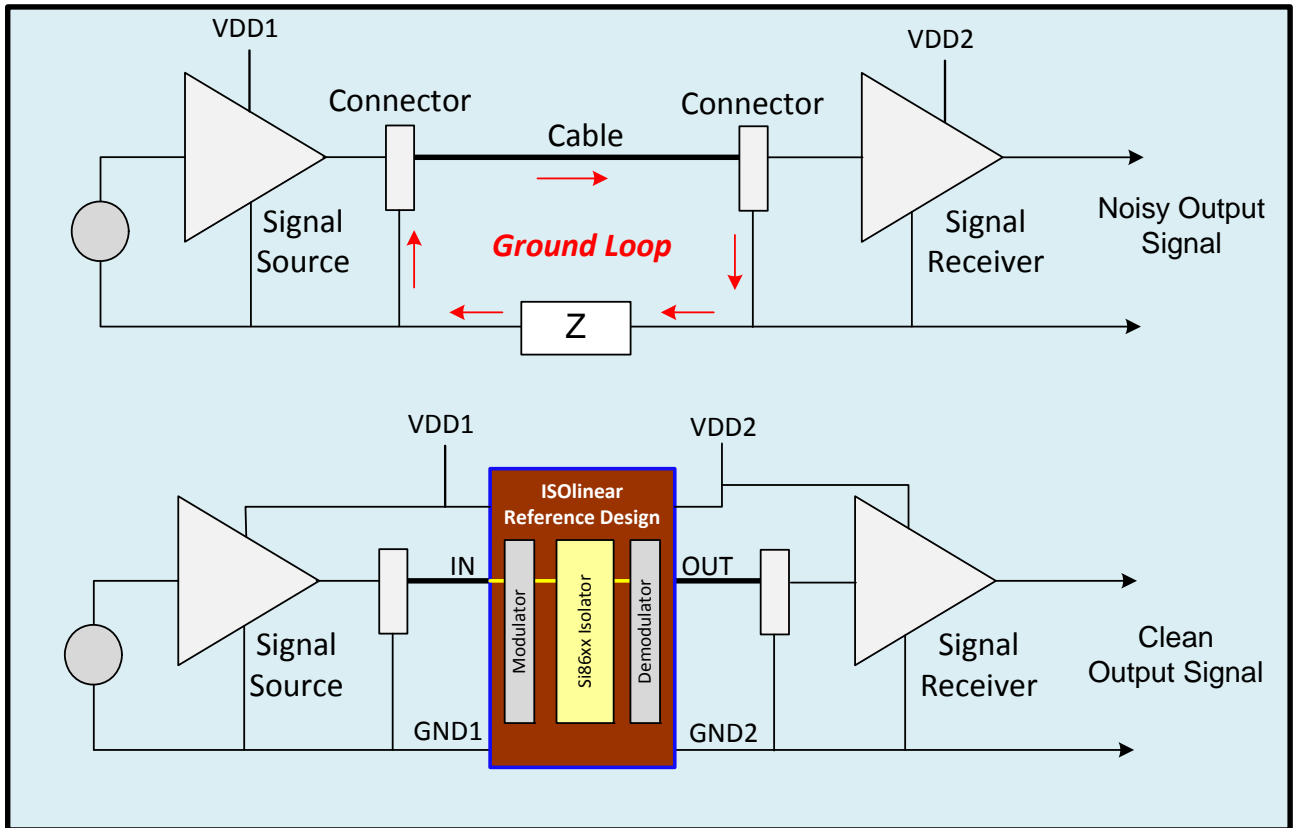


Figure 8. Ground Loop Elimination Circuit



## 4. Summary

Many analog systems require isolation to provide safety, level shifting or to mitigate ground noise. ISOamps are a common but expensive solution that lack flexibility and force the designer to compromise and/or add supplemental circuitry to a design.

Silicon Labs' ISOlinear reference design (Si86IsoLin-EVB) offers a lower-cost, more flexible linear isolation solution. This design is enabled by the Silicon Labs Si86xx industry-leading digital isolator and requires only four operational amplifiers and some passive components in addition to the isolator. The ISOlinear reference design benefits the user with a robust, competitive solution and the opportunity to create an optimum solution for the application at hand at a fraction of the price of an ISOamp.

### 4.1. Related Documents

- AN559: "Isolating Analog Signals Using the Si86xx CMOS Isolator Family", Silicon Labs, 2011
- ISOlinear Users Guide, Silicon Labs, 2011
- AN598: "High-Speed Level Shifting Using Si8xxx Isolators"

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