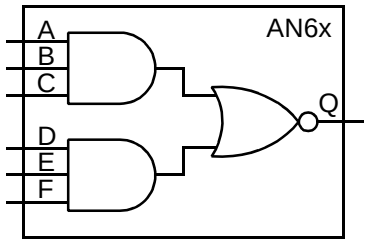
Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	5.0	TBD	8.8
AN64	6.0	TBD	10.1
AN66	12.0	TBD	19.5

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN62	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.48	0.50 0.58	0.62 0.71	0.77 0.87	0.89 0.99
AN64	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.48	0.53 0.61	0.63 0.72	0.73 0.83	0.82 0.95
AN66	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.49	0.51 0.63	0.59 0.72	0.68 0.82	0.78 0.91

Delay will vary with input conditions. See page 2-17 for interconnect estimates.