AN6345

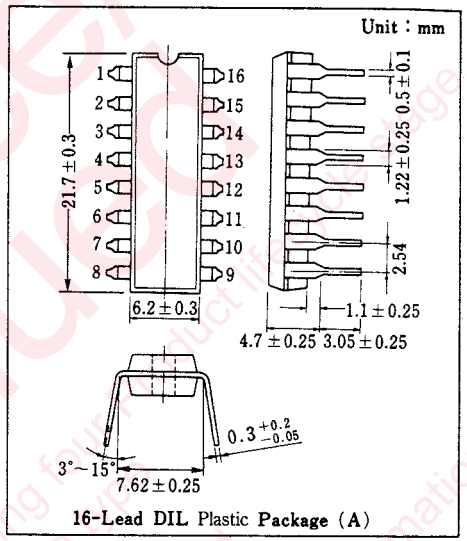
VTR FG Frequency Divider

■ Outline

The AN6345 is an integrated circuit designed for VTR FG frequency dividing.

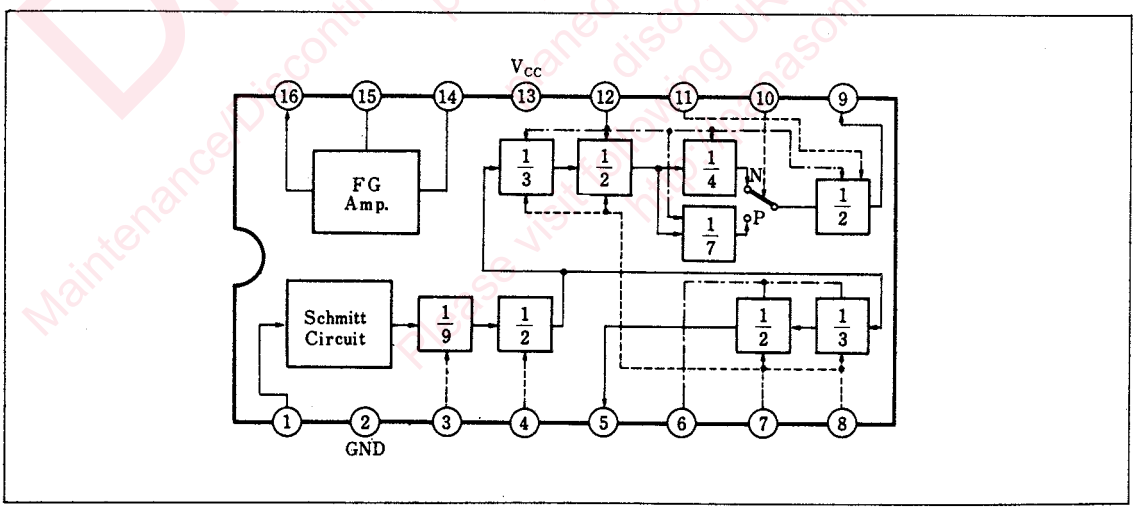
■ Features

- The functions consist of:
  - FG amplifier
  - FG frequency divider
  - Reset circuit
- Supply voltage either 9V or 12V



16-Lead DIL Plastic Package (A)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Schmit Input	9	PG Output
2	GND	10	NTSC/PAL Select
3	×9 Select	11	1/2 Select
4	×2 Select	12	Reset
5	FG Output	13	V_{CC}
6	Divide Select	14	Cap. FG Input
7	2/4/6 Select	15	Bias
8	2/4/6 Select	16	FG Amp. Output

■ Absolute Maximum Ratings (Ta=25℃)

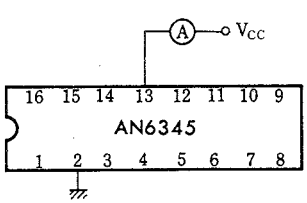
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	13	V
Power dissipation (Ta=70℃)	P_D	320	mW
Operating ambient temperature	T_{opr}	−20～+70	℃
Storage temperature	T_{stg}	−40～+150	℃

■ Electrical Characteristics (V_{CC}= 1 2 V, Ta=25℃± 2 ℃)

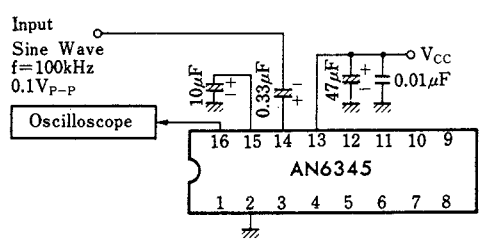
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current	I_{13}	1		10		21	mA
FG amp. gain	G_{V14-16}	2	f=100kHz, 0.1V_{P-P}	1.25		1.95	V_{P-P}
Schmitt circuit input sensitivity	S_1	3		0.2			V_{P-P}
FG Output (H) output voltage	V_{5H}	4		5.9		6.9	V
PG Output (H) output voltage	V_{9H}	5		5.9		6.9	V
FG Output (L) output voltage	V_{5L}	4				0.5	V
PG Output (L) output voltage	V_{9L}	5				0.5	V
Frequency divider select sensitivity	$S_{(Select)}$	4,5		4			V
PG output reset sensitivity	S_{12}	5				1.2	V

Note) Operating supply voltage $V_{CC(opr)}$=8.5～12.5V

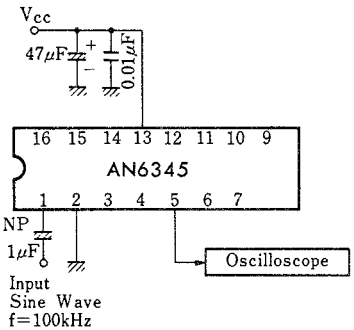
Test Circuit 1 (I_{13})



Test Circuit 2 (G_{V14-16})

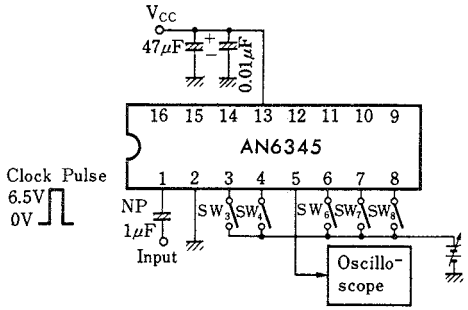


Test Circuit 3 (S_1)



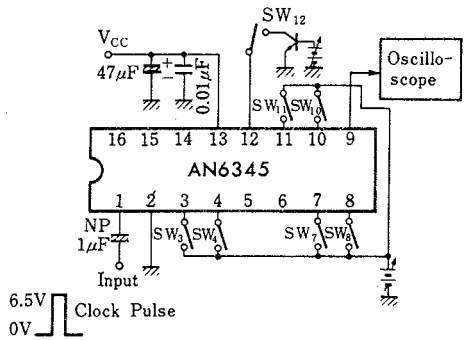
• Input signal when Pin⑤ output is normally made.

Test Circuit 4 (V_{5H}, V_{5L}, $S_{(Select)}$)



• FG Output(H),(L): Apply clock pulses to the Pin① in accordance with the Divide Select List and measure Pin⑤ output per item.

Test Circuit 5 (V_{9V}, V_{9L}, $S_{(Select)}$, S_{12})



• PG Output(H),(L): Apply clock pulses to the Pin① in accordance with the Divide Select List and measure Pin⑨ output per item.

• Frequency divider select sensitivity(test circuits 4, 5): Give a sine wave of 0.2Vp−p, f=100kHz to Pin① input instead of clock pulses, close the switch of the terminal which measures frequency divider select sensitivity, apply a voltage of 0 up to 5V to that terminal, and read the potential of that select terminal when a frequency dividing ratio for outputs(Pin⑤, ⑨) changes as shown in the Divide Select List.

• PG output reset sensitivity: Set Pin⑨ output to "L" in accordance with the Divide Select List, close S_{12} to change Pin⑫ potential to 4V−0V, and read Pin⑫ potential at which Pin⑨ output is turned to "H".

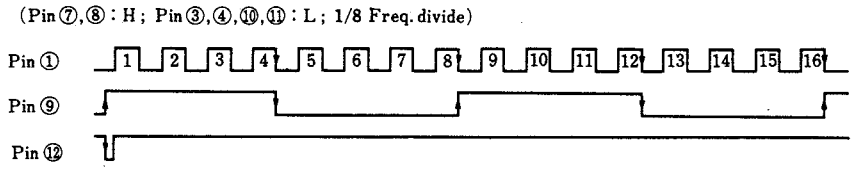
■ Divide Select List

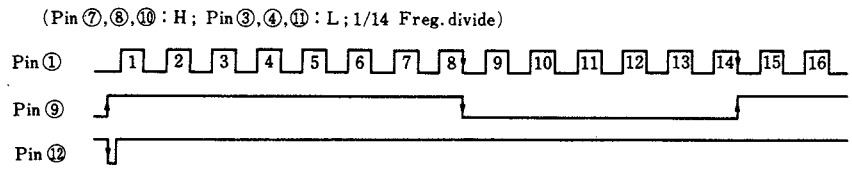
Pin ⑥	Pin ⑦	Pin ⑧	FG Output	PG Output
L	L	L	1/6	1/6
L	H	L	1/3	1/3
L	H	H	1/2	1/2
H	L	L	1/2	1/6
H	H	L	1	1/3
H	H	H	1	1/2

	H	L	FG Output	PG Output
Pin ③	1/9	1	○	○
Pin ④	1/2	1	○	○
Pin ⑩	1/7	1/4		○
Pin ⑪	1/2	1		○

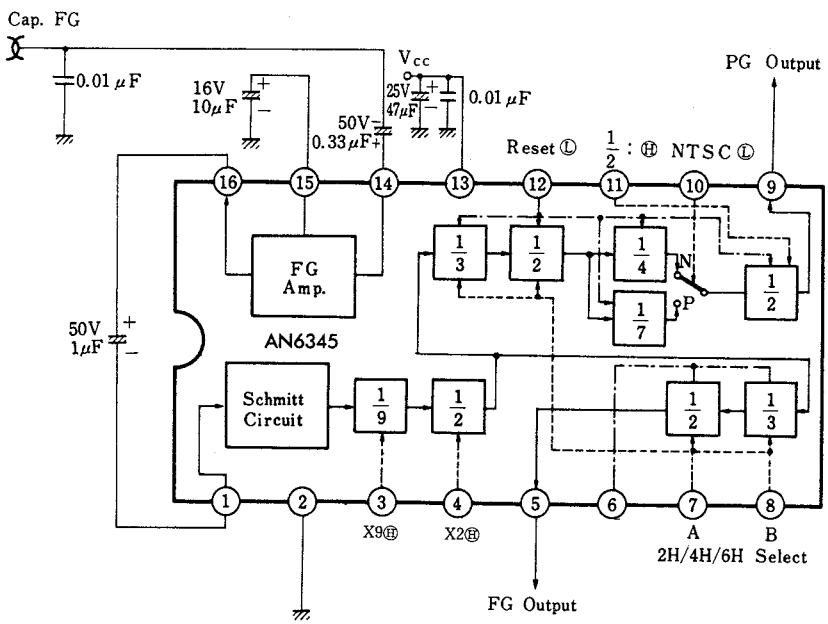
■ PG Output Reset Pin Timming Chart

(⑦⑧ : H, ③④⑩⑪ : L, 1/8 divide)





■ Application Circuit



● 2H/4H/6H Select

	2H	4H	6H
A	Ⓛ	Ⓗ	Ⓗ
B	Ⓛ	Ⓛ	Ⓗ

● Pin ⑥ Select

	2H	4H	6H
Ⓗ	1/2	1	1
Ⓛ	1/6	1/3	1/2

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