AN650

Si468x Schematics and Layout Guide

1. Introduction

This document provides:

- General Si468x design guidelines, which include schematics, layout, and BOM
- Si468x FM/FMHD/T-DMB/DAB antenna/matching network design guidelines

2. Si468x WLCSP Schematic and Layout

2.1. Schematic Design and Component Selection

This section shows the minimal schematic and layout options required for optimal performance of Si468x in the WLCSP package. Population options are provided to mitigate system noise, to use analog audio output, and to operate the Si468x with crystal.

2.1.1. Schematic Design

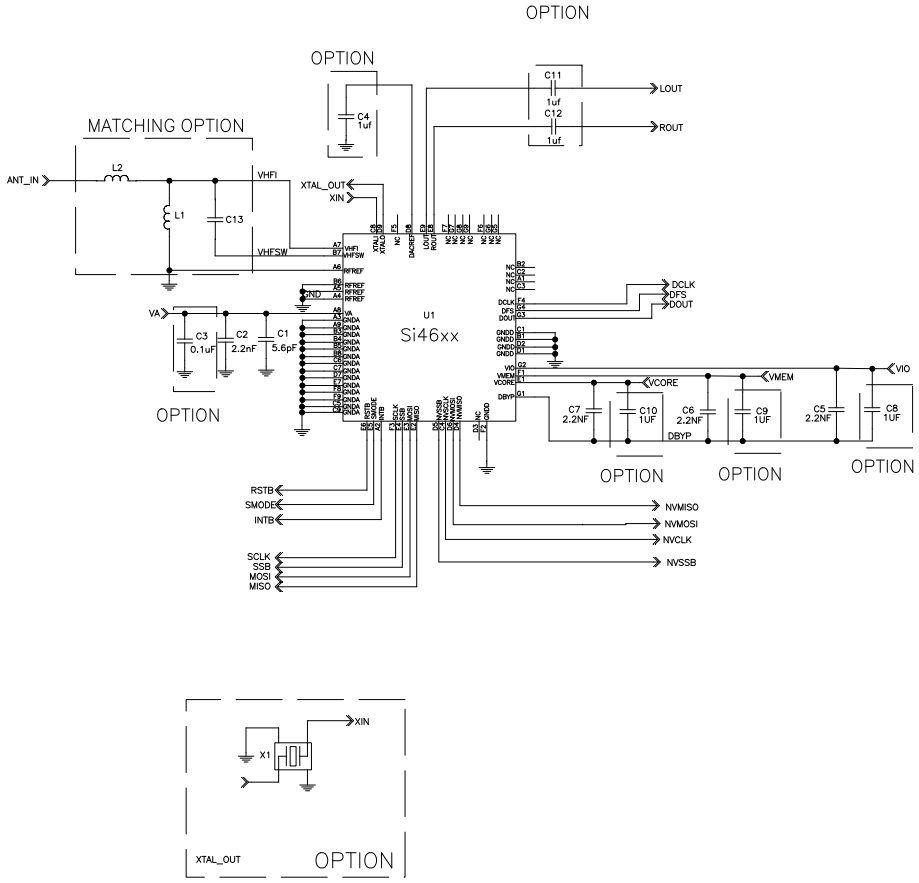


Figure 1. Si468x WLCSP Schematic Design

2.1.2. Component Selection

The L1, L2 and C13 are external components for matching purposes. This configuration is set up for achieving the best conducted sensitivity result. It is shown here for demonstrating best possible layouts. But when designing with a specific antenna, the exact matching network and component values are referred to in each individual antenna selection in “4. Antenna and Matching Network Design and Layout” .

L1 and L2 are front-end matching inductors. Inductors L1 and L2 are selected to maximize the voltage gain across the DAB/T-DMB band. L1 and L2 should be selected with a Q of 15 to 20 in the range of 100 MHz to 200 MHz. Place L1 and L2 as close as possible to the Si468x. Also, route L1 to ground plane with a short trace and a via. Drop an in-pad ground via for A6 to connect the pin to ground plane.

C13 is required to optimize voltage on the VHFI pin in the FM/FMHD band. Refer to property “0x1712” of AN649 for information on how to handle the VHFSW.

The recommendations regarding C1, C2, C3, C5, C6, C7, C8, C9 and C10 are made to reduce the size of the current loop created by the bypass cap and routing, minimize impedance and return all currents to the GND.

C1 and C2 (5.6 pF and 2.2 nF) are required bypass capacitors for VA supply pin A8. C3 (0.1uF) is an optional bypass capacitor. Place C1, C2 and C3 as close as possible to VA. C1 and C2 are chosen to mitigate noise in VCO frequency range and VHF range respectively. Place a via connecting C1, C2, C3 and VA pin to the power rail such that the caps are closer to the Si468x VA pin than the via. Route C1, C2 and C3 to the ground plane with a short trace and a via directly.

C5 (2.2nF) is a required bypass capacitor for VIO supply pin G2. C8 (1uF) is an optional bypass capacitor. C5 and C8 are chosen to mitigate noise in the VHF band. Place C5 and C8 as close as possible to VIO pin G2 and DBYP pin G1. Place a via connecting C5, C8 and VIO supply G2 to the power rail such that the caps are closer to the Si468x VIO pin than the via. Route C5 and C8 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C6 (2.2nF) is a required bypass capacitor for VMEM supply pin F1. C9 (1uF) is an optional bypass capacitor. C6 and C9 are chosen to mitigate noise in VHF band. Place C6 and C9 as close as possible to VMEM pin F1 and DBYP pin G1. Place a via connecting C6, C9 and VMEM supply pin F1 to the power rail such that the caps are closer to the Si468x VMEM pin than the via. Route C6 and C9 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C7 (2.2nF) is a required bypass capacitor for VCORE supply pin E1. C10 (1uF) is an optional bypass capacitor. C7 and C10 are chosen to mitigate noise in the VHF band. Place C7 and C10 as close as possible to VCORE pin E1 and DBYP pin G1. Place a via connecting C7, C10 and VCORE pin E1 to the power rail such that the caps are closer to the Si468x VCORE pin than the via. Route C7 and C10 only to DBYP directly with a short (6-mil width) low inductance trace.

C4 (1uF) is an optional bypass capacitor for DACREF pin D8 if customer uses analog audio output. Place C4 as close as possible to DACREF and the GND pin. Customers do not need to populate this capacitor if they are using digital audio output only.

C11 and C12 (1 uF and 1 uF) are optional ac coupling capacitors for analog audio outputs. The value should be selected to work well with the customer’s choice of audio amp.

X1 is an optional crystal required only when using the internal oscillator feature. Place the crystal X1 as close to XTALI (pin C8) and XTALO (pin D9) as possible to minimize current loops.

2.1.3. Layout Guide

The following placement/layout guides are suggested for 6-layer PCB:

- PCB layer assignment:
  - Layer 1 top side placement and routing for RF and analog traces
  - Layer 2 routing for analog traces
  - Layer 3 GND plane
  - Layer 4 routing for digital traces
  - Layer 5 routing for digital traces
  - Layer 6 bottom side placement and routing for digital traces
- Minimum 3-mil trace
- Minimum 3-mil trace spacing
- 6-mil drill 2-mil plating for in-pad vias (through or buried for 2, 4, 5, 6 layers)
- 6-mil drill 9-mil plating for normal vias
- Minimum 10-mil component spacing
- Power routed by trace
- 0201 component size or larger

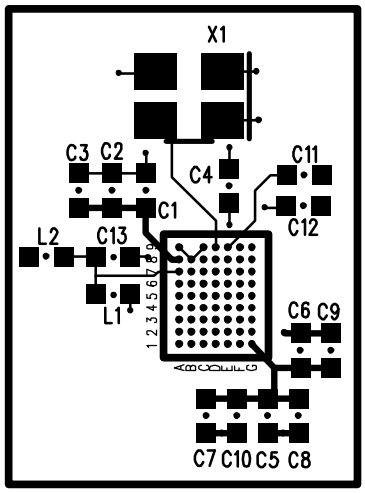


Figure 2. Si468x WLCSP Layout Design

Figure 2 shows critical layout with top side placement, key top side routing, and crystal support. All bypass components are placed around the silicon as close as possible. A few things to note:

- L1 and C13 should be placed as close as possible to the chip and as far from noise sources such as clocks and digital circuits as possible.
- For the VA bypass caps, make sure the cap with the lowest (5.6 pF) value is placed closest to the chip.
- There are 11 GNDA pins which separate the analog and digital portions of the chip. The pins need to be stitched to the ground plane with an in-pad via.
- To prevent disturbance on VCO operation, A9, C9, and B8 pins need to be stitched to the GND plane with in-pad via and connected with 3-mil trace as shown in the layout figure.
- To bring out the digital traces, the following example strategy is described for 6-layer PCB:
  - For pins on outer row (or column) of the grid, use in-pad blind vias to drop down to layer 4 and fanout the traces.
  - For pins on 2nd inner row (or column) of the grid, use in-pad blind vias to drop down to layer 5 and fanout the traces.
  - For pins on 3rd or 4th inner row (or column) of the grid, use in-pad blind vias to drop down to the bottom layer and fanout the traces.

2.1.3.1. BOM

Table 1. Required BOM

Ref Designator	Description	Note
C1	VA supply bypass capacitor, 5.6 pF, 10%, Z5U/X7R	
C2	VA supply bypass capacitor, 2.2 nF, 10%, Z5U/X7R	
C5, C6, C7	VIO supply bypass capacitor, 2.2 nF, 10%, Z5U/X7R	

Table 2. Optional BOM

Ref Designator	Description	Note
L1	IND, 0402, SM, 100nH	This value is required for achieving the best conducted sensitivity result.
L2	IND, 0402, SM, 68nH	This value is required for achieving the best conducted sensitivity result.
C3	VA supply bypass capacitor, 0.1μF, 10%, Z5U/X7R	
C4	DACREF bypass capacitor, 1μF, 10% Z5U/X7R	
C8, C9, C10	Supply bypass capacitor, 1μF, 10%, Z5U/X7R	
C11, C12	Audio AC-coupling capacitor, 1μF, 10% Z5U/X7R	
C13	AC coupling cap, SM, 0402, 18pF	For antenna matching. See value details in section “Antenna and matching network design and layout.”
X1	Abracon, ABM8-19.200MHz-10-1-U-T, 19.2 MHz	For design temperature ranges from –10 deg C to 60 deg C. Contact Silicon Laboratories for recommendations with more flexibility.

3. Si468x QFN Schematic and Layout

3.1. Schematic design and component selection

This section shows the minimal schematic and layout options reserved for optimal performance of the Si468x in the QFN package. Population options are provided to mitigate system noise, to use analog audio output, and to operate the Si468x with crystal.

3.1.1. Schematic Design

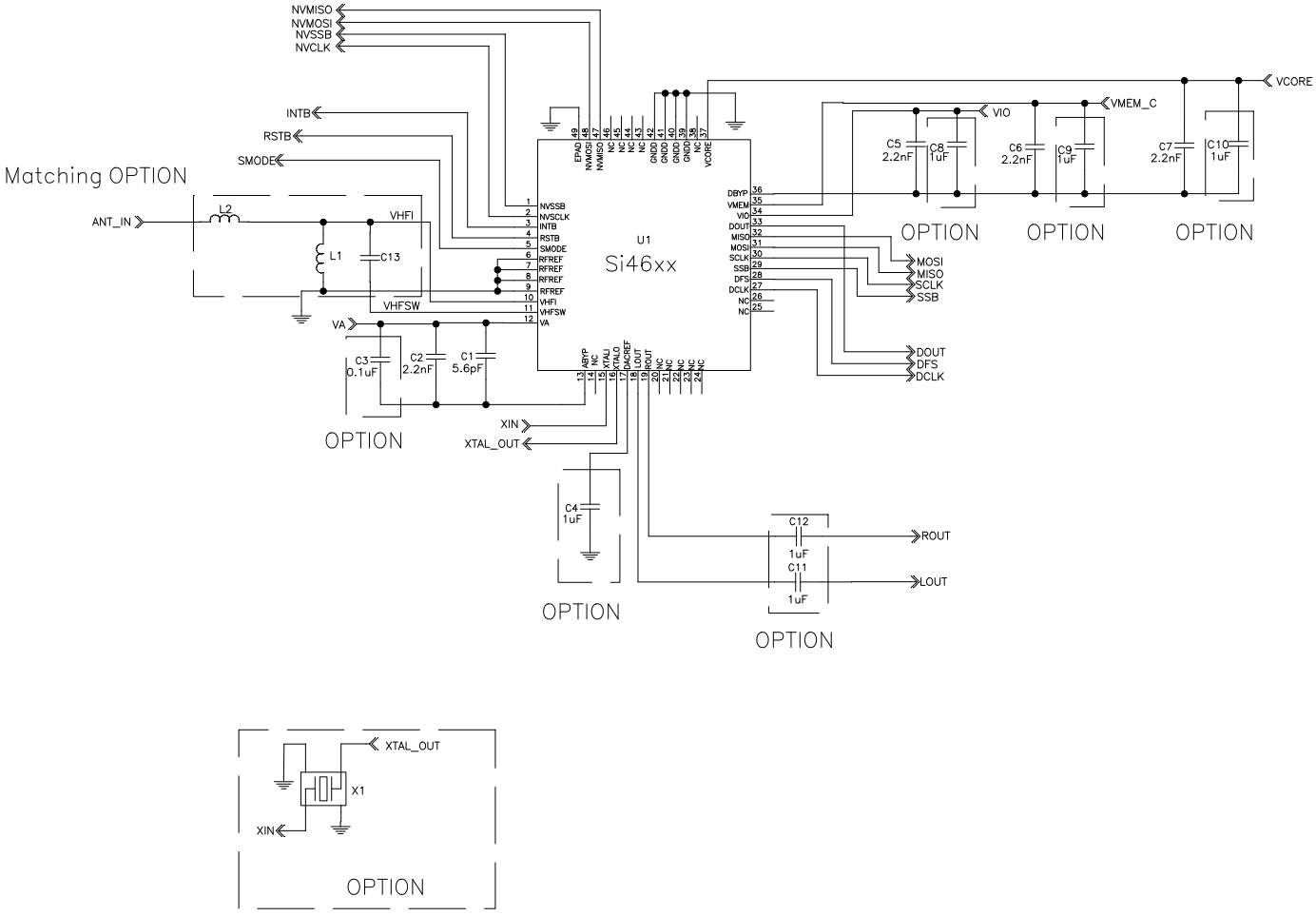


Figure 3. Si468x QFN Schematic Design

3.1.2. Component Selection

The L1, L2 and C13 are external components for matching purposes. This configuration is set up for achieving the best conducted sensitivity result. It is shown here for demonstrating best possible layouts. But when designing with a specific antenna, the exact matching network and component values are referred to in each individual antenna selection in “4. Antenna and Matching Network Design and Layout” .

L1 and L2 are front-end matching inductors. Inductors L1 and L2 are selected to maximize the voltage gain across the DAB/T-DMB band. L1 and L2 should be selected with a Q of 15 to 20 in the range of 100 to 200 MHz. Place L1 and L2 as close as possible to the Si468x. Also, route L1 to ground plane with a short trace and a via. Connect pin9 RFREF to and only to ground pad of L1 in layout.

C13 is required to optimize voltage on the VHFI pin in the FM/FMHD band. Refer to property “0x1712” of AN649 for information on how to enable the VHFSW.

The recommendations regarding C1, C2, C3, C5, C6, C7, C8, C9 and C10 are made to reduce the size of the current loop created by the bypass cap and routing, minimize impedance and return all currents to the ground.

C1 and C2 (5.6 pF and 2.2 nF) are **required** bypass capacitors for VA supply pin 12. C3 (0.1 uF) is an **optional** bypass capacitor. Place C1, C2 and C3 as close as possible to VA. C1 and C2 are chosen to mitigate noise in VCO frequency range and VHF range respectively. Place a via connecting C1, C2, C3 and VA pin to the power rail such that the caps are closer to the Si468x VA pin than the via. Route C1, C2 and C3 only to the ABYP pin directly with a short (6-mil width) low inductance trace.

C5 (2.2 nF) is a **required** bypass capacitor for VIO supply pin 34. C8 (1 uF) is an **optional** bypass capacitor. C5 and C8 are chosen to mitigate noise in VHF band. Place C5 and C8 as close as possible to VIO pin 34 and DBYP pin 36. Place a via connecting C5, C8 and VIO supply to the power rail such that the caps are closer to the Si468x VIO pin than the via. Route C5 and C8 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C6 (2.2nF) is a **required** bypass capacitor for VMEM supply pin 35. C9 (1 uF) is an **optional** bypass capacitor. C6 and C9 are chosen to mitigate noise in VHF band. Place C6 and C9 as close as possible to VMEM pin 35 and DBYP pin 36. Place a via connecting C6, C9 and VMEM supply pin to the power rail such that the caps are closer to the Si468x VMEM pin than the via. Route C6 and C9 only to DBYP pin directly with a short (6-mil width) low inductance trace.

C7 (2.2nF) is a **required** bypass capacitor for VCORE supply pin 37. C10 (1 uF) is an **optional** bypass capacitor. C7 and C10 are chosen to mitigate noise in VHF band. Place C7 and C10 as close as possible to VCORE pin 37 and DBYP pin 36. Place a via connecting C7, C10 and VCORE pin 37 to the power rail such that the caps are closer to the Si468x VCORE pin than the via. Route C7 and C10 only to DBYP directly with a short (6-mil width) low inductance trace.

C4 (1uF) is an **optional** bypass capacitor for DACREF pin 17 if customer uses analog audio output. Place C4 as close as possible to DACREF pin. Customers do not need to populate this capacitor if they are using digital audio output only.

C11 and C12 (1uF and 1uF) are **optional** ac coupling capacitors for analog audio outputs. The value should be selected to work well with the customer’s choice of audio amp.

X1 is an **optional** crystal required only when using the internal oscillator feature. Place the crystal X1 as close to XTALI (pin 15) and XTALO (pin 16) as possible to minimize current loops.

3.1.3. Layout Guide

The following placement/layout guidelines are suggested for 4-layer PCB:

- PCB layer assignment:
  - Layer 1 top side placement and routing for RF and analog traces
  - Layer 2 ground plane
  - Layer 3 routing for digital traces and ground plane
  - Layer 4 bottom side placement and routing for digital traces
- Minimum 6-mil trace
- Minimum 6-mil trace spacing
- 6-mil drill 9-mil plating for normal vias
- Minimum 10-mil component spacing
- Power routed by trace
- 0402 component size or larger

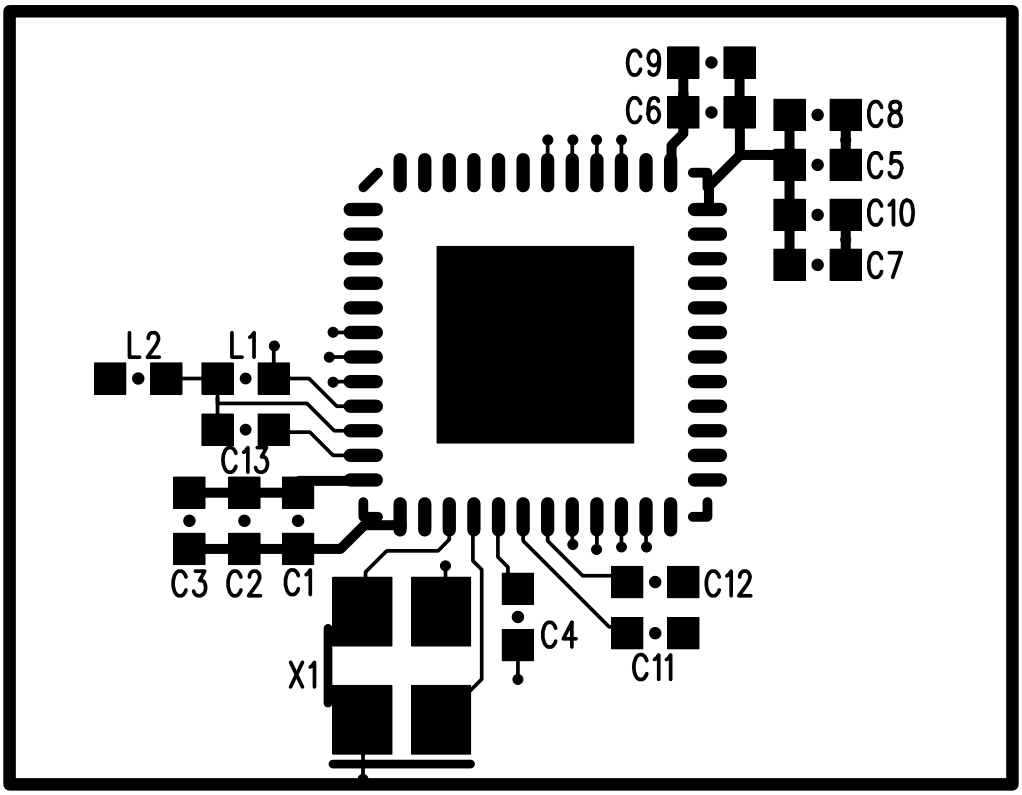


Figure 4. Si468x QFN Layout Design

Figure 4 shows critical layout with top side placement, key top side routing, and crystal support. All bypass components are placed around the silicon as close as possible. A few things to note:

- L1 and C13 should be placed as close as possible to the chip and as far from noise sources such as clocks and digital circuits as possible.
- For the VA bypass caps, make sure the cap with the lowest (5.6 pF) value is placed the closest to the chip.
- Do not tie any GND pins back to the GND paddle. Stitch the GND paddle to GND using vias.

3.1.3.1. BOM

Table 3. Required BOM

Ref Designator	Description	Note
C1	VA supply bypass capacitor, 5.6 pF, 10%, Z5U/X7R	
C2	VA supply bypass capacitor, 2.2 nF, 10%, Z5U/X7R	
C5, C6, C7	VIO supply bypass capacitor, 2.2 nF, 10%, Z5U/X7R	

Table 4. Optional BOM

Ref Designator	Description	Note
L1	IND, 0402, SM, 100 nH	This value is required for achieving the best conducted sensitivity result.
L2	IND, 0402, SM, 68 nH	This value is required for achieving the best conducted sensitivity result.
C3	VA Supply bypass capacitor, 0.1 μF, 10%, Z5U/X7R	
C4	DACREF bypass capacitor, 1 μF, 10% Z5U/X7R	
C8, C9, C10	Supply bypass capacitor, 1 μF, 10%, Z5U/X7R	
C11, C12	Audio AC-coupling capacitor, 1 μF, 10% Z5U/X7R	
C13	AC coupling cap, SM, 0402, 18 pF	This value is required for achieving the best conducted sensitivity result.
X1	Abracon, ABM8-19.200MHz-10-1-U-T, 19.2 MHz	For design temperature ranges from –10 to 60 °C. Contact Silicon Laboratories for recommendations with more flexibility.

4. Antenna and Matching Network Design and Layout

4.1. HP Antenna (Si468x)

The Si468x Digital Radio Receiver component supports a headphone antenna interface through the VHFI pin. A headphone antenna with a length of 1.1 m suits FM/FMHD/T-DMB/DAB applications well.

4.1.1. Headphone Antenna Design

A typical headphone cable will contain three or more conductors. The left and right audio channels are driven by a headphone amplifier onto left and right audio conductors and the common audio conductor is used for the audio return path and RF antenna. Additional conductors may be used for microphone audio, switching, or other functions, and in some applications the RF antenna will be a separate conductor within the cable. A representation of a typical application is shown in Figure 5.

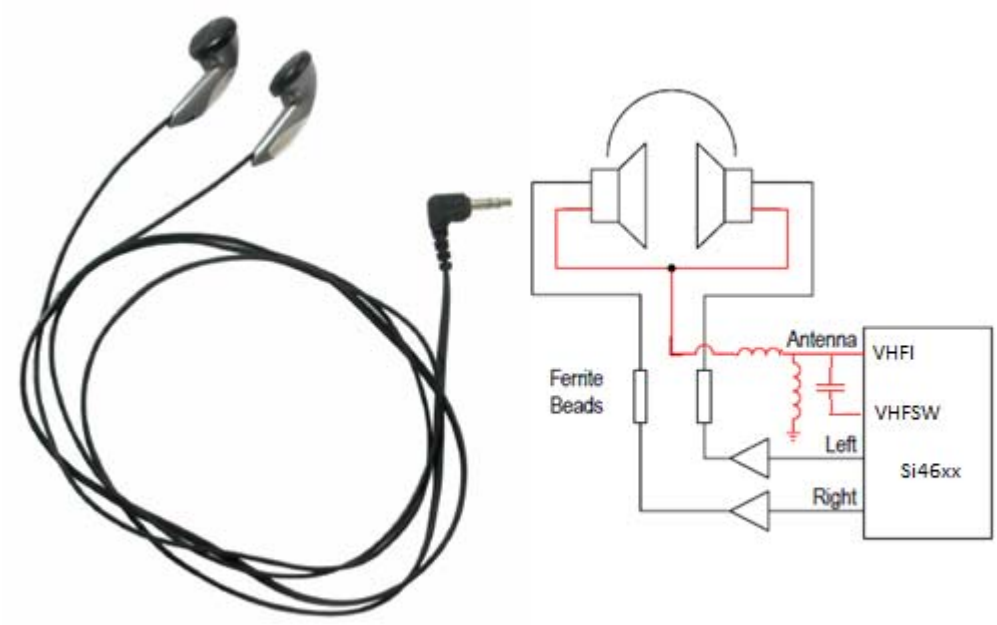


Figure 5. A Typical HP Antenna Application

4.1.2. Headphone Antenna Schematic

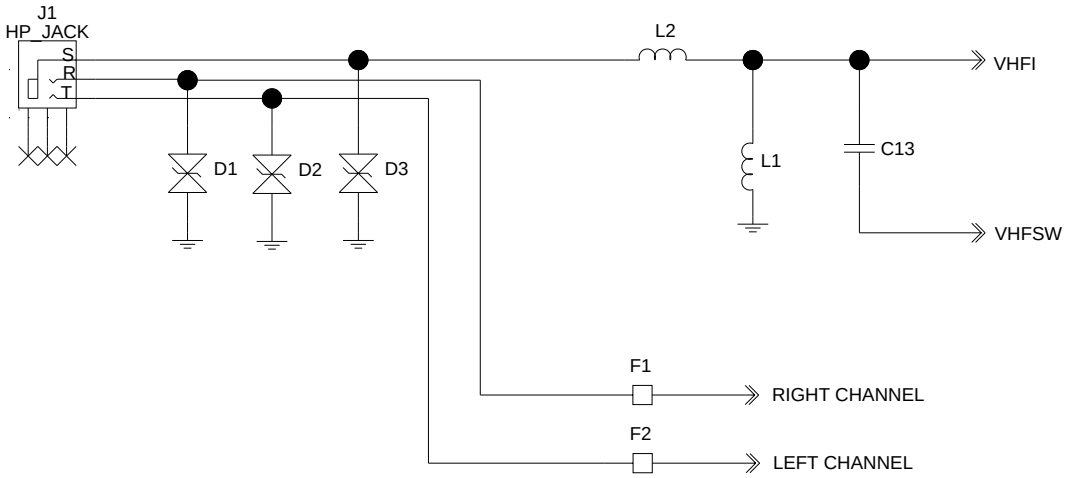


Figure 6. Headphone Antenna Design

The headphone antenna implementation requires components L1, L2, C13, F1, F2, and F3 for a minimal implementation. In Figure 6, a headphone and circuit with headphone audio common grounded is used. The ESD protection diodes and headphone amplifier components are system components that will be required for proper implementation of any tuner. Inductors 1 and 2 are selected to maximize the voltage gain across the DAB/T-DMB band. C13 is switched in with VFHSW to ensure the FM/FMHD band is properly resonated. The user should refer to property “0x1712” of AN649 to understand how to enable and disable the switch.

Ferrite beads F1 and F2 provide a low-impedance audio path and high-impedance RF path between the headphone amplifier and the headphone. Ferrite beads should be placed on each antenna conductor connected to nodes other than the VHFI such as left and right audio, microphone audio, switching, etc. In the example shown in the figure above, these nodes are the left and right audio conductors. Ferrite beads should be 2.5 kΩ or greater at 100 MHz, such as the Murata BLM18BD252SN1. High impedance is desirable to reduce antenna coupling to the other conductors.

L1 and L2 are used as audio ground. Diodes should be chosen with no more than 1 pF parasitic capacitance, and diode capacitance should be minimized. If D1 and D2 must be chosen with a capacitance greater than 1 pF, they should be placed between the ferrite beads and the headphone amplifier to minimize PCB parasitic capacitance. This placement will, however, reduce the effectiveness of the ESD protection devices. Diode D3 may not be relocated and must therefore have a capacitance less than 1 pF. Note that each diode package contains two devices to protect against positive and negative polarity ESD events.

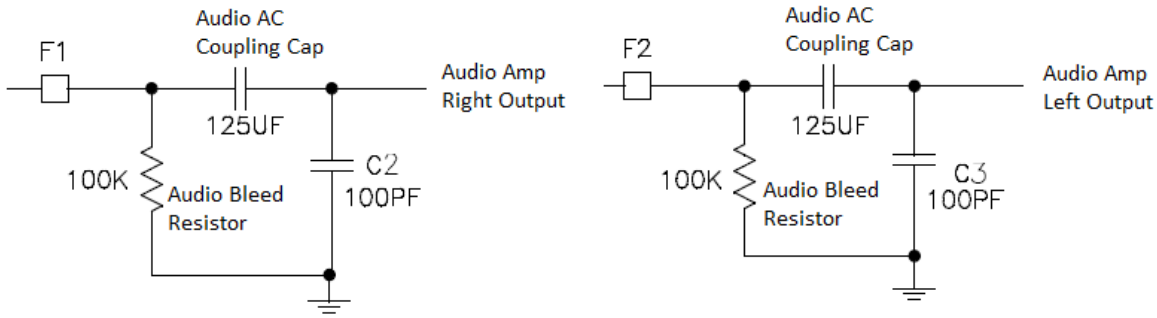


Figure 7. Optional RF Shunt Capacitors to Reduce Noise Coupling to Antenna

As shown in Figure 7, **optional** RF shunt capacitors C2 and C3 may be placed on the left and right audio traces at the headphone amplifier output to reduce the level of digital noise passed to the antenna. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

Table 5. Headphone Antenna BOM

Ref Designator	Description	Note
L1	IND, SM, 100 nH, MURATA	
L2	IND, SM, 36 nH, MURATA	
C13	AC coupling cap, SM, 18 pF, Murata	
F1, F2, F3	FERRITE BEAD, SM, 0603, 2.5 kΩ, Murata, BLM18BD252SNID	
D1, D2, D3	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213	

Table 6. Headphone Antenna Optional BOM

Ref Designator	Description	Note
C2	SM, 0402, X7R, 100 pF	Optional RF shunt capacitor
C3	SM, 0402, X7R, 100 pF	Optional RF shunt capacitor

4.1.3. Headphone Antenna Layout

To minimize inductive and capactive coupling, inductors C13, L1 and L2 should be placed together close to the Si468x and as far from noise sources such as clocks and digital circuits as possible.

To minimize shunt capacitance on antenna trace, place ferrite beads F1 and F2 as close as possible to the headphone connector. To maximize ESD protection diode effectiveness, place diodes D1, D2, and D3 as close as possible to the headphone connector. If capacitance larger than 1 pF is required for D1 and D2, both components should be placed between F1, F2, and F3 and the headphone amplifier to minimize antenna shunt capacitance.

Place the chip as close as possible to the headphone connector to minimize antenna trace capacitance. Keep the trace length short and narrow and as far above the reference plane as possible, restrict the trace to a microstrip topology (trace routes on the top or bottom PCB layers only), minimize trace vias, and relieve ground fill on the trace layer. Note that minimizing capacitance has the effect of maximizing characteristic impedance. It is not necessary to design for 50 Ω transmission lines.

4.2. Cable antenna (Si468x)

The charger cable of a consumer product can be used as an FM/FMHD/T-DMB/DAB antenna. This section describes how to interface the Si468x VHFI input to a cable antenna.

4.2.1. Cable Antenna Design

A typical cable antenna contains multiple inner wires/conductors, which are covered with a protective ground shield. The coupling between the wires and the shield can cause the antenna to have large capacitance in the several hundred pF range. In order to boost the received FM/FMHD/T-DMB/DAB voltage, it is necessary to minimize this capacitance. This reduction can be achieved by placing ferrite beads in series with each of the antenna's conductors.

4.2.2. Cable Antenna Schematic

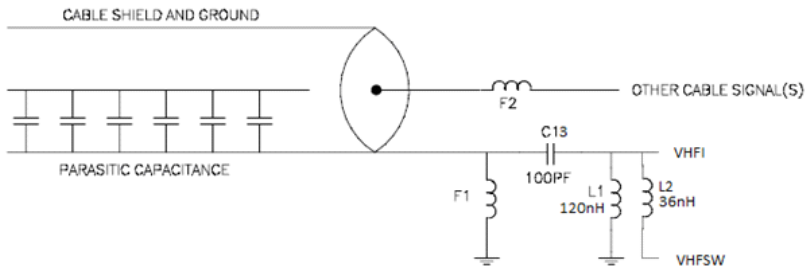


Figure 8. A Typical Cable Antenna Application

To resonate the cable antenna within the FM band, the antenna's capacitance needs to be reduced. As described in Section 4.2.1, this reduction can be achieved by placing the ferrite beads in series with each of the antenna's conductors. The capacitance should be further controlled by limiting the trace length from the cable ground shield and the RF input pin (VHFI input) on the Si468x digital radio chip. Each of the components in the schematic above is explained in detail below:

L1 (120 nH) is the tuning inductor. This is the typical value used to resonate the cable antenna in the center of the DAB Band.

L2 (36 nH) is the tuning inductor. This is the typical value used to parallel with L1 to resonate the cable antenna in the center of the DAB Band.

C13 (100 pF) is a dc blocking cap placed between the VHFI pin and the cable antenna ground. The capacitor is used to isolate the cable return currents from the L1 (120 nH) is the tuning inductor. This is the typical value used to resonate the cable antenna in the center of the FM band.

F1(1.5 kΩ at 100 MHz) is a shunt ferrite to ground at the cable antenna side. A substantial amount of ground return current may flow through the cable antenna shield/ground because there are multiple conductors inside the cable along with power supply conductors. The ferrite will divert the ground return current of the cable antenna to go

through the shunt ferrite rather than going through the tuning inductor and/or Si468x chip.

F2 (1.5 kΩ at 100 MHz) is a series ferrite placed on the signal conductor in the cable antenna. Note that series ferrites should be placed on each signal conductor in the cable. The ferrite is used to isolate the signal conductors from the shield/ground. The choice of the ferrite is dependent upon the type of signal on each individual conductor. If the conductor is used to carry power, then a ferrite with a large dc current carrying capability should be used. Likewise, if the conductor is used to carry high frequency analog signals, make sure that the ferrite does not filter the high frequency.

Table 7. Cable Antenna BOM

Ref Designator	Description	Note
L1	IND, SM, 120 nH, MURATA	
L2	IND, SM, 36 nH, MURATA	
C13	AC coupling cap, SM, 0402, X7R, 100 pF	
F1	Shunt Ferrite bead, SM, 0603, 470Ω, 1 A, Murata, BLM18PG471SN1J	Rated dc current> max expected ground return current.
F2	Series Ferrite bead, various types. Recommended ferrite for power lines: FERRITEBEAD, SM, 0603, 470Ω, 1 A, Murata, BLM18PG471SN1J Recommended ferrite for signals: FERRITEBEAD, SM, 0603, 2.5kΩ, 50mA Murata, BLM18BD252DN1D	For power signals, make sure the rated dc current> max expected ground return current. For all other signals, make sure ferrite does not block/filter the high frequency component of the signals.

4.2.3. Cable Antenna Layout

Place the chip as close to the cable antenna as possible. This will minimize the trace length going to the cable antenna which will minimize the parasitic capacitance. Place the shunt ferrite for the ground return current as close to the cable as possible. Putting the shunt ferrite for the ground return current close to the cable ensures that the ground return current has minimal loop which will reduce noise coupling. The series ferrites should be put as close as possible to the cable. This will minimize the parasitic capacitance seen by the VHFI pin.

APPENDIX A—PROCEDURE TO OPTIMIZE CONDUCTED SENSITIVITY THROUGH VARACTOR TUNING

The recommended front-end circuit value is proposed as below:

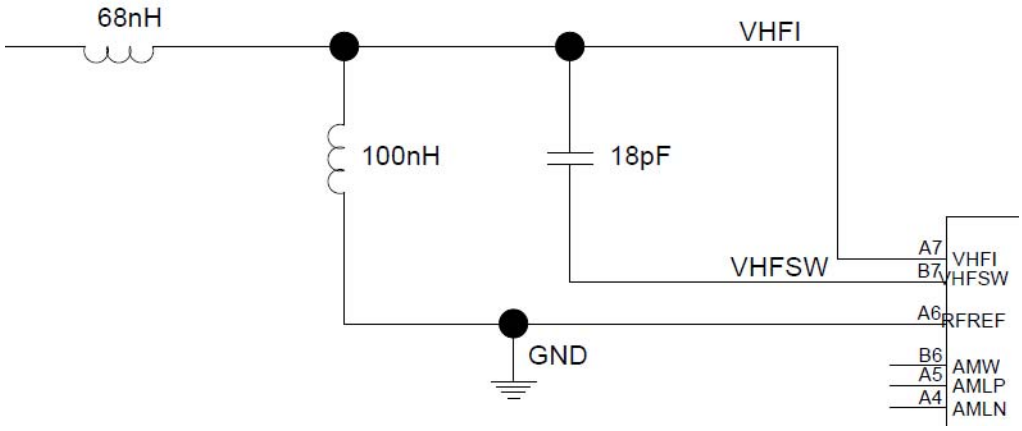


Figure 9. Recommended Front-End Network

There are 3 properties related with varactor-tuning procedure in each image:

Table 8. Varactor Tuning Properties

ID	FMHD	DMB	Note*
0x1710	FM_TUNE_FE_VARM	DAB_TUNE_FE_VARM	Slope of Varactor vs Frequency Curve
0x1711	FM_TUNE_FE_VARB	DAB_TUNE_FE_VARB	Intercept of Varactor vs Frequency Curve
0x1712	FM_TUNE_FE_CFG	DAB_TUNE_FE_CFG	Configure VHFSW switch from pin to ground
***Note:** See AN649 for detailed descriptions of these properties.			

The following procedure is intended to show how to achieve the best conducted sensitivity result for Si468x in both FM/FMHD and DMB/DAB bands by tuning the on-chip varactor. The end goal is for the customer to identify the desired values of the above 3 properties in each functional FW image. After the part is booted, the 3 properties are set to 0 by default. For each PCB design, the customer needs to set identified values so that the customer can use the automatic tuning function to achieve the target of conducted sensitivity specification.

In the tuning command of each image (DAB_TUNE_FREQ & FM_TUNE_FREQ), there is an ANTCAP parameter. Once the ANTCAP is issued with the tuning command as any value other than 0, the automatic tuning function (determined by VARM/VARB settings) is bypassed and the on-chip varactor is set as the ANTCAP value as specified by users. This feature is utilized in the procedure description below.

FM/FMHD

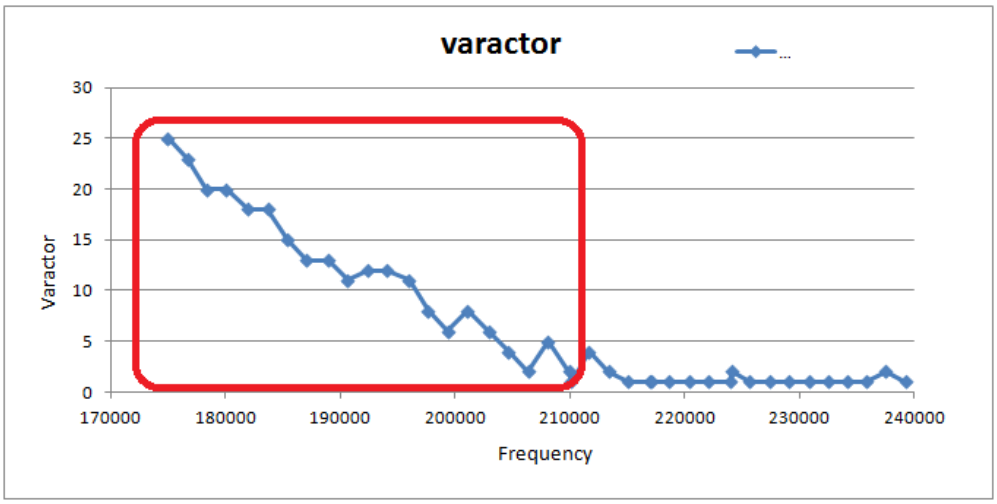
- Set FM_TUNE_FE_CFG property as 1, which closes the VHFSW.
- How to identify the varactor value for each individual frequency X:
  1. Connect the signal-generator to DUT with an SMA barrel.
  2. Set the signal-generator to frequency X with 60 dBµV reading or reaching the max tunable varactor range of 128, whichever events come first.
  3. Tune Si468x to frequency X with ANTCAP set to 1.

4. Call Test_Get_RSSI command 5 times and get the average of the 5 RSSI measurements.
5. Increment the ANTCAP by 1 and re-issue the tune command to Si468x.
6. Repeat Step 4 and Step 5 until reach the targeted 60 dBuV reading or reach the max tunable varactor range of 128, whichever events come first.
7. Log this value.

- Conduct the test above for frequencies: 88 MHz, 98 MHz, and 108 MHz (and 76 MHz if necessary).
- If describing the varactor's relationship with frequency by
  varactor_value = m/1000 x frequency (in MHz) +b
  1. Use linear-fit algorithm to calculate m and b.
  2. User may want to run more points to get a more accurage equation.
- When tuning, issue the "fm_tune_freq $arg1$freq0" to enable automatic tuning method.

DAB/DMB

- Set DAB_TUNE_FE_CFG property as 0, which opens the VHFSW.
- How to optimize varactor value for each individual frequency X:
  1. Connect the signal-generator to DUT with an SMA barrel.
  2. Set the signal-generator to frequency X with 40 dBuV rf level and DAB modulation.
  3. Tune Si468x to frequency X with ANTCAP set to 1.
  4. Call Test_Get_RSSI command 5 times and get the average of the 5 RSSi measurements.
  5. Increment the ANTCAP by 1 and re-issue the tune command to Si468x.
  6. Repeat Step 4 and Step 5 until reaching the max tunable varactor range of 128.
  7. Identify the varactor value with the max RSSI reading.
- Repeat the test for frequencies across the DAB band.
- If describing the varactor's relationship with frequency by varactor_value=m/1000*frequency (in MHz) +b, m represents the slope (DAB_TUNE_FE_VARM), b represents the intercept (DAB_TUNE_FE_VARB). Given the data collected, identify the low frequency range where the optimal varactor is not lower than 4. This is illustrated in the graph* below.



***Note:** This graph is taken with Silicon Laboratories' Si468x WLCSP daughtercard, version 2.0

Figure 10. Varactor vs. Frequency Chart

- Feed this data section in red circle to linear-fit algorithm to identify the slope m and intercept b. Program m and b values into the properties: 0x1710, 0x1711 after Si468x is booted.
- When tuning, issue the "dab_tune_freq0$freq0" to enable automatic tuning method.

APPENDIX B—CLASSIC FRONT-END

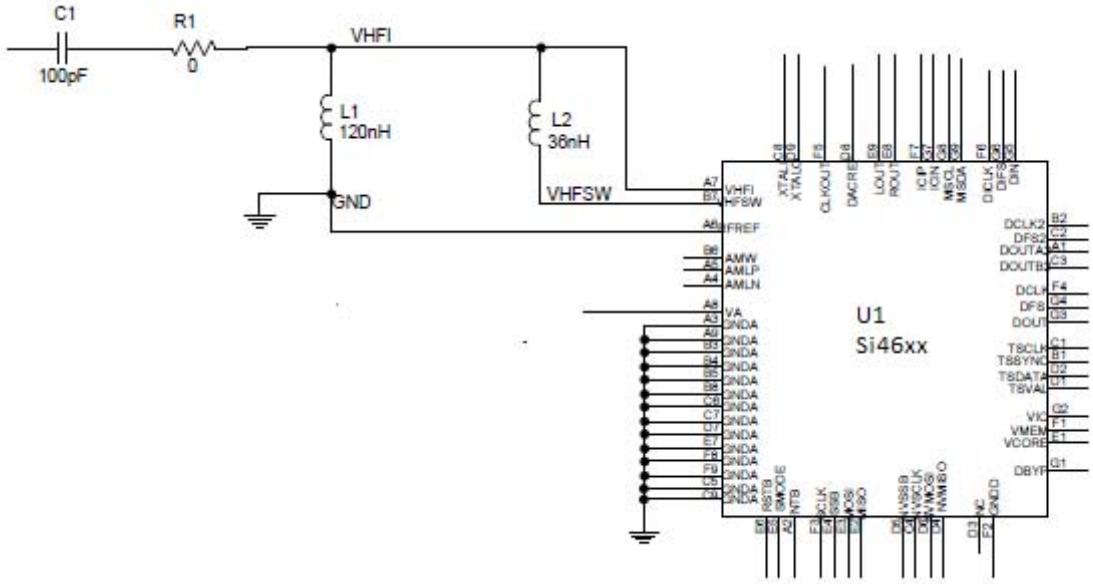


Figure 11. Matching Network

Silicon Labs recommend using the classic front-end matching network shown in Figure 11 for the DAB-P2 and FMHD-P2 release. The classic front-end network requires no PCB layout change and can be implemented by replacing components and value as follows:

Original Matching Network (Refer to Figure 11)	Classic Front-end Network
L1(68 nH)	C1 (100 pF)
C13 (18 pF)	L2 (36 nH)
L1(100 nH)	L1(120 nH)

In the meantime, for VHFSW configuration (property DAB_TUNE_FE_CFG), refer to the following:

	Original Matching Network (Refer Figure 11)	Classic Front-end Network
FMHD	Switch Closed	Switch Open
DAB	Switch Open	Switch Closed

The change addressed in this appendix is applicable for QFN and WLCSP packages.

APPENDIX C—APPLICATION CIRCUIT FOR EMI MITIGATION

The application circuit recommended in this appendix is for reducing the on-chip VCO radiated emissions and achieving the optimum matching.

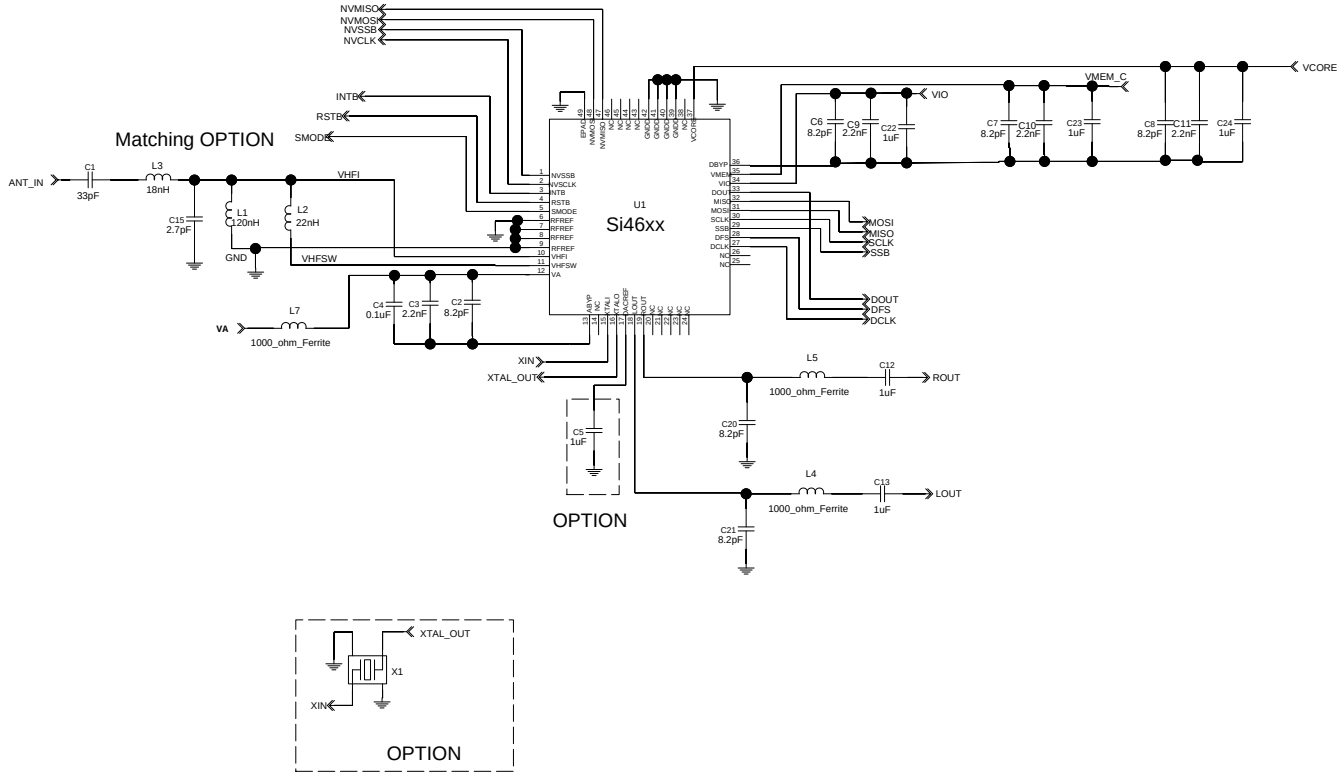


Figure 12. QFN Application Schematic

EMI Mitigation

Due to a high frequency (2880–3840 MHz) on-chip VCO, there is some conductive and magnetic coupling from the VCO to the adjacent traces. The VCO fundamental spur level can be reduced by adding external filtering and using the proper layout.

External filtering

- Add filter network comprising of L3 and C15 on the RF input trace (VHFI) for filtering the VCO spur (2880–3840 MHz). The capacitance C15 provides a low impedance path to ground, and inductor L3 provides high impedance to the VCO spur. The two component network attenuates the VCO spur from reaching external antenna port and radiating out. The values of these components are selected to achieve the balance between the sensitivity and the emission levels.
- Add low pass network C20 & L5 and C21 & L4 on the audio lines Right and Left respectively for attenuating the VCO coupling
- Add ferrite bead L7 on the VA supply line for providing high impedance to any VCO leakage
- Add high Self Resonant Frequency (>3 GHz) capacitors C2, C6, C7 and C8 on the supply lines to decouple the VCO leakage currents.

Layout Guide

The following placement/layout guidelines are suggested for 4-layer PCB:

- PCB layer assignment:
- Layer 1 top side placement and routing for RF and analog traces
- Layer 2 ground plane
- Layer 3 routing for high frequency digital traces and ground plane
- Layer 4 bottom side placement and routing for low frequency digital traces
- Minimum 6-mil trace
- Minimum 6-mil trace spacing
- 6-mil drill 9-mil plating for normal vias
- Minimum 10-mil component spacing
- Power routed by trace
- 0402 component size or larger

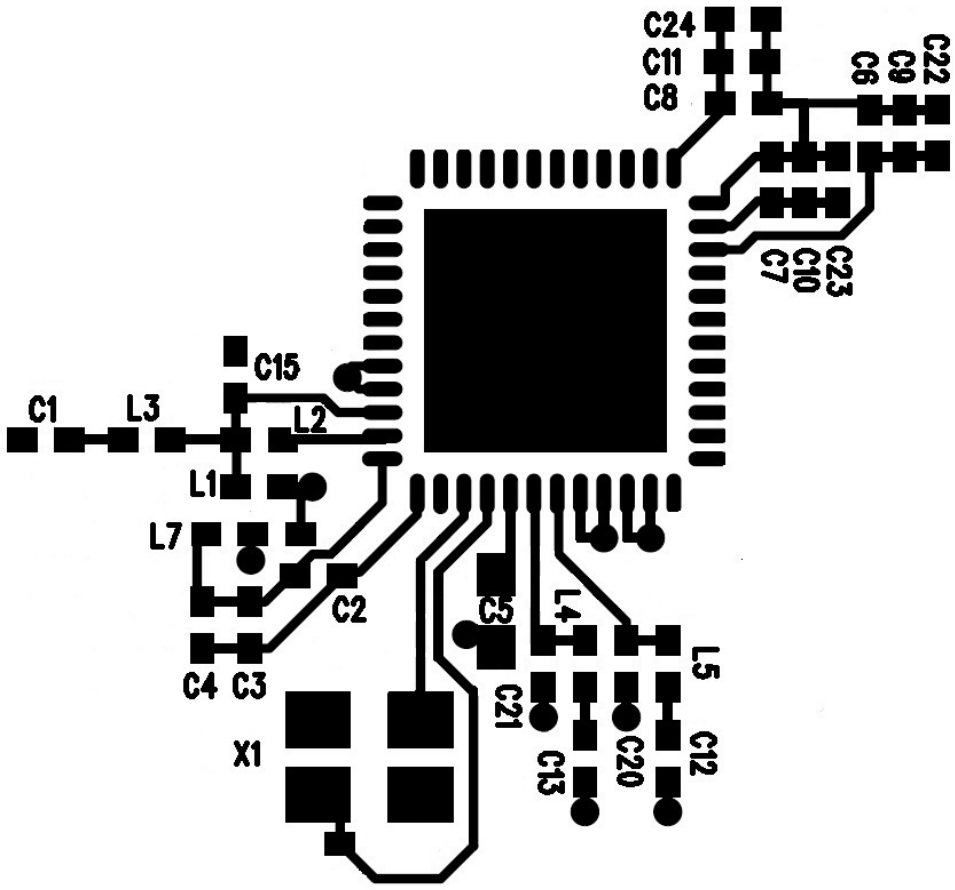


Figure 13. Si468x QFN Layout Design

Figure 13 shows critical layout with top side placement, top side routing, and crystal support. All bypass components are placed around the silicon as close as possible. A few things to note:

- The front end network components shall be placed as close as possible to the chip and as far away from noise sources such as clocks and digital circuits. L2 shall be routed to ground plane with a short trace and a via connection.
- The lowest value capacitor (8.2 pF) shall be placed the closest to the chip.
- Crystal and Audio traces shall be short in length and the recommended trace width is 6 mils.
- To minimize the loop area, all return currents shall be returned to its source as compactly as possible.

Front-End Matching

The components (C1, L1 and L2) are used for transforming the source impedance to match the input impedance of the Si468x front-end. The component values selected for the matching network achieves the best conducted sensitivity when used with 50 Ω source impedance. The matching components will require optimization when used with an actual antenna having different source impedance than 50 Ω.

For the DAB band, the matching component L2 connected to VHFSW switch will require optimization to maximize the voltage gain on the VHFI pin. Refer to property "0x1712" of AN649 for information on how to handle the VHFSW switch. The voltage gain is maximized by forming a high Q parallel LC resonant tank circuit. The inductor of the tank circuit is the parallel combination of L1 and L2. And, the tank capacitance includes the antenna capacitance, capacitance of the external front end network, PCB parasitic, internal chip parasitic and internal variable capacitance provided by on-chip varactor tuning.

With a given antenna source impedance and the parasitics (pcb and chip internal), the resonant peak of the LC tank circuit across the DAB band can be maximized by finding the right combination of L2 and the internal varactor capacitance. Refer to Appendix A for additional details on using internal varactor tuning. Note that the procedure outlined in Appendix A for internal varactor tuning is considering the signal generator source impedance (50 Ω) but the same procedure can be used with different antenna source impedance. To measure and optimize the network for a given source impedance, it is recommended to create an antenna model or dummy circuit. The input impedance of the dummy circuit across the DAB band should be 50 Ω and the output impedance of the dummy circuit should match the antenna source impedance. The internal varactor tuning procedure can then be followed after inserting a calibrated dummy circuit between the signal generator and the external front-end matching network.

For the FM/FMHD band, the components C1 and L1 will require optimization. A similar approach to DAB of using dummy circuit can be followed to find the right combination of C1 and L1 for achieving best FM/FMHD sensitivity for a given antenna source impedance. The capacitance provided by the internal varactor is not required for the FM/FMHD band, and therefore, for the FM/FMHD radiated sensitivity optimization it is not required to follow the internal varactor tuning.

Table 9. Application Schematic BOM

Ref Designator	Description	Value	Manufacture Part #
C1	CAP,SM,0402	33 pF	C0402C0G500-330JNP
L3	IND,SM,0402	18 nH	LQG15HS18NJ02D
C15	CAP,SM,0402	2.7 pF	GJM1555C1H2R7BB01D
L1	IND,SM,0402	120 nH	LQW15ANR12J00D
L2	IND,SM,0402	22 nH	LQW15AN22NH00D
C2,C6,C7,C8,C20 and C21	CAP,SM,0402	8.2 pF	GRM1555C1H8R2DA01D
L4,L5 and L7	Ferrite, 0402	1000 ohm	BLM15HG102SN1D
C3,C9,C10 and C11	CAP,SM,0402	2.2 nF	C0402X7R500-222KNP
C4,C22,C23 and C24	CAP,SM,0402	0.1 µF	C0402X7R100-104KNP
C12,C13 and C5	CAP,SM,0402	1 µF	C1005X5R1C105K050BC
X1	Crystal	19.2	Abracon, ABM8-19.200MHz-10-1-U_T, 19.2 MHz

Note: The application schematic and the layout shown in this appendix are applicable for WLCSP package as well. Refer to the main layout guide for WLCSP package layout guidance.

Document Change List

Revision 0.1 to Revision 0.2

- Added QFN section schematic design and layout guide.
- Added description of C3 in option BOM of WLCSP on page 8.
- Changed description of C8, C9, C10 in optional BOM of WLCSP on page 8.

Revision 0.2 to Revision 0.3

- Updated schematics (both WLCSP and QFN) to reflect the front-end network recommendation to achieve the best conducted sensitivity.
- Updated schematics (both WLCSP and QFN) to reflect A10 production pin-out definition.
- Updated WLCSP layout on GNDA for DFM optimization. Original recommendation in 0.2 has no RF performance difference compared to the current recommendation.
- Updated design recommendation for headphone antenna.

Revision 0.3 to Revision 0.4

- Added Appendix B—Applies to FW Release Si46xx_130215.
- Added Appendix C—Applies to FW Release Si46xx_130524.

Revision 0.4 to Revision 0.5

- Changed “Si46xx” to “Si468x” throughout.

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