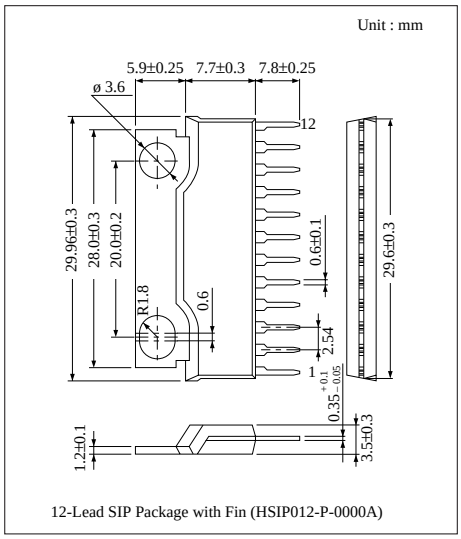
# AN7169

## Dual 5.8W Audio Power Amplifier Circuit

### ■ Overview

The AN7169 is an integrated circuit designed for low distortion, low noise and low power dissipation audio set of 5.8W (13.2V, 4Ω) output. Stereo operation is enabled due to incorporating two amplifiers on one chip. 12-pin SIL package enabled compact and high integrated set. Thermal protection, short protection and excessive voltage protection circuits are built in.



12-Lead SIP Package with Fin (HSIP012-P-0000A)

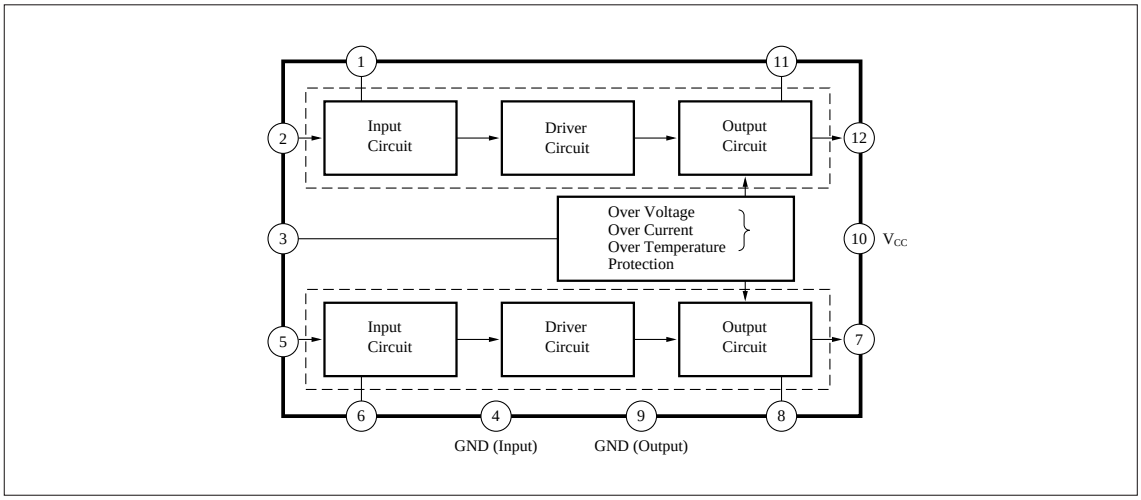
### ■ Features

- Highly stable operation
- Low distortion
- Low quiescent current
- Low noise
- Low shock noise from power ON/OFF operation
- Built-in muting circuit
- Fewer external components
- Incorporating protection circuits

### ■ Pin Descriptions

| Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|
| 1 | NFB Ch.1 | 7 | Output Ch.2 |
| 2 | Input Ch.1 | 8 | Bootstrap Ch.2 |
| 3 | Ripple Filter | 9 | GND (Output) |
| 4 | GND (Input) | 10 | $V_{CC}$ |
| 5 | Input Ch.2 | 11 | Bootstrap Ch.1 |
| 6 | NFB Ch.2 | 12 | Output Ch.1 |

### ■ Block Diagram



## ■ Absolute Maximum Ratings (Ta= 25˚C)

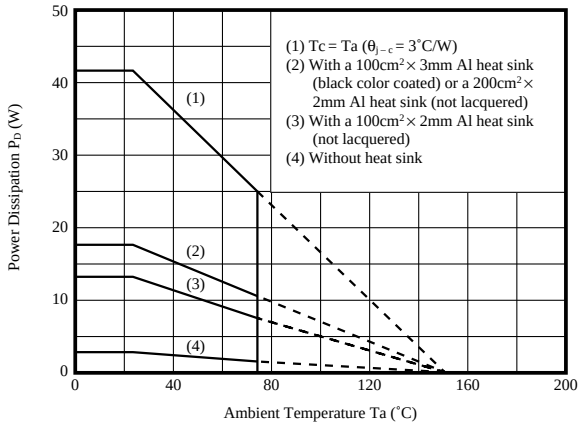
| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 24 | V |
| Supply Current | $I_{CC}$ | 4.0 | A |
| Power Dissipation | $P_D$ | 41.7 Note 1) | W |
| Peak Supply Voltage | $V_{CC\ (surge)}$ | 50 Note 2) | V |
| Operating Ambient Temperature | $T_{opr}$ | – 30 ~ + 75 | ˚C |
| Storage Temperature | $T_{stg}$ | – 55 ~ + 150 | ˚C |

Note 1) $R_{\theta j-c}$ = 3˚C/W
Note 2) Voltage applied time = 0.2s

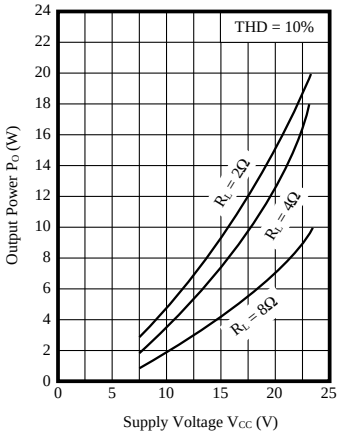
## ■ Electrical Characteristics ($V_{CC}$ = 13.2V, f = 1kHz, $R_L$= 4Ω, Ta= 25˚C)

| Parameter | Symbol | Condition | min. | typ. | max. | Unit |
|---|---|---|---|---|---|---|
| Quiescent Circuit Current | $I_{CQ}$ | $V_i$= 0mV | 30 | 55 | 100 | mA |
| Voltage Gain | $G_V$ | $P_O$= 0.5W | 45 | 47 | 49 | dB |
| Total Harmonic Distortion | THD | $P_O$= 0.5W, f= 1kHz | — | 0.06 | 0.5 | % |
| | | $P_O$= 0.5W, f= 100Hz | — | 0.07 | — | |
| | | $P_O$= 0.5W, f= 10kHz | — | 0.15 | — | |
| Maximum Output | $P_O$ | THD = 10% | 5.0 | 5.7 | — | W |
| | | THD = 10%, $R_L$= 2Ω | — | 8.9 | — | |
| | | THD = 10%, $R_L$= 8Ω | — | 3.1 | — | |
| Output Noise Voltage | $V_{no}$ | $R_g$= 10kΩ, 1000pF, f= 15Hz ~ 30kHz, 12dB/OCT | — | 0.5 | 1.5 | mV |
| | | $R_g$= 10kΩ, 1000pF, Without Filter | — | 0.65 | — | |
| Channel Balance | CB | $P_O$= 0.5W | — | 0 | 1.0 | dB |
| Channel Separation | CS | $P_O$= 0.5W | 40 | 50 | — | dB |
| Ripple Rejection Ratio | RR | $P_O$= 0.5W, $V_{ripple}$ = 280$mV_{rms}$, $f_{ripple}$ = 120Hz Sine wave | 35 | 45 | — | dB |
| Offset Voltage | $V_{O\ (offset)}$ | $V_i$= 0mV | — | 0 | 200 | mV |

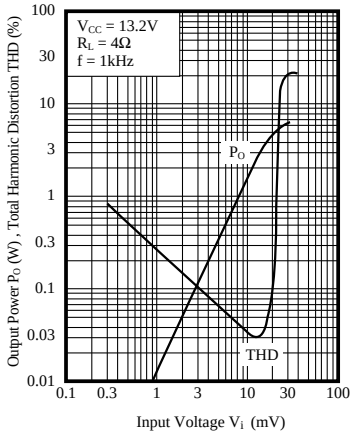
$P_D$ – Ta



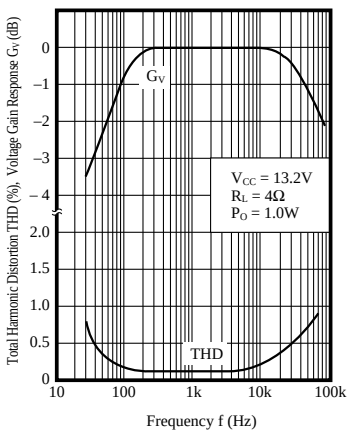
$P_O - V_{CC}$



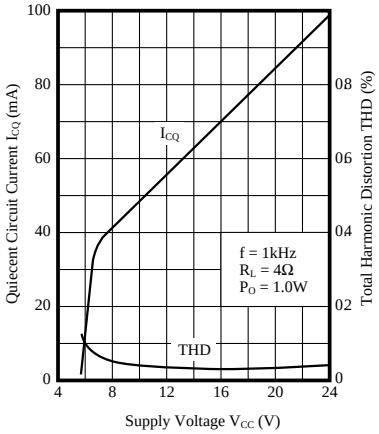

$P_O$, THD – $V_i$



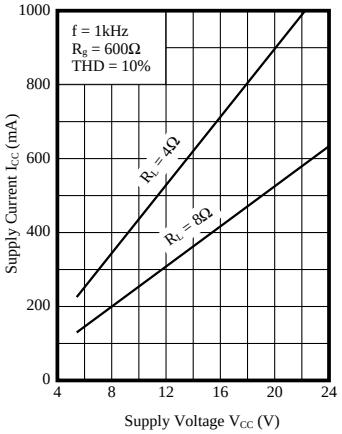

THD, $G_V$ – f



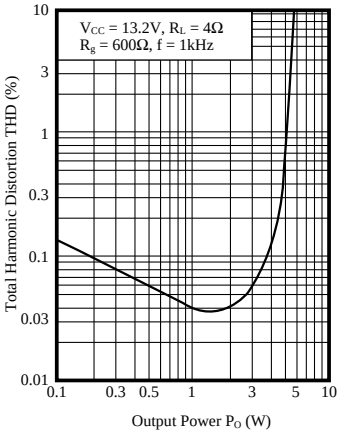

$I_{CQ}$, THD – $V_{CC}$



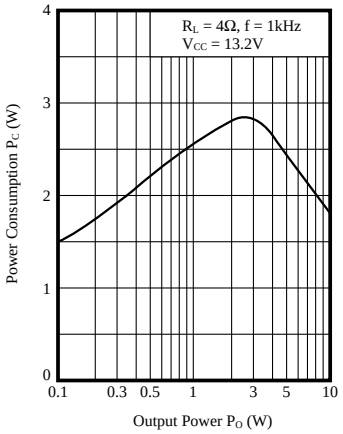

$I_{CC}$ – $V_{CC}$ (Single Channel)



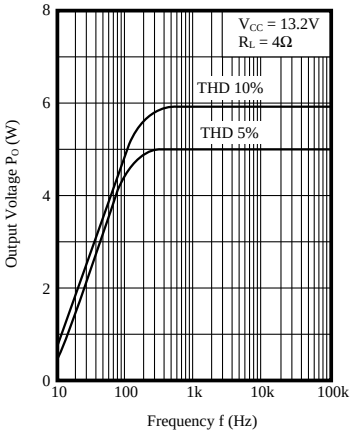

THD – $P_O$



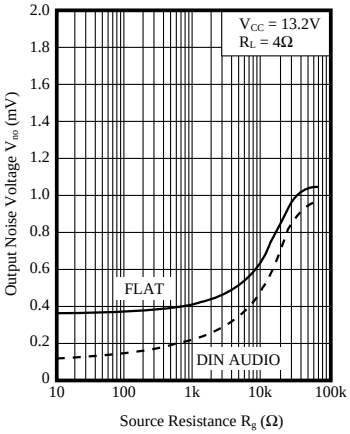

$P_C$ – $P_O$ (Single Channel)




$P_O$ – f

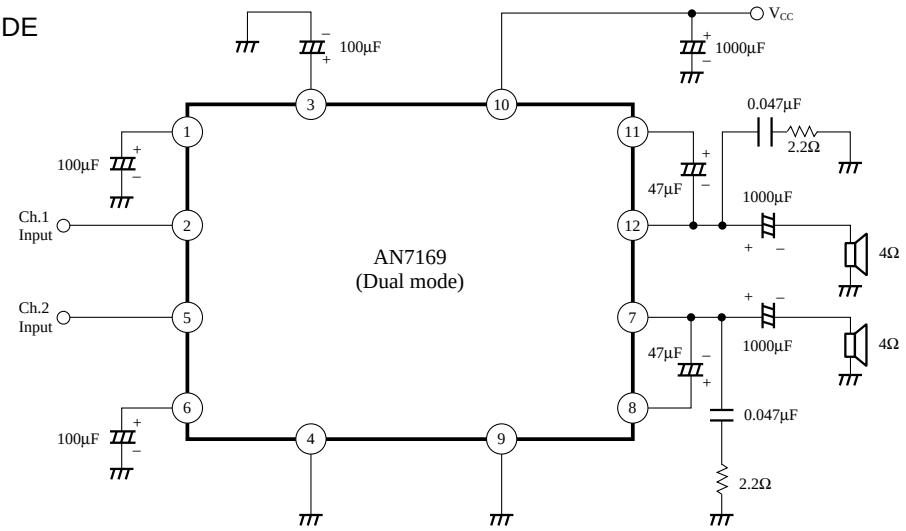



$V_{no}$ – $R_g$

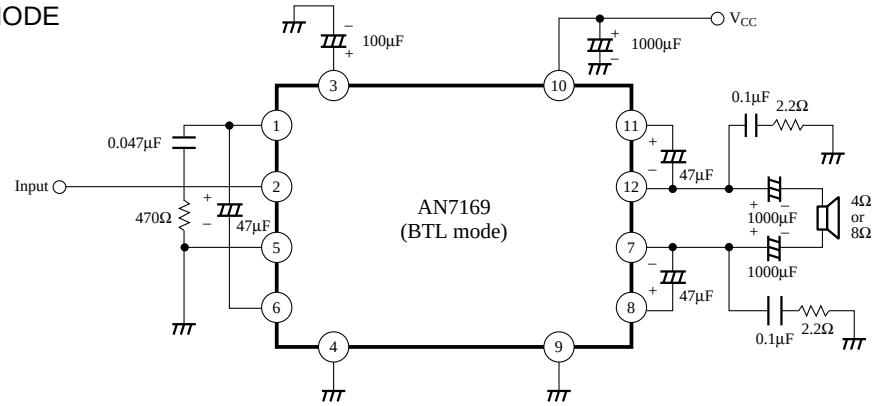


## ■ Application Circuits

• DUAL MODE




• BTL MODE




## ■ Printed Circuit Board Layout